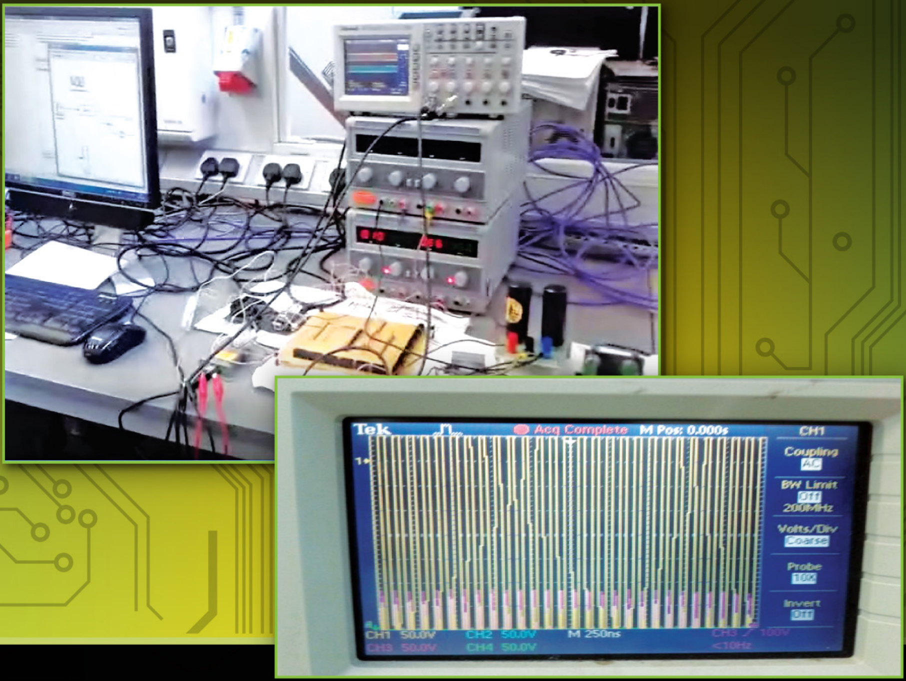
# Power Electronic Converters

## Interactive Modelling Using Simulink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**Narayanaswamy P R Iyer**

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## Interactive Modelling Using Simulink

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By

Narayanaswamy P. R. Iyer

CRC Press
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Printed on acid-free paper

International Standard Book Number-13: 978-0-8153-6819-9 (Hardback)

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*Dedicated to the memory of the late Dr. Venkat Ramaswamy,*

*who was a great source of inspiration.*

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# Preface

This textbook provides a step-by-step method for the development of a virtual interactive power electronics laboratory. Therefore, this textbook is suitable for undergraduates and graduates in electrical and electronics engineering for their laboratory courses and projects in power electronics. This textbook is equally suitable for practising professional engineers in the power electronics industry. They can develop an interactive virtual power electronics laboratory as outlined in this textbook and perform simulation of their new power electronic converter designs. Similarly, instructors may find this textbook useful for running an interactive virtual laboratory course or a new project in the area of power electronics.

The topic of power electronic converter modelling is a growing field. There are many software packages available for this purpose. Most of them are power electronic circuit simulation packages using semiconductor and other passive components. Circuit component-level simulation of power electronic converters is a basic or fundamental level of modelling. A higher level of modelling is the system model, which solves the characteristic equations describing the behaviour of the power electronic converter. The Simulink® software, developed by The Mathworks Inc., USA, can be used to develop advanced system models as well as circuit component-level models for any given power electronic converter. Moreover, it is possible to develop both interactive system models and circuit component-level models using Simulink, which is a special feature. Therefore, I have used Simulink to develop interactive models of power electronic converters presented in this textbook. Unless specified otherwise, the term *model* in this textbook refers to Simulink model.

Chapter 1 provides the introduction, where the significance of modelling power electronic converters, the novelty of this textbook and the reason for the choice of the Simulink software are presented. The fundamentals of developing interactive models are presented in Chapter 2 with an example of a three-phase half-wave thyristor rectifier converter. This chapter also highlights the advantage of interactive modelling, which is primarily the saving in time in testing power electronic converters by model simulation. Interactive system models of power electronic converters are presented in the following order:

AC to DC, DC to AC, DC to DC and AC to AC converters are presented in Chapters 3 to 6, respectively. The buck converter switched mode power supply is presented in Chapter 7. This is followed by selected fourth-order DC to DC converters in Chapter 8 and, finally, three-phase multilevel inverters in Chapter 9.

To verify the performance of the system models of the power electronic converters in Chapters 3 to 9, Chapter 10 has been added. Chapter 10 provides the interactive component-level models of the power electronic converters presented in Chapters 3 to 9.

An interactive component-level model and real-time software in the loop (SIL), also known as processor in the loop (PIL) simulation of a single-phase half H-bridge sine pulse width modulation (PWM) inverter is presented in Chapter 11. This work was carried out by the author while a research fellow in the Faculty of Engineering, University of Nottingham, UK. The author is grateful to Prof. Alberto Castellazzi and Prof. Pat Wheeler, both of the School of Electrical and Electronics Engineering, University of Nottingham, UK, for their support in carrying out this work.

As mentioned before, it is possible to develop system models of power electronic converters using the Simulink block set and circuit component-level models using the Simscape-Electrical, Power Systems and Specialized Technology block sets.

Much of the material presented in this textbook is work undertaken by the author during his Master of Engineering degree by research programme at the University of Technology Sydney, NSW, Australia. The author is grateful to the late Dr. Venkat Ramaswamy, formerly senior lecturer, School of Electrical Engineering, University of Technology Sydney, NSW, who was a great source of encouragement and support. The author also wishes to thank Dr. Jianguo Zhu, head, School of Electrical Engineering, University of Technology Sydney, NSW, for his support.

The whole of Chapter 8 and the models in Sections 5.4, 5.7 and 5.10 and in Sections 9.4 and 9.7 are my original contributions and are not a part of the above research work.

No end of chapter exercises are given, as this seems to be unnecessary. The reader can practice interactive modelling according to the method outlined here in this book and using the many textbooks on power electronics, some of which are mentioned in the references at the end of each chapter.

The step-by-step interactive modelling details are explained in Chapter 2 only. They are not repeated in Chapters 3 to 11, as most of the sources and components used in the power electronic converter shown in Chapter 2 are repeatedly used in the converters presented in these chapters.

The whole of Chapter 10, excluding Sections 10.7, 10.8, 10.10 and 10.11, is suitable for a senior-level undergraduate curriculum in power electronics.

The model files in this textbook can be found on the website https://www.crcpress.com/Power-Electronic-Converters-Interactive-Modelling-Using-Simulink/Iyer/p/book/9780815368199. Instructors can download a copy of these model files.

I presume that students, instructors and practising professional engineers in the industry alike will find this textbook useful.

I would like to thank Ms. Nora Konopka, Editorial Director: Engineering, CRC Press for her help and support. Also, many thanks to the anonymous reviewers for their valuable comments.

Finally, I would like to thank my wife, Mythili Iyer, for her patience and understanding. Without her support, this work would not have been possible.

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# 1

# *Introduction*

## 1.1 Background

The performance of power electronic converters can be studied using mathematical equations which describe the behaviour of the particular converter. For example, the load current and load voltage pattern for a single-phase full-wave diode bridge rectifier delivering power to a series-connected R–L load can be studied by developing and then solving the differential equation describing the behaviour of this converter. The power electronic converter supplying power to these loads can be developed either as a system model that duplicates the performance of this converter or as a circuit model using the actual power electronic semiconductor and other passive components.

The models developed in this book are system models that solve the equations describing the behaviour of the system. A relatively new concept known as the *switching function concept* is used to simulate the behaviour of the power electronic converters [1–9]. At this stage, it will be appropriate to mention the difference between the system model and the circuit component-level model that is obtained by electronic circuit simulation software. While the system model solves the characteristic equation describing the behaviour of the system, circuit component-level models developed using electronic circuit simulators use the passive and active semiconductor component parameters, such as, for example, ON and OFF switch resistance, voltage and current gain values, parasitic or stray capacitances between junctions, junction potentials, inherent inductive reactance and so on arranged as a subcircuit (also called the *equivalent circuit* of the semiconductor component or the device) to solve a given power electronic converter. In the system models, the characteristic equation describing the behaviour of the system can be either algebraic or differential.

## 1.2 Why Use Simulink?

In this book, I have used Simulink® software developed by The Mathworks Inc. [10]. Simulink has the following advantages compared with other software packages with regard to power electronic circuit simulation:

- Facility to develop interactive models with user dialogue boxes for power electronic systems, with which any given power electronic converter can be tested by entering the parameters in the dialogue boxes without actually going into each block of the model to enter the data. This saves time for the user and finds applications in the virtual power electronics laboratory. This is one of the unique features in Simulink.
- Harmonic analysis of power electronic converters can be easily developed with Powergui in the PowerSystems block set.
- Many non-linear phenomena such as pulse width modulation (PWM) techniques can be easily verified.
- Many power electronic circuits can be studied by modelling techniques and can be verified by semiconductor components in the PowerSystems block set; that is, it is possible to develop both system models based on the characteristic equations describing the behaviour of the system and electronic circuit component-level models utilising the equivalent circuit parameters of the semiconductor component.
- Facility to study analogue and digital gate drives used in power electronic circuits.
- Facility to save data in workspace, which can be later brought to the MATLAB® window for further mathematical processing, editing graphics and so on.

## 1.3 Significance of Modelling

The significance of the term *modelling* is summarized here:

- Modelling a physical system refers to the analysis and synthesis to arrive at a suitable mathematical description encompassing the dynamic characteristics of the system in terms of its parameters [11].
- Models are used to predict the performance of the given system [11].

- Model prediction permits engineers to think of its potential applications and practical implementation and to develop various control strategies [11].
- Reduces time involved or shortens the overall design process [12, 13].
- Saves time and money as compared with procuring, installing and testing the system in the laboratory, especially when the system is too bulky [11].
- Simulation refers to performing experiments on the model [11].
- Computer simulation plays a vital role in the R&D of power electronic devices for its high manoeuvrability, low cost and ability to speed up system implementation [14].

## 1.4 Book Novelty

The book mainly concentrates on interactive modelling of selected power electronic converters using Simulink. This book's novelties are given here:

1. The interactive system model for single-phase AC to DC converter using diodes developed here is new and different from that existing in the literature references.
2. The interactive system model for single-phase AC to DC converter using silicon-controlled rectifiers (SCRs) developed here is new.
3. The interactive system model for three-phase inverter in the discontinuous current conduction (120°) mode is new.
4. The interactive system model three-phase sine-triangle carrier PWM inverter is new.
5. The interactive system models for three-phase thyristor AC to AC controllers are new.
6. The interactive system model for buck converter switched mode power supply (SMPS), especially the feedback control part using a triangle carrier is new. This is different from that existing in the literature references, where a saw-tooth carrier is used.
7. The interactive system model for quadratic boost and ultra-lift Luo converters are new.
8. The interactive system models developed for three-phase diode-clamped three-level inverter (DCTLI), flying-capacitor three-level inverter (FCTLI) and five-level cascaded H-bridge inverter (FLCHBI) are new.

9. The interactive system models developed for multi-carrier sine-phase shift PWM (MSPSPWM) and multi-carrier sine-level shift PWM (MSLSPWM) are new.
10. The software in the loop (SIL) or processor in the loop (PIL) simulation is presented with a power electronic converter example.
11. System models of power electronic converters are verified for performance using interactive circuit component-level models developed using Simscape-Electrical, Power Systems and Specialized Technology block sets.

## 1.5 Book Outline

In this text book, interactive system models for power electronic converters have mainly been developed and are then verified using interactive circuit component-level models.

Chapter 1 provides the introduction. In Chapter 2, the method of developing and advantage of interactive modelling are presented with a power electronic converter example. Chapters 3 through 6 provide building of interactive system models for AC to DC, DC to AC, DC to DC and AC to AC converters respectively. In Chapter 3, system models for single-phase full-wave diode bridge rectifier (FWDBR), single-phase full-wave thyristor silicon controlled rectifier (SCR), controlled bridge rectifier (FWCBR) and three-phase FWDBR are presented. In Chapter 4, system models for continuous current conduction (180°) mode and discontinuous current conduction (120°) mode inverters and the three-phase sine-triangle carrier PWM inverter are presented. In Chapter 5, system models for second-order DC to DC converters such as buck, boost and buck–boost converters are presented. In Chapter 6, three-phase thyristor AC to AC controllers connected in series with resistive loads in star with isolated neutral and three-phase thyristor AC to AC controllers in series with resistive load in delta are presented. In Chapter 7, the system model for SMPS using a buck converter is presented. The system models for fourth-order DC to DC converters such as single-ended primary inductance converters (SEPIC), quadratic boost and ultra-lift Luo converters are presented in Chapter 8. Chapter 9 deals with system models for three-phase DCTLI, three-phase FCTLI, three-phase FLCHBI, multi-carrier sine-phase shift (MSPS) and multi-carrier sine-level shift (MSLS) PWM. Finally, system models of power electronic converters discussed in Chapters 3 through 9 are verified for performance using circuit component-level models in Chapter 10, where semiconductor and passive components from Simscape-Electrical, Power Systems and Specialized Technology block sets are used. An interactive component-level model and real-time SIL or PIL simulation of a single-phase half H-bridge sine PWM inverter is presented in Chapter 11.

In the system- and component-level models for these power electronic converters, it is the aim to simulate any given power electronic converter by entering the parameters of the converter into the appropriate dialogue boxes, without altering the inner details of the model. This easy-to-use system, and component-level models, save time and are suitable for virtual power electronic laboratory applications.

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# 2

# *Fundamentals of Interactive Modelling*

## 2.1 Introduction

In this chapter, fundamentals relating to the interactive modelling concept are introduced. Interactive modelling is a facility available in the Simulink® software. With an interactive model, the user can simulate and solve the problem in hand without going into each of the model blocks to enter parameters. If the same or different users want to simulate the very same power electronic converter topology with different parameters, then it is easy to use the interactive model. The same user or different users can enter their data in the appropriate dialogue boxes and solve their power electronics design problems. This saves time, as the user does not have to click each module in the model to enter the data. The method of interactive model development for power electronic converters is illustrated with an example.

## 2.2 Interactive Modelling Concept

Interactive modelling is a facility available in the Simulink software [1]. Interactive modelling is suitable for use in academic research and virtual power electronics laboratories in universities, as well as in a power electronic converter design and manufacturing environment. Imagine a power electronics industry manufacturing different types of DC to DC converters. Assume that different clients order the same DC to DC buck converter, each specifying different input voltage, output voltage, output power, output voltage and inductor current ripple and switching frequency requirements. With component values designed by the industry for each converter specification using the well-known modelling equations for the buck converter, the industry can easily and quickly test the performance of each of the buck converters using an interactive model. This is because the interactive model provides dialogue boxes where the designer can easily enter parameter values and test their performance in less time as compared with a conventional model where the designer has to open each component subsystem in the model to enter their parameter values. With different specifications for the buck converter, the time consumed for testing with a conventional model will be greater compared with testing the same with an interactive model. Thus, interactive modelling accelerates the manufacturing process and saves time and money.

## 2.3 Interactive Modelling Procedure

The interactive modelling procedure depends on the topology of the power electronic converter such as the value of the DC voltage source, the amplitude, frequency and phase of single-phase or three-phase AC source, pulse amplitude, frequency, pulse width and phase delay for the gate drive used for the semiconductor switches, component values for resistors, inductors and capacitors used in the model. These are tabulated in Table 2.1.

Interactive modelling involves assigning a variable name to each of the parameter values in Table 2.1 that are used in the model. In some cases, parameters such as on–off resistance and junction forward voltage for semiconductor switches may be built into the model already available, and in such cases, these can be neglected. Then, identical sources or components that form one group are selected by clicking the mouse and the subsystem is created from a selection using the 'Diagram' menu. Then, for the subsystem selected, the 'Create Mask' option from the 'Diagram' menu is used to develop the interactive model. 'Create Mask', or 'Edit Mask' if the mask is already created, opens up the Mask Editor. Then, in the Mask Editor, the 'Parameters and Dialog' menu is selected. In this menu, the user clicks the 'Edit' button, then enters the parameter description and parameter group variable name. The parameter group variable name entered must be the one

**TABLE 2.1**

Interactive Model Parameters

| Sl. No. | Source/Component | Parameter Values |
|---|---|---|
| 1 | DC voltage source | Amplitude |
| 2 | Single-phase AC voltage source | Amplitude, frequency, phase delay |
| 3 | Three-phase AC voltage source | Amplitude, frequency, phase angle, phase delay |
| 4 | Gate pulse drive | Amplitude, frequency, pulse width, phase delay |
| 5 | Resistor, inductor, capacitor, diode | Values in ohms, henries, farads, on–off resistance and junction forward voltage |
| 6 | Semiconductor switch (BJT, IGBT, MOSFET, SCR) | Gate threshold voltage, on–off resistance and junction forward voltage |

used for the source/component in the subsystem. This is repeated for each parameter used in the created subsystem. After clicking the 'Apply' button, the user selects the 'Initialization' menu from the Mask Editor. Any value specification or condition to be fulfilled for parameter variables is entered in the 'Initialization commands' box. Finally, the 'Documentation' menu in the Mask Editor is selected, where the name or title of the subsystem and a brief description relating to the numerical value showing the unit to be entered in each of the pop-up menus or dialogue boxes are entered. Then, the 'Apply' and 'OK' buttons are clicked to complete the interactive model development. In the next section, the interactive model development is explained with an example.

### 2.3.1 Interactive Model Development

In this section, the interactive model development process is explained with an example of a power electronic converter model. This method is the same irrespective of whether a power electronic converter component-level or system-level model is used. To encompass all the sources/components specified in Table 2.1, a three-phase half-wave silicon controlled rectifier (SCR) converter is considered here [2]. Figure 2.1 shows a three-phase SCR half-wave converter. A three-phase 120 V root mean square (RMS) line-to-neutral, 60 Hz AC voltage source is used. The parameters used for the model are tabulated in Table 2.2.

In Figure 2.1, the three-phase AC voltage sources R, Y and B are connected to the anodes of SCRs SCR1, SCR2 and SCR3, respectively. The cathodes of these three SCRs are tied together and connected to a single-phase load comprising R1, L1 and E. The gate pulse firing angle $\alpha$ for SCR1 in Phase R is 90°. The gate pulse firing angle for SCR2 in Phase Y will be $(\alpha+120)$ and that for SCR3 in Phase B will be $(\alpha+240)°$. A suitable amplitude for the gate pulse depends on the SCR gate turn-on threshold voltage, and a suitable gate pulse width is provided that depends on the data sheet for the relevant SCR. These gate drives for the three SCRs are not shown in Figure 2.1 for clarity. The interactive model development for this converter is explained next.

Figure 2.2 shows the interactive model of the three-phase SCR half-wave controller and Figure 2.3 shows the same model with interactive blocks. Figure 2.4a–f shows the various subsystems used in the model shown in Figure 2.2. These are explained as follows:

The three-phase AC voltage source subsystem is shown in Figure 2.4a. The three single-phase AC sources marked AC Voltage Source, AC Voltage Source1 and AC Voltage Source2 form the three-phase AC Voltage Source block. The three-phase half-wave SCR converter subsystem is shown in Figure 2.4b, and consists of three SCRs marked Thyristor, Thyristor1 and Thyristor2. The gate pulse generator subsystem is shown in Figure 2.4c, and consists of three gate drives marked Pulse Generator, Pulse Generator1 and Pulse Generator2. The RLE (R–resistor; L–inductor; E–EMF source, where E can be a DC voltage source, battery or AC voltage source and has to

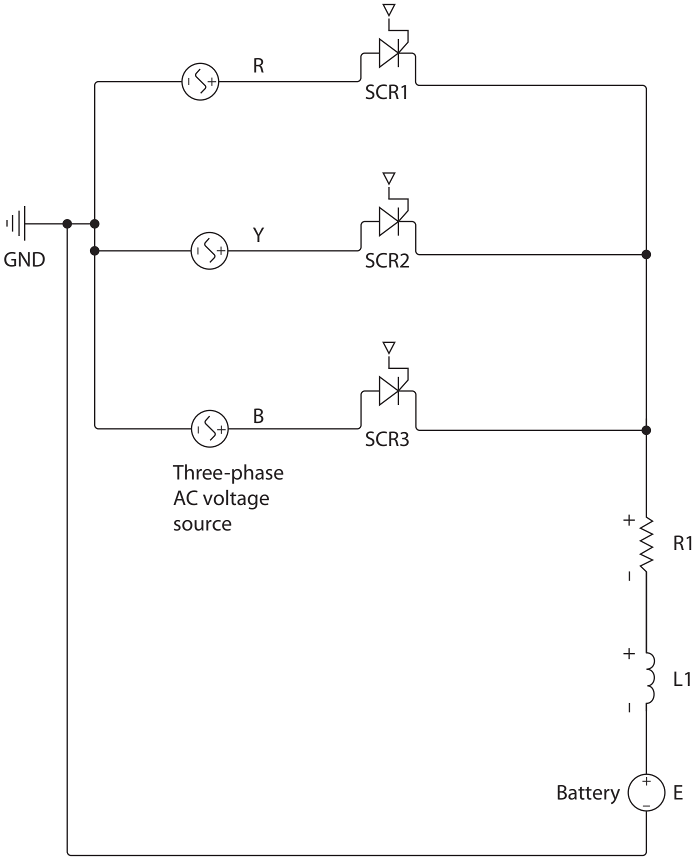

R
SCR1
Y
SCR2
B
SCR3
GND
Three-phase
AC voltage
source
+
R1
–
+
L1
–
Battery
+
–
E

**FIGURE 2.1**
Three-phase half-wave SCR converter.

**TABLE 2.2**
Model Parameters

| Sl. No. | Parameter | Value | Unit |
|---|---|---|---|
| 1 | RMS line-to-neutral input voltage | 120 | Volts |
| 2 | Frequency | 60 | Hertz |
| 3 | Gate drive amplitude | 10 | Volts |
| 4 | Gate drive frequency | 60 | Hertz |
| 5 | SCR firing angle for reference phase | 90 | Degrees |
| 6 | Load resistance | 0.5 | Ohms |
| 7 | Load inductance | 6.5e−3 | Henries |
| 8 | Load battery DC voltage | 10 | Volts |

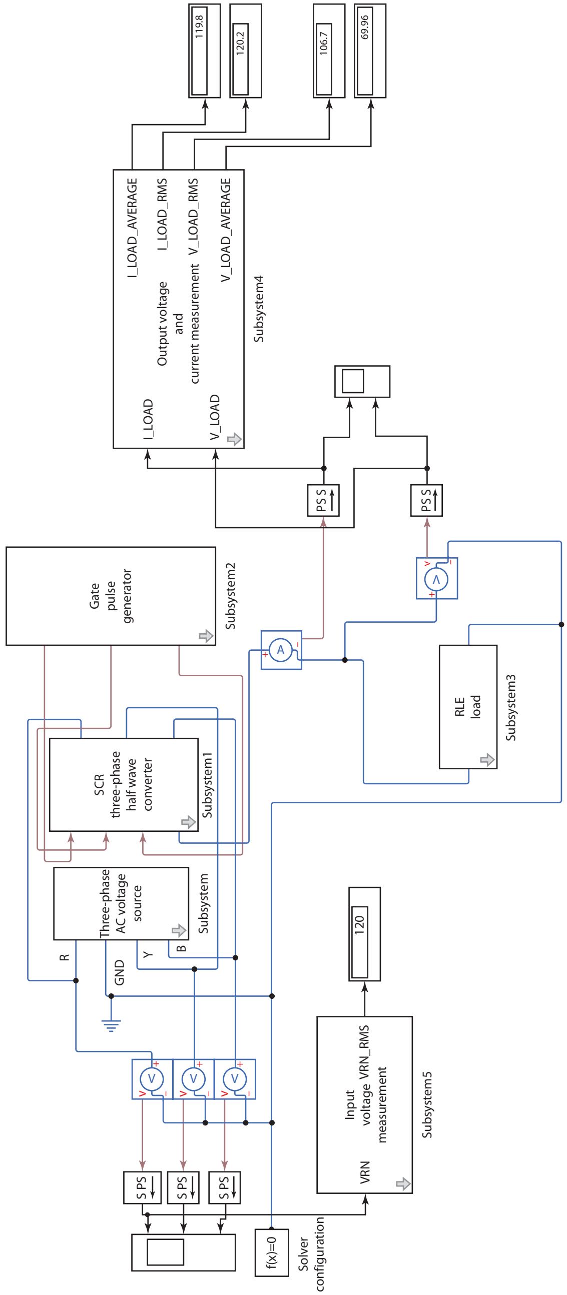
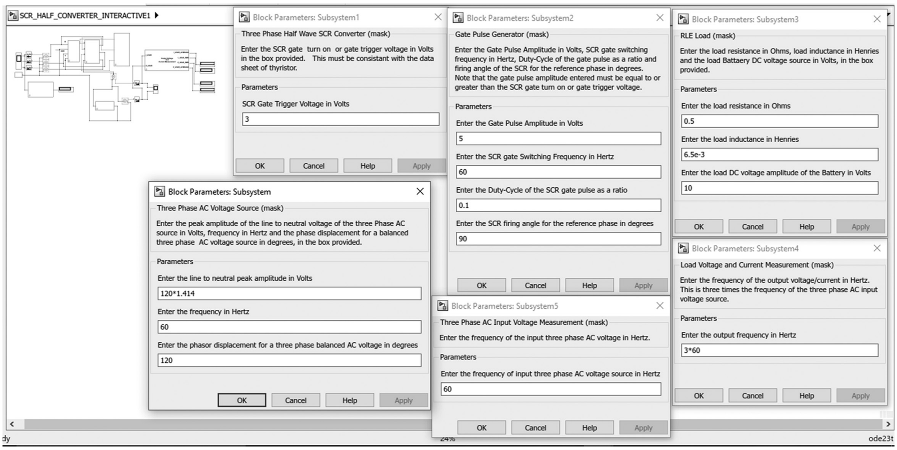

119.8
120.2
106.7
69.96
I_LOAD_AVERAGE
I_LOAD_RMS
V_LOAD_RMS
V_LOAD_AVERAGE
I_LOAD
V_LOAD
Output voltage and current measurement
Subsystem4
PS S
PS S
Gate pulse generator
Subsystem2
A
V
SCR three-phase half wave converter
Subsystem1
RLE load
Subsystem3
Three-phase AC voltage source
Subsystem
R
GND
Y
B
V
V
V
S PS
S PS
S PS
120
Input voltage measurement
VRN_RMS
VRN
Subsystem5
f(x)=0
Solver configuration

**FIGURE 2.2**
Three-phase half-wave SCR converter.



Block Parameters: Subsystem1

Three Phase Half Wave SCR Converter (mask)

Enter the SCR gate turn on or gate trigger voltage in Volts in the box provided. This must be consistant with the data sheet of thyristor.

Parameters

SCR Gate Trigger Voltage in Volts: 3

Block Parameters: Subsystem2

Gate Pulse Generator (mask)

Enter the Gate Pulse Amplitude in Volts, SCR gate switching frequency in Hertz, Duty-Cycle of the gate pulse as a ratio and firing angle of the SCR for the reference phase in degrees. Note that the gate pulse amplitude entered must be equal to or greater than the SCR gate turn on or gate trigger voltage.

Parameters

Enter the Gate Pulse Amplitude in Volts: 5

Enter the SCR gate Switching Frequency in Hertz: 60

Enter the Duty-Cycle of the SCR gate pulse as a ratio: 0.1

Enter the SCR firing angle for the reference phase in degrees: 90

Block Parameters: Subsystem3

RLE Load (mask)

Enter the load resistance in Ohms, load inductance in Henries and the load Battaery DC voltage source in Volts, in the box provided.

Parameters

Enter the load resistance in Ohms: 0.5

Enter the load inductance in Henries: 6.5e-3

Enter the load DC voltage amplitude of the Battery in Volts: 10

Block Parameters: Subsystem

Three Phase AC Voltage Source (mask)

Enter the peak amplitude of the line to neutral voltage of the three Phase AC source in Volts, frequency in Hertz and the phase displacement for a balanced three phase AC voltage source in degrees, in the box provided.

Parameters

Enter the line to neutral peak amplitude in Volts: 120*1.414

Enter the frequency in Hertz: 60

Enter the phasor displacement for a three phase balanced AC voltage in degrees: 120

Block Parameters: Subsystem4

Load Voltage and Current Measurement (mask)

Enter the frequency of the output voltage/current in Hertz. This is three times the frequency of the three phase AC input voltage source.

Parameters

Enter the output frequency in Hertz: 3*60

Block Parameters: Subsystem5

Three Phase AC Input Voltage Measurement (mask)

Enter the frequency of the input three phase AC voltage in Hertz.

Parameters

Enter the frequency of input three phase AC voltage source in Hertz: 60

**FIGURE 2.3**
Three-phase half-wave SCR converter with interactive blocks.

be understood by referring to the circuit schematic) load subsystem is shown in Figure 2.4d, consisting of a resistor, inductor and a DC voltage source all connected in series. The output voltage and current measurement subsystem is shown in Figure 2.4e, where RMS and MEAN value measurement blocks are used to display the RMS and mean or average value of the output voltage and currents. The input AC voltage measurement block is shown in Figure 2.4f, consisting of an RMS measurement block to display the RMS value of the line-to-neutral input voltage. Detailed interactive model formation is discussed in the following sections.

### 2.3.2 Three-Phase AC Voltage Source

The three-phase AC voltage source subsystem is shown in Figure 2.4a. The dialogue box relating to the AC voltage source module connected to Phase R is shown in Figure 2.5a. The peak amplitude variable is entered as 'A' in volts. The phase shift is entered as 'phi*0' in degrees. The frequency is entered as 'f' in hertz. In the AC Voltage Source1 module relating to Phase Y and the AC Voltage Source2 module relating to Phase B, the entry corresponding to the phase shift is entered as 'phi*(–1)' and 'phi*(1)' (or 'phi*(–2)'), respectively, with all other entries as previously. The following procedure is used to make the three-phase AC voltage source model interactive.

- *Step 1:* In Figure 2.2, before masking, which appears like Figure 2.4a, select AC Voltage Source, AC Voltage Source1 and AC Voltage Source2 using the mouse pointer. Then, click Diagram → Subsystem and Model Reference → Create Subsystem from the selection to form a subsystem called 'Three-Phase AC Voltage Source'.

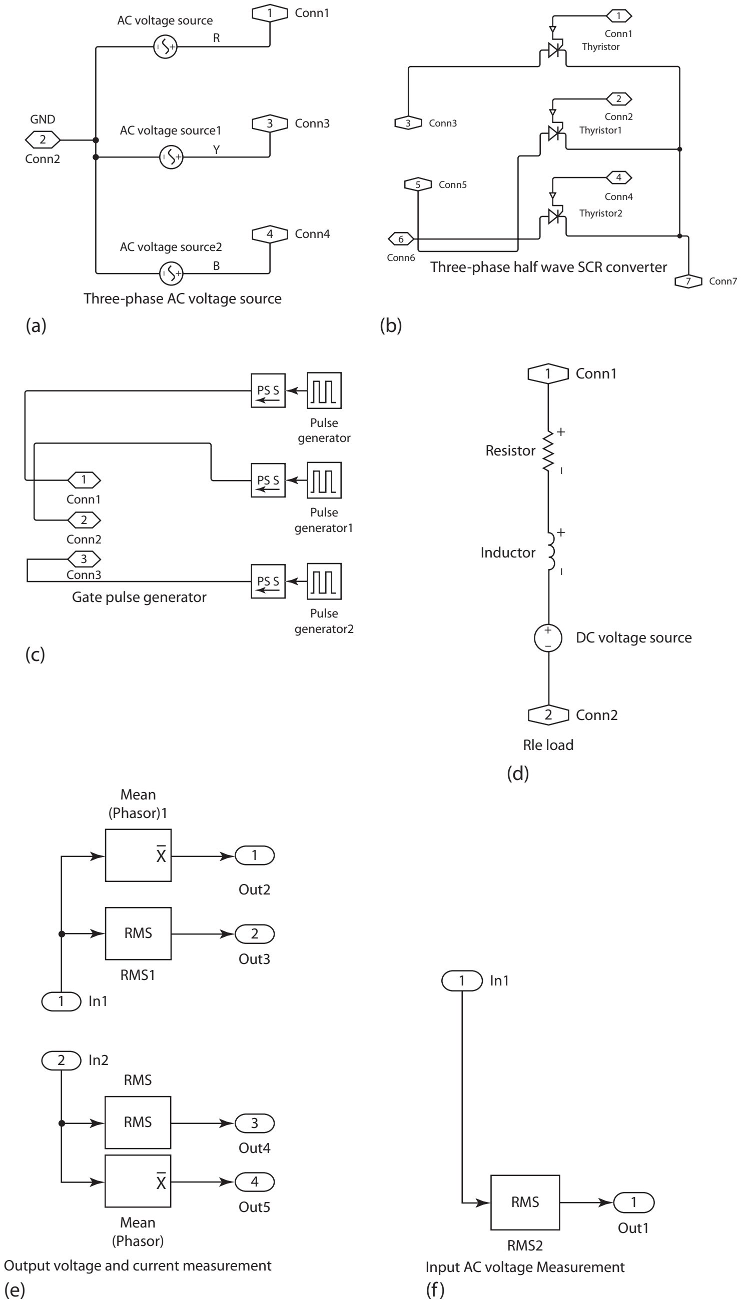
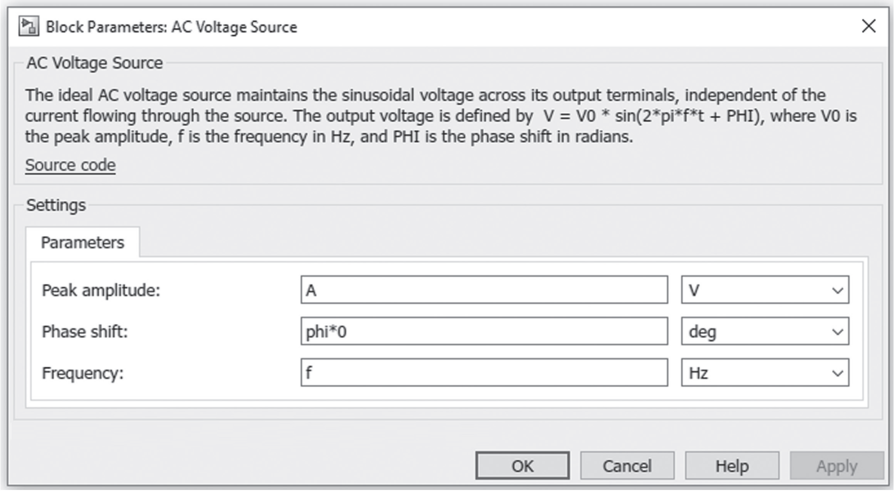

AC voltage source
R
1
Conn1
GND
2
Conn2
AC voltage source1
Y
3
Conn3
AC voltage source2
B
4
Conn4
Three-phase AC voltage source
(a)
1
Conn1
Thyristor
3
Conn3
2
Conn2
Thyristor1
5
Conn5
4
Conn4
Thyristor2
6
Conn6
Three-phase half wave SCR converter
7
Conn7
(b)
PS S
Pulse generator
PS S
Pulse generator1
1
Conn1
2
Conn2
3
Conn3
Gate pulse generator
PS S
Pulse generator2
(c)
1
Conn1
Resistor
Inductor
DC voltage source
2
Conn2
Rle load
(d)
Mean (Phasor)1
X̄
1
Out2
RMS
2
Out3
RMS1
1
In1
2
In2
RMS
RMS
3
Out4
X̄
4
Out5
Mean (Phasor)
Output voltage and current measurement
(e)
1
In1
RMS
1
Out1
RMS2
Input AC voltage Measurement
(f)

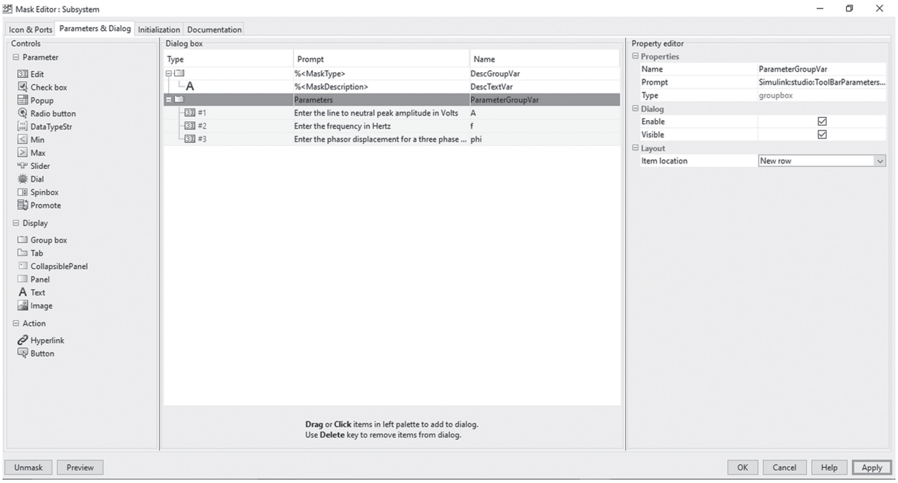
**FIGURE 2.4**
(a) Three-phase AC voltage source. (b) Three-phase half-wave SCR converter. (c) Gate pulse generator. (d) RLE load. (e) Output voltage and current measurement. (f) Input AC voltage measurement.


Block Parameters: AC Voltage Source
AC Voltage Source
Source code
Settings
Parameters
OK
Cancel
Help
Apply

The ideal AC voltage source maintains the sinusoidal voltage across its output terminals, independent of the current flowing through the source. The output voltage is defined by V = V0 * sin(2*pi*f*t + PHI), where V0 is the peak amplitude, f is the frequency in Hz, and PHI is the phase shift in radians.

| | | |
|---|---|---|
| Peak amplitude: | A | V |
| Phase shift: | phi*0 | deg |
| Frequency: | f | Hz |

(a)


Mask Editor : Subsystem
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Controls
Parameter
Edit
Check box
Popup
Radio button
DataTypeStr
Min
Max
Slider
Dial
Spinbox
Promote
Display
Group box
Tab
CollapsiblePanel
Panel
Text
Image
Action
Hyperlink
Button
Dialog box
Property editor
Unmask
Preview
OK
Cancel
Help
Apply

| Type | Prompt | Name |
|---|---|---|
| | %<MaskType> | DescGroupVar |
| A | %<MaskDescription> | DescTextVar |
| | Parameters | ParameterGroupVar |
| #1 | Enter the line to neutral peak amplitude in Volts | A |
| #2 | Enter the frequency in Hertz | f |
| #3 | Enter the phasor displacement for a three phase ... | phi |

**Drag** or **Click** items in left palette to add to dialog.
Use **Delete** key to remove items from dialog.

| | |
|---|---|
| Properties | |
| Name | ParameterGroupVar |
| Prompt | Simulink:studio:ToolBarParameters... |
| Type | groupbox |
| Dialog | |
| Enable | ☑ |
| Visible | ☑ |
| Layout | |
| Item location | New row |

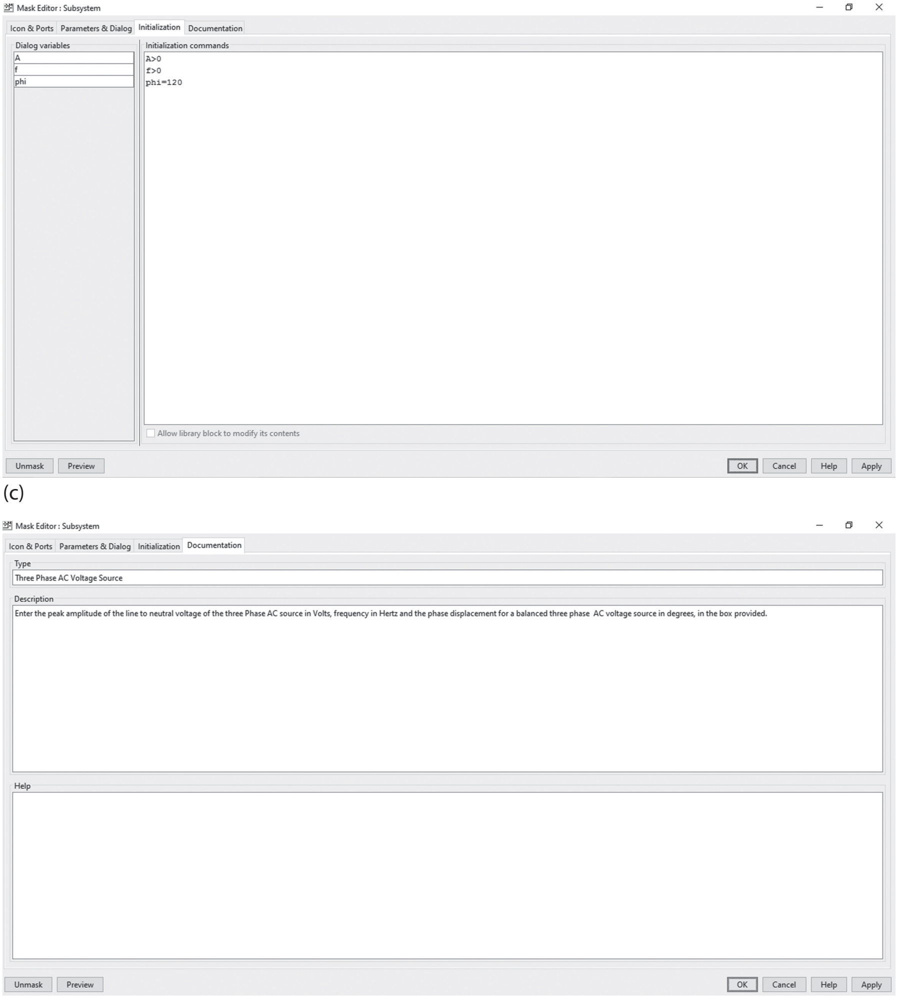
(b)

**FIGURE 2.5**
(a) AC voltage source parameters. (b) ‘Parameters and Dialog’ menu for three-phase AC voltage source.

- *Step 2:* Select the subsystem marked ‘Three-Phase AC Voltage Source’, and then click Diagram → Mask → Create Mask. This opens the Mask Editor.
- *Step 3:* In the Mask Editor, click Parameters and Dialog → Edit.
- *Step 4:* Click or select ‘Parameters’ and enter the instructions to the user.

- *Step 5:* Click or select ‘Parameter Group Var’ and enter the variable name used in the subsystem for the particular parameter.
- *Step 6:* Repeat Steps 4 and 5 until all parameter variable names are entered for the particular subsystem. Then click the ‘Apply’ button.

  A view of the ‘Parameters and Dialog’ menu completed for the ‘Three-Phase AC Voltage Source’ subsystem is shown in Figure 2.5b.
- *Step 7:* Click ‘Initialization’ in the Mask Editor.


Mask Editor : Subsystem
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Dialog variables
Initialization commands
Unmask
Preview
OK
Cancel
Help
Apply

Dialog variables: A, f, phi

Initialization commands:

```
A>0
f>0
phi=120
```

☐ Allow library block to modify its contents

(c)

Mask Editor : Subsystem
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Help
Unmask
Preview
OK
Cancel
Help
Apply

Type: Three Phase AC Voltage Source

Description: Enter the peak amplitude of the line to neutral voltage of the three Phase AC source in Volts, frequency in Hertz and the phase displacement for a balanced three phase AC voltage source in degrees, in the box provided.

(d)

**FIGURE 2.5**
(c) ‘Intialization’ menu for three-phase AC voltage source. (d) ‘Documentation’ menu for three-phase AC voltage source.

- *Step 8:* Ensure all parameter group variables are displayed on the left-hand side.
- *Step 9:* In the 'Initialization commands' box, enter the condition to be satisfied for each parameter variable. This can be a parameter variable greater than zero or lying within a range or above, below or equal to a particular value. Then click the 'Apply' button.
- A view of the 'Initialization' menu completed for the 'Three-Phase AC Voltage Source' subsystem is shown in Figure 2.5c.
- *Step 10:* Click 'Documentation Menu' in the Mask Editor.
- *Step 11:* In the 'Type' box, enter the name of the subsystem.
- *Step 12:* In the 'Description' box, enter the details of the subsystem, the pop-up menu and the value to be entered in each pop-up menu with units.
- *Step 13:* In the 'Help' box, provide any other information relating to the subsystem that the user may need. Clicking the 'Help' button opens up this dialogue box. If there is no other information, the 'Help' box can be left blank. Then click the 'Apply' and 'OK' buttons.

The 'Documentation' menu for the three-phase AC voltage subsystem is shown in Figure 2.5d.

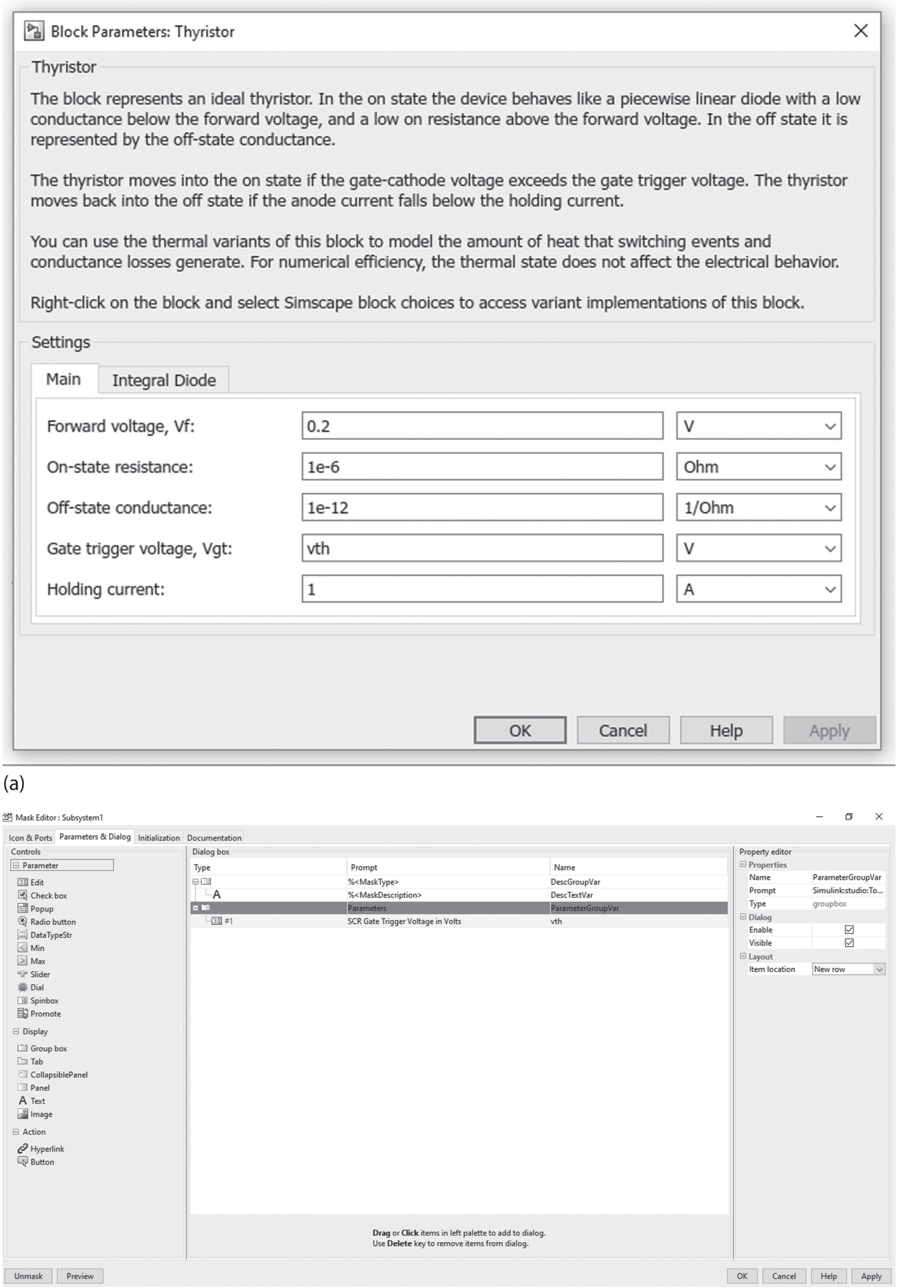
### 2.3.3 SCR Three-Phase Half-Wave Converter

The three-phase half-wave SCR converter subsystem is shown in Figure 2.4b. The dialogue box relating to Thyristor connected to Phase R is shown in Figure 2.6a. Here, only one parameter, which is the gate trigger voltage, is entered as 'vth' in volts. The thyristor will be turned ON only if the gate cathode voltage exceeds this gate trigger voltage 'vth'. For Thyristor1 and Thyristor2 in phases Y and B, the same value, 'vth', is entered for the gate trigger voltage. The following procedure is used to make the SCR three-phase half-wave converter model interactive.

*Step 1:* In Figure 2.2, select the SCRs marked Thyristor, Thyristor1 and Thyristor2 using the mouse pointer. Then, click Diagram → Subsystem and Model Reference → Create Subsystem from Selection to form a subsystem called 'SCR Three-Phase Half-Wave Converter'. Then, follow Steps 2 to 6 in Section 2.3.2. A view of the 'Parameters and Dialog' menu completed for the SCR three-phase half-wave converter subsystem is shown in Figure 2.6b.

Then, follow Steps 7 to 9 in Section 2.3.2 to open and complete the 'Initialization commands' box. The 'Initialization commands' box completed for the SCR three-phase half-wave converter is shown in Figure 2.6c.

Finally, follow Steps 10 to 13 in Section 2.3.2 to complete all the dialogue boxes in the 'Documentation' menu. A view of the 'Documentation' menu completed for the SCR three-phase half-wave converter subsystem is shown in Figure 2.6d.



Block Parameters: Thyristor
Settings
Main
Integral Diode
OK
Cancel
Help
Apply

Thyristor

The block represents an ideal thyristor. In the on state the device behaves like a piecewise linear diode with a low conductance below the forward voltage, and a low on resistance above the forward voltage. In the off state it is represented by the off-state conductance.

The thyristor moves into the on state if the gate-cathode voltage exceeds the gate trigger voltage. The thyristor moves back into the off state if the anode current falls below the holding current.

You can use the thermal variants of this block to model the amount of heat that switching events and conductance losses generate. For numerical efficiency, the thermal state does not affect the electrical behavior.

Right-click on the block and select Simscape block choices to access variant implementations of this block.

| | | |
|---|---|---|
| Forward voltage, Vf: | 0.2 | V |
| On-state resistance: | 1e-6 | Ohm |
| Off-state conductance: | 1e-12 | 1/Ohm |
| Gate trigger voltage, Vgt: | vth | V |
| Holding current: | 1 | A |

(a)

Mask Editor : Subsystem1
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Controls
Parameter
Edit
Check box
Popup
Radio button
DataTypeStr
Min
Max
Slider
Dial
Spinbox
Promote
Display
Group box
Tab
CollapsiblePanel
Panel
Text
Image
Action
Hyperlink
Button
Dialog box
Property editor
Unmask
Preview
OK
Cancel
Help
Apply

| Type | Prompt | Name |
|---|---|---|
| | %<MaskType> | DescGroupVar |
| A | %<MaskDescription> | DescTextVar |
| | Parameters | ParameterGroupVar |
| #1 | SCR Gate Trigger Voltage in Volts | vth |

**Drag** or **Click** items in left palette to add to dialog.
Use **Delete** key to remove items from dialog.

Properties

| | |
|---|---|
| Name | ParameterGroupVar |
| Prompt | Simulink:studio:To... |
| Type | groupbox |

Dialog

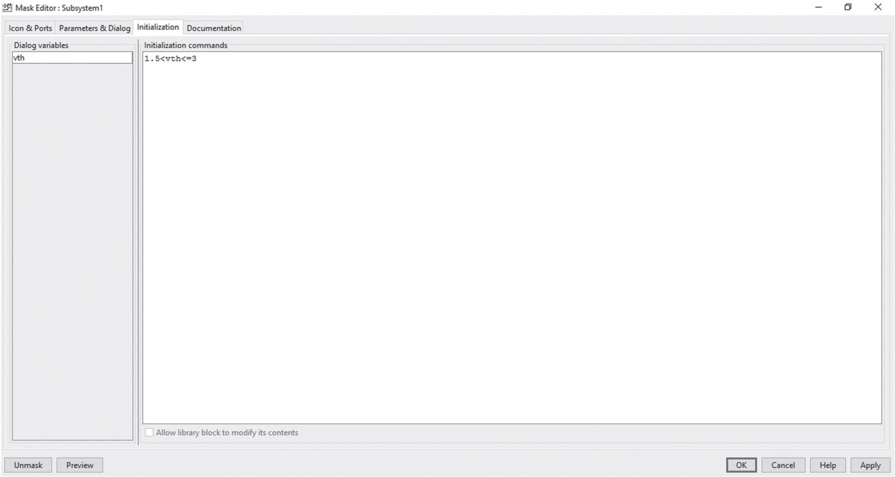
| | |
|---|---|
| Enable | ☑ |
| Visible | ☑ |

Layout

| | |
|---|---|
| Item location | New row |

(b)

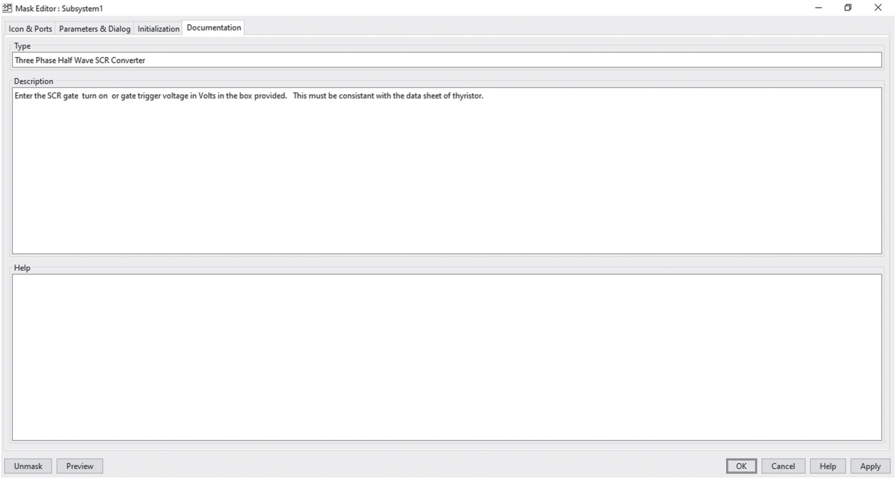
**FIGURE 2.6**
(a) Thyristor parameters. (b) 'Parameters and Dialog' menu for three-phase half-wave SCR converter.


Mask Editor : Subsystem1
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Dialog variables
Initialization commands
Allow library block to modify its contents
Unmask
Preview
OK
Cancel
Help
Apply

vth

```
1.5<vth<=3
```

(c)


Mask Editor : Subsystem1
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Help
Unmask
Preview
OK
Cancel
Help
Apply

Type: Three Phase Half Wave SCR Converter

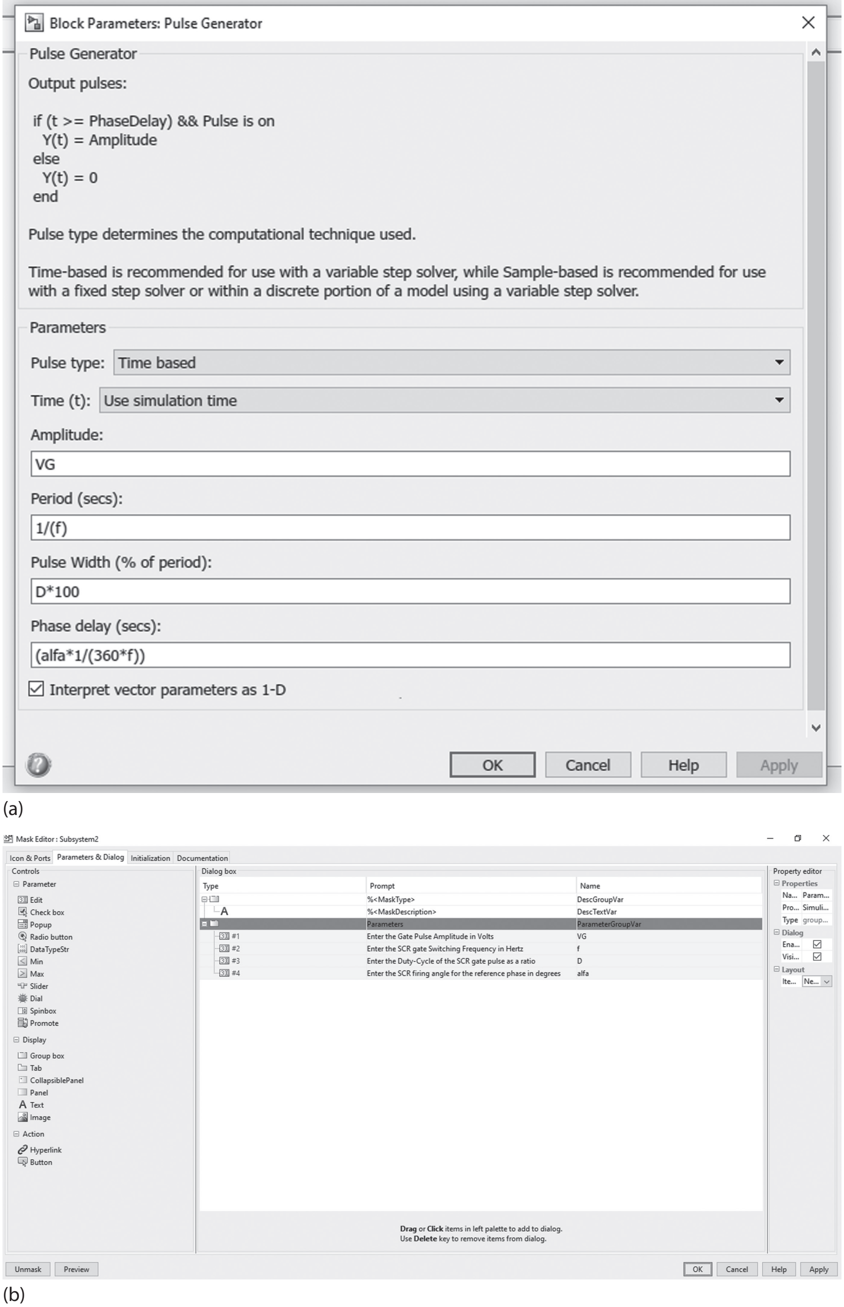
Description: Enter the SCR gate turn on or gate trigger voltage in Volts in the box provided. This must be consistant with the data sheet of thyristor.

(d)

**FIGURE 2.6**
(c) 'Initialization' menu for three-phase half-wave SCR converter. (d) 'Documentation' menu for three-phase half-wave SCR converter.

### 2.3.4 Gate Pulse Generator

The gate pulse generator subsystem is shown in Figure 2.4c. The dialogue box relating to the pulse generator connected to the gate of Thyristor in Phase R is shown in Figure 2.7a. Here, the various parameters are pulse amplitude 'VG' in volts, pulse period 1/(f) in seconds where 'f' is the frequency of the gate pulse in hertz, pulse width or duty cycle as a ratio of the pulse period and phase delay alfa in degrees. In the dialogue box in Figure 2.7a, 'Amplitude' is entered as 'VG' V, 'Period' is entered as 1/(f) s, 'Pulse Width' is



Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: VG

Period (secs): 1/(f)

Pulse Width (% of period): D*100

Phase delay (secs): (alfa*1/(360*f))

☑ Interpret vector parameters as 1-D

OK
Cancel
Help
Apply

(a)

Mask Editor : Subsystem2
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Controls
Parameter
Edit
Check box
Popup
Radio button
DataTypeStr
Min
Max
Slider
Dial
Spinbox
Promote
Display
Group box
Tab
CollapsiblePanel
Panel
Text
Image
Action
Hyperlink
Button
Dialog box

| Type | Prompt | Name |
|---|---|---|
|  | %<MaskType> | DescGroupVar |
| A | %<MaskDescription> | DescTextVar |
|  | Parameters | ParameterGroupVar |
| #1 | Enter the Gate Pulse Amplitude in Volts | VG |
| #2 | Enter the SCR gate Switching Frequency in Hertz | f |
| #3 | Enter the Duty-Cycle of the SCR gate pulse as a ratio | D |
| #4 | Enter the SCR firing angle for the reference phase in degrees | alfa |

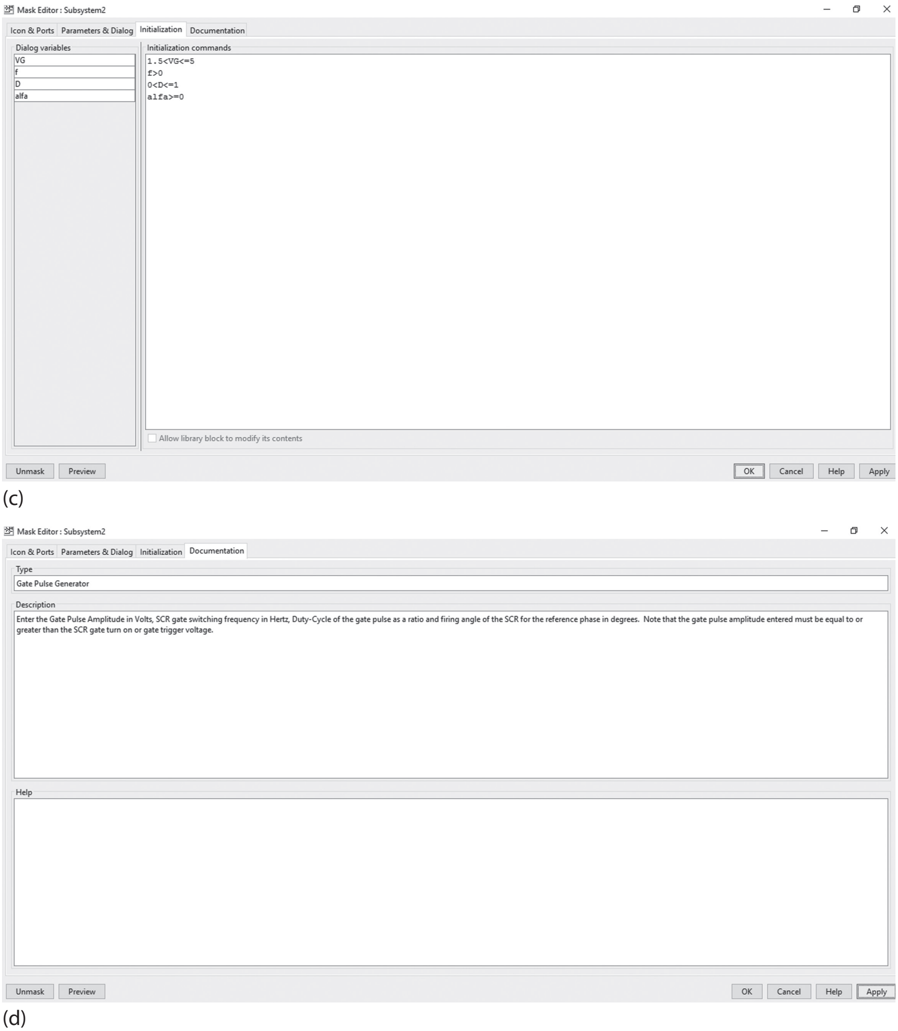
**Drag** or **Click** items in left palette to add to dialog.
Use **Delete** key to remove items from dialog.

Property editor
Properties
Na... Param...
Pro... Simuli...
Type group...
Dialog
Ena... ☑
Visi... ☑
Layout
Ite... Ne...
Unmask
Preview
OK
Cancel
Help
Apply

(b)

**FIGURE 2.7**

(a) Pulse generator parameters. (b) 'Parameters and Dialog' menu for gate pulse generator.


Mask Editor : Subsystem2
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Dialog variables
Initialization commands
Allow library block to modify its contents
Unmask
Preview
OK
Cancel
Help
Apply
(c)
Mask Editor : Subsystem2
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Help
Unmask
Preview
OK
Cancel
Help
Apply
(d)

Dialog variables: VG, f, D, alfa

```
1.5<VG<=5
f>0
0<D<=1
alfa>=0
```

Type: Gate Pulse Generator

Description: Enter the Gate Pulse Amplitude in Volts, SCR gate switching frequency in Hertz, Duty-Cycle of the gate pulse as a ratio and firing angle of the SCR for the reference phase in degrees. Note that the gate pulse amplitude entered must be equal to or greater than the SCR gate turn on or gate trigger voltage.

**FIGURE 2.7**

(c) 'Initialization' menu for gate pulse generator. (d) 'Documentation' menu for gate pulse generator.

entered as 'D*100' and 'Phase delay' is entered as '(alfa*1/(360*f))' s. For Pulse Generator1, connected to the gate of Thyristor1 in Phase Y, the phase delay is entered as '(alfa*1/(360*f) + 1/(3*f))', and for Pulse Generator2, connected to Thyristor2 in Phase B, the phase delay is entered as '(alfa*1/(360*f) + 2/(3*f))', respectively, with all other entries the same as for the pulse generator connected to the gate of Thyristor in Phase R. The following procedure is used to make the gate pulse generator model interactive.

*Step 1:* In Figure 2.2, select the 'Pulse Generator', 'Pulse Generator1' and 'Pulse Generator2' modules using the mouse pointer. Then click Diagram → Subsystem and Model Reference → Create Subsystem from the selection to create a subsystem called 'Gate Pulse Generator'. Then, follow Steps 2 to 6 in Section 2.3.2. A view of the 'Parameters and Dialog' menu completed for the gate pulse generator subsystem is shown in Figure 2.7b.

Then, follow Steps 7 to 9 in Section 2.3.2 to open and complete the 'Initialization commands' box. The 'Initialization commands' box completed for the 'Gate Pulse Generator' subsystem is shown in Figure 2.7c.

Finally, follow Steps 10 to 13 given in Section 2.3.2 to complete all the dialogue boxes in the 'Documentation' menu. A view of the 'Documentation' menu completed for the 'Gate Pulse Generator' subsystem is shown in Figure 2.7d.

### 2.3.5 RLE Load

The RLE load subsystem is shown in Figure 2.4d. This consists of a series-connected resistor, inductor and DC voltage source. The dialogue boxes for the resistor, inductor and DC voltage source are shown in Figure 2.8a–c, respectively. The parameter variable names used for the resistor, inductor and DC voltage source are R1, L1 and E, with units of ohms, henries and volts, respectively.

The following procedure is used to make the RLE load model interactive.

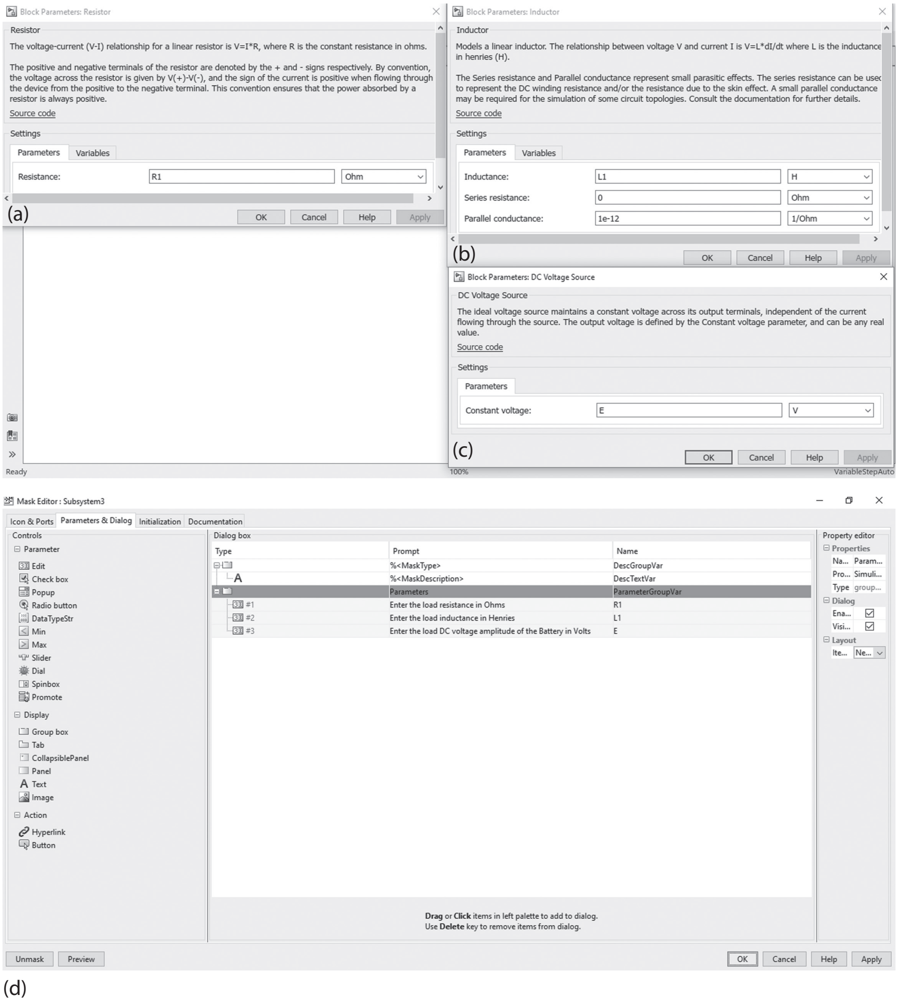
*Step 1:* In Figure 2.2, select the Resistor, Inductor and DC Voltage source modules using the mouse pointer. Then, click Diagram → Subsystem and Model Reference → Create Subsystem from Selection to create a subsystem called 'RLE Load'. Then, follow Steps 2 to 6 in Section 2.3.2. A view of the 'Parameters and Dialog' menu completed for the RLE load subsystem is shown in Figure 2.8d.

Then, follow Steps 7 to 9 in Section 2.3.2 to open and complete the 'Initialization commands' box. The 'Initialization commands' box completed for the RLE load subsystem is shown in Figure 2.8e.

Finally, follow Steps 10 to 13 given in Section 2.3.2 to complete all the dialogue boxes in the 'Documentation' menu. A view of the 'Documentation' menu completed for the RLE load subsystem is shown in Figure 2.8f.

### 2.3.6 Output Voltage and Current Measurement

The output voltage and current measurement subsystem is shown in Figure 2.4e. This consists of separate RMS and MEAN(Phasor) blocks to measure the RMS values and average values of the output voltage and load current. The dialogue box for the RMS and MEAN(Phasor) blocks are shown in Figure 2.9a,b respectively. The parameter used is the output frequency 'f' in hertz, which is three times the input AC voltage frequency for both RMS and average value measurement.


Block Parameters: Resistor
Resistor
Source code
Settings
Parameters
Variables
OK
Cancel
Help
Apply
(a)
Ready
Block Parameters: Inductor
Inductor
(b)
Block Parameters: DC Voltage Source
DC Voltage Source
(c)
100%
VariableStepAuto
Mask Editor : Subsystem3
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Controls
Parameter
Edit
Check box
Popup
Radio button
DataTypeStr
Min
Max
Slider
Dial
Spinbox
Promote
Display
Group box
Tab
CollapsiblePanel
Panel
Text
Image
Action
Hyperlink
Button
Dialog box
Property editor
Properties
Na... Param...
Pro... Simuli...
Type group...
Dialog
Ena... ☑
Visi... ☑
Layout
Ite... Ne...
Unmask
Preview
(d)

The voltage-current (V-I) relationship for a linear resistor is V=I*R, where R is the constant resistance in ohms.

The positive and negative terminals of the resistor are denoted by the + and - signs respectively. By convention, the voltage across the resistor is given by V(+)-V(-), and the sign of the current is positive when flowing through the device from the positive to the negative terminal. This convention ensures that the power absorbed by a resistor is always positive.

Resistance: R1 Ohm

Models a linear inductor. The relationship between voltage V and current I is V=L*dI/dt where L is the inductance in henries (H).

The Series resistance and Parallel conductance represent small parasitic effects. The series resistance can be used to represent the DC winding resistance and/or the resistance due to the skin effect. A small parallel conductance may be required for the simulation of some circuit topologies. Consult the documentation for further details.

Inductance: L1 H

Series resistance: 0 Ohm

Parallel conductance: 1e-12 1/Ohm

The ideal voltage source maintains a constant voltage across its output terminals, independent of the current flowing through the source. The output voltage is defined by the Constant voltage parameter, and can be any real value.

Constant voltage: E V

| Type | Prompt | Name |
|---|---|---|
| | %<MaskType> | DescGroupVar |
| A | %<MaskDescription> | DescTextVar |
| | Parameters | ParameterGroupVar |
| #1 | Enter the load resistance in Ohms | R1 |
| #2 | Enter the load inductance in Henries | L1 |
| #3 | Enter the load DC voltage amplitude of the Battery in Volts | E |

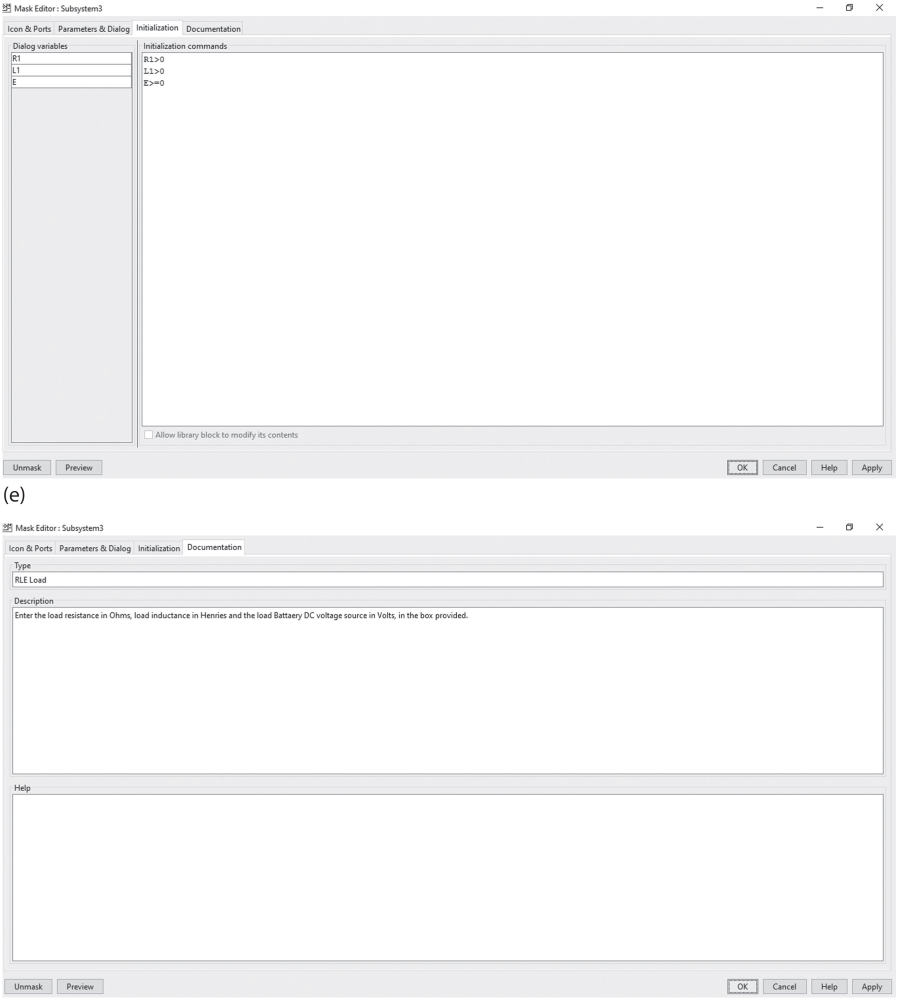
**Drag** or **Click** items in left palette to add to dialog.
Use **Delete** key to remove items from dialog.

**FIGURE 2.8**
(a) Parameters for resistor. (b) Parameters for inductor. (c) Parameters for DC voltage source. (d) 'Parameters and Dialog' menu for RLE load.

The following procedure is used to make the output voltage and current measurement model interactive.

*Step 1:* In Figure 2.2, select the RMS, MEAN(Phasor), RMS1 and MEAN(Phasor)1 modules using the mouse pointer. Then, click Diagram → Subsystem and Model Reference → Create Subsystem from Selection to create a subsystem called 'Output Voltage and Current Measurement'.

Then, follow Steps 2 to 6 in Section 2.3.2. A view of the 'Parameters and Dialog' menu completed for the output voltage and current measurement subsystem is shown in Figure 2.9c.


Mask Editor : Subsystem3
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Dialog variables
Initialization commands
Allow library block to modify its contents
Unmask
Preview
OK
Cancel
Help
Apply

R1
L1
E

```
R1>0
L1>0
E>=0
```

(e)

Type

RLE Load

Description

Enter the load resistance in Ohms, load inductance in Henries and the load Battaery DC voltage source in Volts, in the box provided.

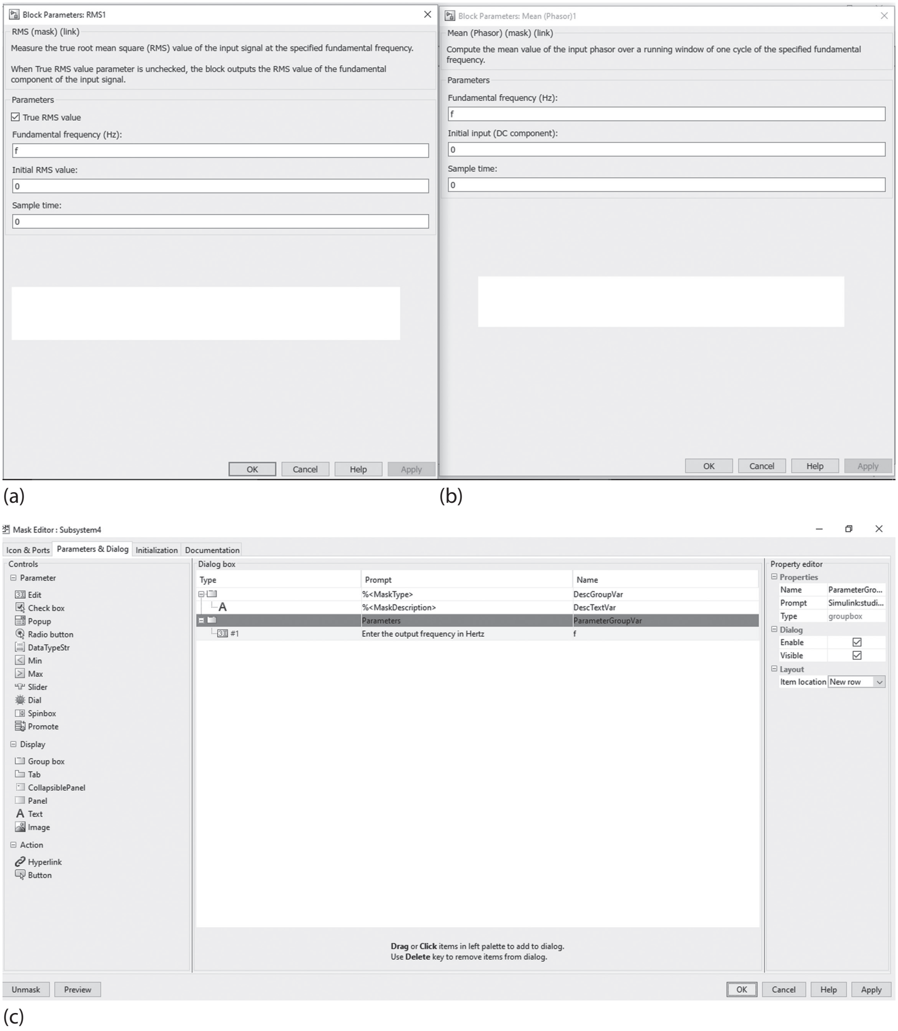
Help

(f)

**FIGURE 2.8**
(e) ‘Intialization’ menu for RLE load. (f) ‘Documentation’ menu for RLE load.

Then, follow Steps 7 to 9 in Section 2.3.2 to open and complete the ‘Initialization commands’ box. The ‘Initialization commands’ box completed for the output voltage and current measurement subsystem is shown in Figure 2.9d.

Finally, follow Steps 10 to 13 given in Section 2.3.2 to complete all the dialogue boxes in the ‘Documentation’ menu. A view of the ‘Documentation’ menu completed for the output voltage and current measurement subsystem is shown in Figure 2.9e.



Block Parameters: RMS1

RMS (mask) (link)

Measure the true root mean square (RMS) value of the input signal at the specified fundamental frequency.

When True RMS value parameter is unchecked, the block outputs the RMS value of the fundamental component of the input signal.

Parameters

☑ True RMS value

Fundamental frequency (Hz): f

Initial RMS value: 0

Sample time: 0

OK
Cancel
Help
Apply

(a)

Block Parameters: Mean (Phasor)1

Mean (Phasor) (mask) (link)

Compute the mean value of the input phasor over a running window of one cycle of the specified fundamental frequency.

Parameters

Fundamental frequency (Hz): f

Initial input (DC component): 0

Sample time: 0

OK
Cancel
Help
Apply

(b)

Mask Editor : Subsystem4

Icon & Ports
Parameters & Dialog
Initialization
Documentation
Controls
Parameter
Edit
Check box
Popup
Radio button
DataTypeStr
Min
Max
Slider
Dial
Spinbox
Promote
Display
Group box
Tab
CollapsiblePanel
Panel
Text
Image
Action
Hyperlink
Button

Dialog box

| Type | Prompt | Name |
|---|---|---|
| | %<MaskType> | DescGroupVar |
| A | %<MaskDescription> | DescTextVar |
| | Parameters | ParameterGroupVar |
| #1 | Enter the output frequency in Hertz | f |

**Drag** or **Click** items in left palette to add to dialog.
Use **Delete** key to remove items from dialog.

Property editor

Properties

Name: ParameterGro...
Prompt: Simulink:studi...
Type: groupbox

Dialog

Enable: ☑
Visible: ☑

Layout

Item location: New row

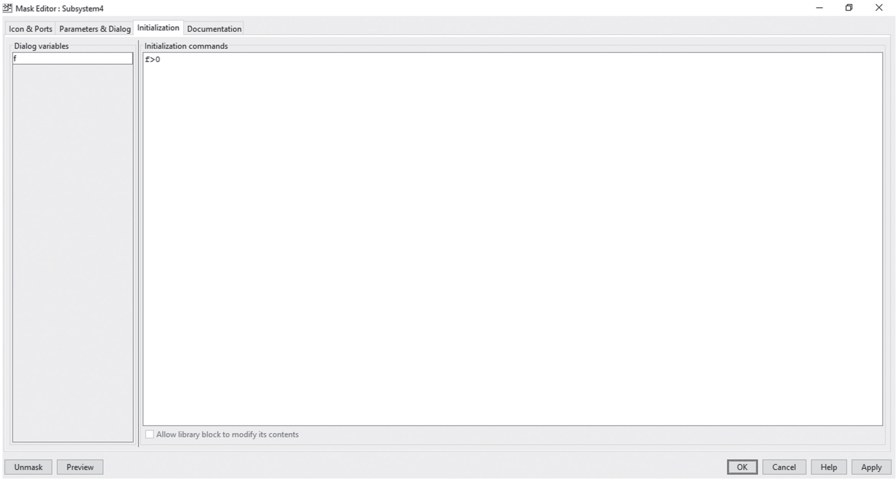
Unmask
Preview
OK
Cancel
Help
Apply

(c)

**FIGURE 2.9**
(a) Parameters for RMS value. (b) Parameters for MEAN(Phasor) value. (c) 'Parameters and Dialog' menu for output voltage and current measurement.

### 2.3.7 Input Voltage Measurement

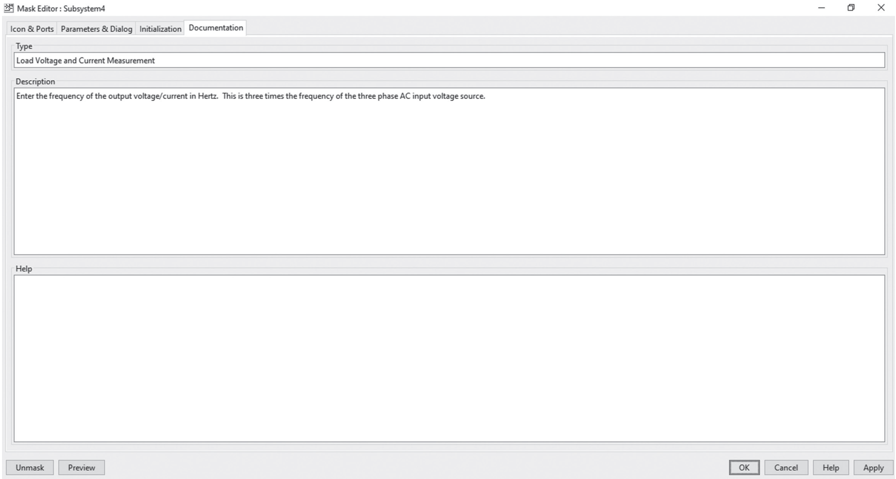
The three-phase AC input voltage line-to-neutral RMS value measurement subsystem is shown in Figure 2.4f. This consists of an RMS line-to-neutral input voltage measurement block called RMS2. The parameter used is the input frequency 'f' in hertz. The dialogue box is the same as shown in Figure 2.9a. The following procedure is used to make the input voltage measurement model interactive.


Mask Editor : Subsystem4
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Dialog variables
Initialization commands
Allow library block to modify its contents
Unmask
Preview
OK
Cancel
Help
Apply

Dialog variables: f

Initialization commands: f>0

(d)


Mask Editor : Subsystem4
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Type
Description
Help
Unmask
Preview
OK
Cancel
Help
Apply

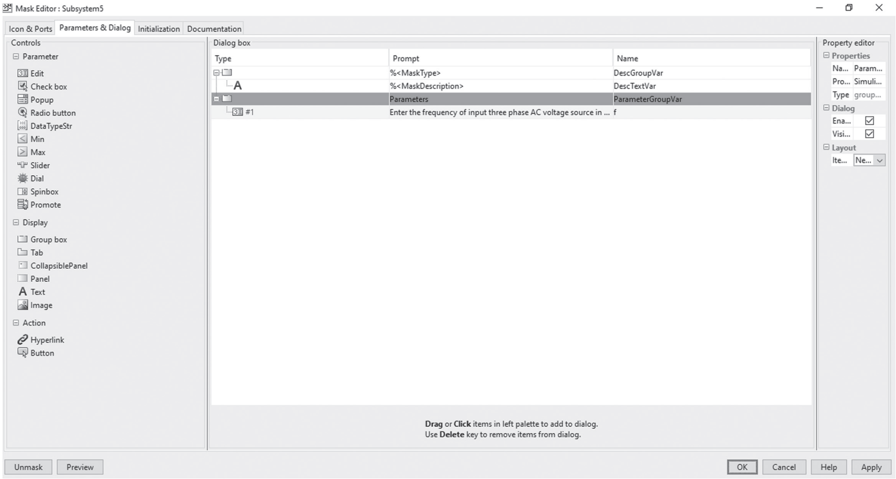
Type: Load Voltage and Current Measurement

Description: Enter the frequency of the output voltage/current in Hertz. This is three times the frequency of the three phase AC input voltage source.

(e)

**FIGURE 2.9**
(d) 'Intialization' menu for output voltage and current measurement. (e) Documentation menu for output voltage and current measurement.

*Step 1:* In Figure 2.2, select the RMS2 module using the mouse pointer. Then click Diagram → Subsystem and Model Reference → Create Subsystem from Selection to create a subsystem called 'Input Voltage Measurement'. Then, follow Steps 2 to 6 in Section 2.3.2. A view of the 'Parameters and Dialog' menu completed for the input voltage measurement subsystem is shown in Figure 2.10a.

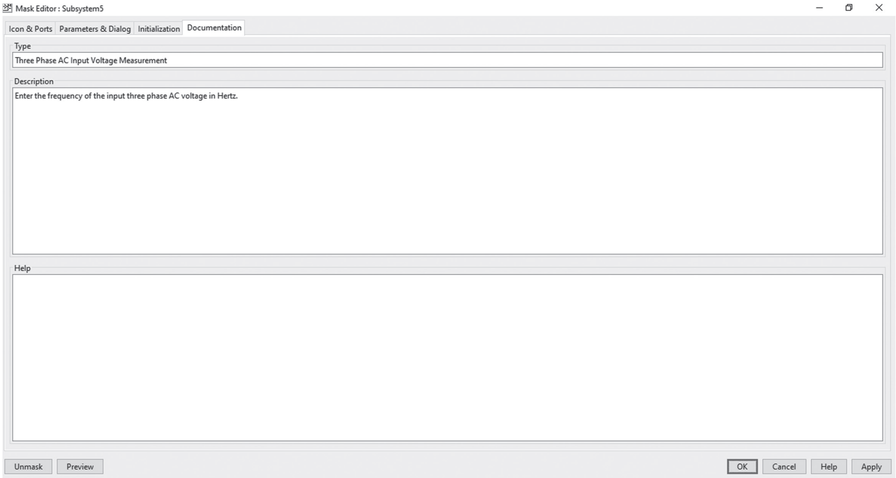

Mask Editor : Subsystem5
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Controls
Parameter
Edit
Check box
Popup
Radio button
DataTypeStr
Min
Max
Slider
Dial
Spinbox
Promote
Display
Group box
Tab
CollapsiblePanel
Panel
Text
Image
Action
Hyperlink
Button
Dialog box
Property editor
Properties
Dialog
Layout
Unmask
Preview
OK
Cancel
Help
Apply

| Type | Prompt | Name |
|---|---|---|
| | %<MaskType> | DescGroupVar |
| A | %<MaskDescription> | DescTextVar |
| | Parameters | ParameterGroupVar |
| #1 | Enter the frequency of input three phase AC voltage source in ... | f |

Na... Param...
Pro... Simuli...
Type group...
Ena... ☑
Visi... ☑
Ite... Ne...

**Drag** or **Click** items in left palette to add to dialog.
Use **Delete** key to remove items from dialog.

(a)


Mask Editor : Subsystem5
Icon & Ports
Parameters & Dialog
Initialization
Documentation
Unmask
Preview
OK
Cancel
Help
Apply

Type
Three Phase AC Input Voltage Measurement

Description
Enter the frequency of the input three phase AC voltage in Hertz.

Help

(e)

**FIGURE 2.10**
(a) 'Parameters and Dialog' menu for input voltage measurement. (b) 'Documentation' menu for input voltage measurement.

Then, follow Steps 7 to 9 in Section 2.3.2 to open and complete the 'Initialization commands' box. The 'Initialization commands' box completed for the input voltage measurement subsystem is the same as shown in Figure 2.9d.

Finally, follow Steps 10 to 13 in Section 2.3.2 to complete all the dialogue boxes in the 'Documentation' menu. A view of the 'Documentation' menu completed for the input voltage measurement subsystem is shown in Figure 2.10b.

## 2.4 Simulation Results

A simulation of the three-phase half-wave SCR converter model shown in Figure 2.2 was carried out for the parameters shown in Table 2.2. The ode23t(stiff trapezoidal) solver is used [1]. The simulation results for the three-phase AC input voltage are shown in Figure 2.11a–c. The load current and output voltage are shown in Figure 2.12a,b. The simulation results are also tabulated in Table 2.3.

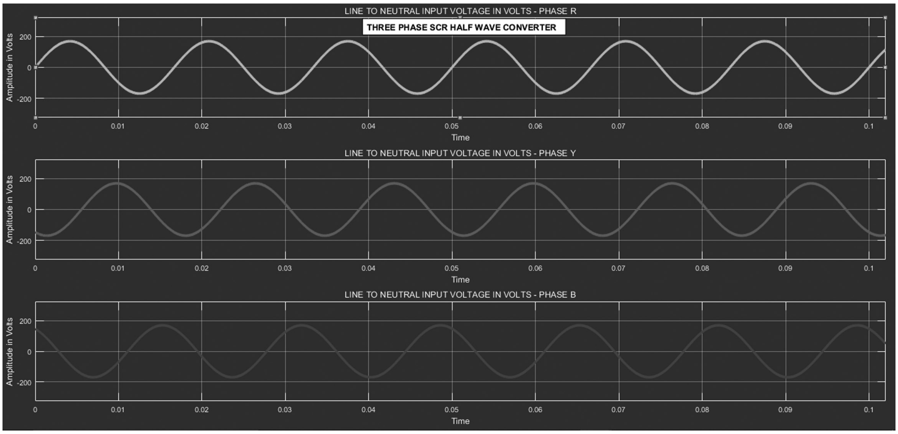


**FIGURE 2.11**
Three-phase half-wave SCR converter. (a) Line-to-neutral input voltage in volts: Phase R. (b) Line-to-neutral input voltage in volts: Phase Y. (c) Line-to-neutral input voltage in volts: Phase B.

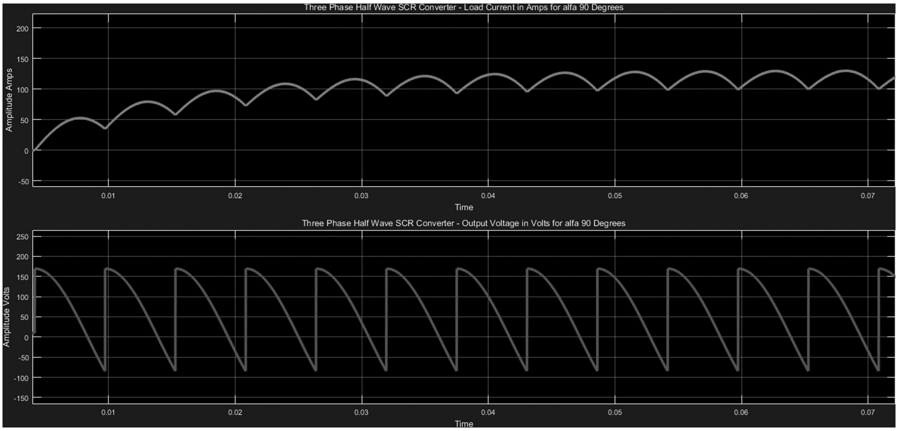


**FIGURE 2.12**
(a) Three-phase half-wave SCR converter: load current in amps for α = 90°. (b) Three-phase half-wave SCR converter: output voltage in volts for α = 90°.

**TABLE 2.3**

Simulation Results for Three-Phase Half-Wave SCR Converter: $\alpha = 90°$

| Sl. No. | RMS Line-to-Neutral Input Voltage (V) | Input Frequency (Hz) | RMS Output Voltage (V) | Average Output Voltage (V) | RMS Load Current (A) | Average Load Current (A) |
|---|---|---|---|---|---|---|
| 1 | 120 | 60 | 106.7 | 69.96 | 120.2 | 119.9 |

## 2.5 Discussion of Results

An interactive model consumes less time compared with a conventional model to simulate and obtain results when there are one or more parameter changes. For example, with a conventional model, if there is a change in the firing angle α, the three pulse generators connected to the gate of the three SCRs have to be opened and the necessary changes in the three dialogue boxes have to be made. This comes to three mouse clicks and three erase and re-enter operations. With an interactive model, it comes to one mouse click and one erase and re-enter operation. Similarly, if there is a change in the input frequency and corresponding thyristor switching frequency, 11 mouse clicks and 11 erase and re-enter operations are required with a conventional model, whereas only four mouse clicks and four erase and re-enter operations are required with an interactive model. For a change in the input line-to-neutral voltage, three mouse clicks and three erase and re-enter operations are required with a conventional model, whereas only one mouse click and one erase and re-enter operation are required with an interactive model. Thus, there is a saving in time, especially when there are a large number of models to be tested for various input parameters. Interactive model development takes more time compared with a conventional model development. But, once an interactive model is developed, the saving in time when testing the model for changes in the input parameters is a definite advantage. If the model topology has one or more capacitors, then variable names starting with C/c, CF/cf, C1/c1, C2/c2 and so on can be given and an interactive model can be developed as for the RLE load subsystem shown in Section 2.3.5.

## 2.6 Conclusions

Interactive modelling capability is a feature available in the Simulink software. The entire model is developed using the electrical block set in the Simscape foundation library and Semiconductor block set in the power systems library. With Simscape and Simulink block set components, S to PS converters and PS to S converters have to be connected. Also, with Simscape components, the Solver Configuration block has to be connected to achieve simulation. The method of developing an interactive model with a three-phase SCR half-wave converter example is presented in this chapter. The method can be easily extended to any power electronic converter topology. With interactive models, the saving in time when testing a power converter for varying parameters is a definite advantage. A virtual power electronics laboratory can be developed with interactive models and, hence, is suitable in an industrial and in a research and development environment.

## References

1. Math Works Inc.: "MATLAB/SIMULINK user guide", R2016b, 2016.
2. M.H. Rashid: *SPICE for Power Electronics and Electric Power*, Boca Raton, FL: CRC Press, 2012, pp. 373–377.

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# 3

# *Interactive Models for AC to DC Converters*

## 3.1 Introduction

In this chapter, the building of interactive models for AC to DC converters, also known as *rectifiers*, is presented. Rectifier circuits can be classified either as half-wave or full-wave bridge rectifiers using semiconductor diodes, or as controlled half-wave or full-wave bridge rectifiers using silicon-controlled rectifiers (SCRs) or thyristors. Modern rectifiers use bipolar junction transistors (BJTs), metal oxide semiconductor field-effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs) and gate turn-off thyristors (GTOs). Here, interactive system models for single-phase full-wave diode bridge rectifiers (FWDBRs), full-wave controlled bridge rectifiers (FWCBRs) using SCRs and three-phase FWDBRs are developed. The switching function concept is used to develop these models. These models have pop-up menus or dialogue boxes where the required data relating to the AC to DC converter are entered by the user. These system models use Simulink® blocks that solve the governing equations relating to the relevant AC to DC converter. No semiconductor circuit component is used in the model.

## 3.2 Single-Phase Full-Wave Diode Bridge Rectifier

The single-phase FWDBR circuit schematic is shown in Figure 3.1 [1–4]. The resistive load or RLE load selection using SS1 is shown for convenience only. Let the applied AC voltage $V_S$ be of the form $V_S = V_m * \sin(\omega.t)$. During the positive half-cycle of $V_S$, diodes D1 and D2 conduct from 0 to π, and during the negative half-cycle, diodes D3 and D4 conduct from π to 2π. The essential derivations of the output voltage are given here for purely resistive load [1].

$$V_{o\_\text{avg}} = \frac{1}{\pi} * \int_0^{\pi} v_m.\sin(\omega.t).d(\omega.t) = \frac{2.V_m}{\pi} \tag{3.1}$$

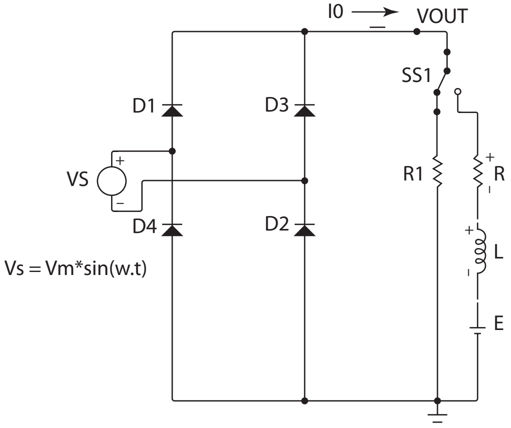


**FIGURE 3.1**
Single-phase FWDBR.

$$I_{o\_\text{avg}} = \frac{V_{o\_\text{avg}}}{R} \tag{3.2}$$

$$V_{o\_\text{rms}} = \sqrt{\frac{1}{\pi} * \left[ \int_0^{\pi} V_m^2 . \sin^2(\omega.t).d(\omega.t) \right]} = \frac{V_m}{\sqrt{2}} \tag{3.3}$$

$$I_{o\_\text{rms}} = \frac{V_{o\_\text{rms}}}{R} \tag{3.4}$$

The output voltage derivations are shown for RLE load [1–4].

$$L.\frac{di_O}{dt} + R.i_O + E = V_m.\sin(\omega.t) \tag{3.5}$$

The solution of Equation 3.5 is given here:

$$i_O = \left[ \frac{V_m}{\left(R^2 + \omega^2.L^2\right)} \right] * \left[ R.\sin(\omega.t) - \omega.L.\cos(\omega.t) + \omega.L.e^{\frac{-R.t}{L}} \right] - \frac{E.e^{\frac{-R.t}{L}}}{R} + \frac{E}{R} \tag{3.6}$$

### 3.2.1 Interactive Model for Single-Phase FWDBR with Purely Resistive or with RLE Load

The system model for the single-phase FWDBR is shown in Figure 3.2 [5]. The purely resistive or RLE load selection is combined in one model. The various dialogue boxes are shown in Figure 3.3, where the user can enter

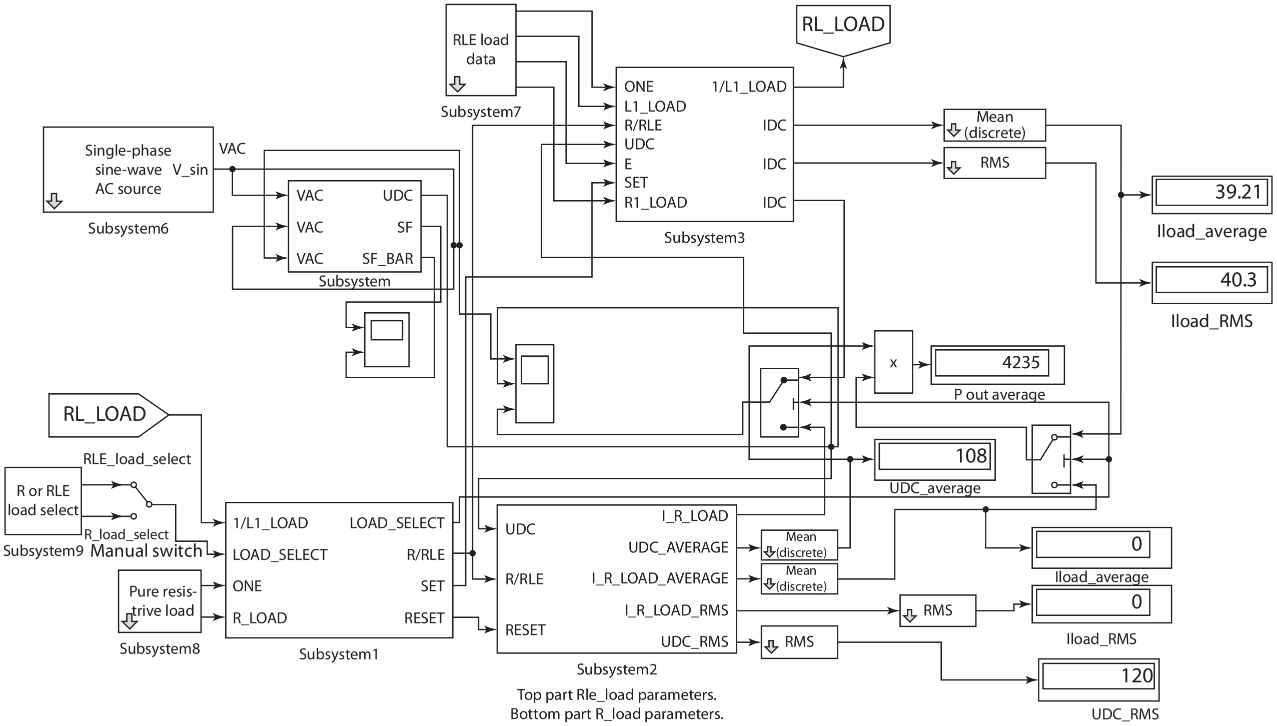
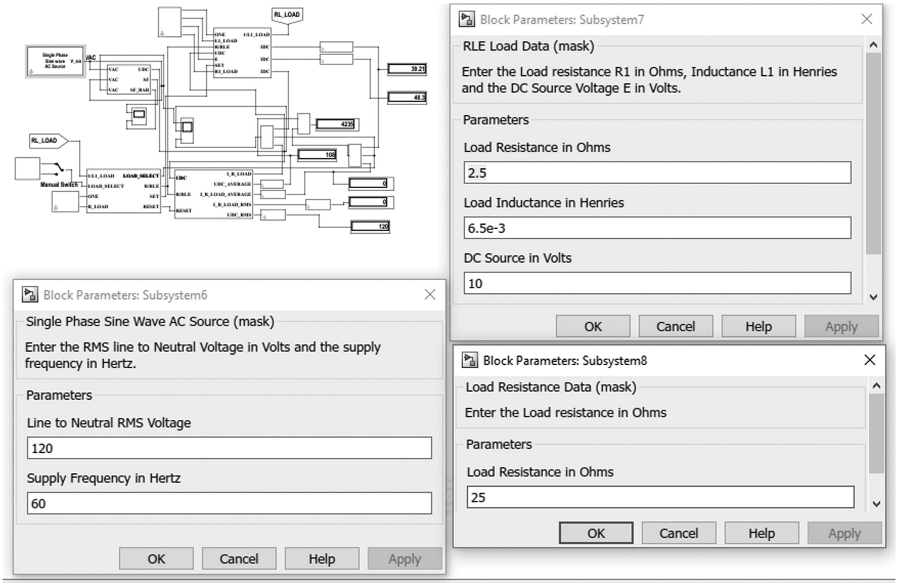

RLE load data
Subsystem7
ONE
L1_LOAD
R/RLE
UDC
E
SET
R1_LOAD
1/L1_LOAD
IDC
IDC
IDC
Subsystem3
RL_LOAD
Mean (discrete)
RMS
39.21
Iload_average
40.3
Iload_RMS
Single-phase sine-wave AC source
V_sin
VAC
Subsystem6
VAC
VAC
VAC
UDC
SF
SF_BAR
Subsystem
x
4235
P out average
108
UDC_average
RL_LOAD
RLE_load_select
R or RLE load select
R_load_select
Subsystem9
Manual switch
1/L1_LOAD
LOAD_SELECT
ONE
R_LOAD
LOAD_SELECT
R/RLE
SET
RESET
Subsystem1
Pure resistive load
Subsystem8
UDC
R/RLE
RESET
I_R_LOAD
UDC_AVERAGE
I_R_LOAD_AVERAGE
I_R_LOAD_RMS
UDC_RMS
Subsystem2
Top part Rle_load parameters.
Bottom part R_load parameters.
Mean (discrete)
Mean (discrete)
RMS
RMS
0
Iload_average
0
Iload_RMS
120
UDC_RMS

**FIGURE 3.2**
Single-phase FWDBR.


Single Phase Sine wave AC Source
V_sin
VAC
VAC
VAC
VAC
UDC
SF
SF_BAR
ONE
L1_LOAD
R/RLE
UDC
E
SET
R1_LOAD
1/L1_LOAD
IDC
IDC
IDC
RL_LOAD
39.21
48.3
4235
108
RL_LOAD
Manual Switch
1/L1_LOAD
LOAD_SELECT
ONE
R_LOAD
LOAD_SELECT
R/RLE
SET
RESET
UDC
R/RLE
RESET
I_R_LOAD
UDC_AVERAGE
I_R_LOAD_AVERAGE
I_R_LOAD_RMS
UDC_RMS
0
0
120
OK
Cancel
Help
Apply
OK
Cancel
Help
Apply
OK
Cancel
Help
Apply

Block Parameters: Subsystem7

RLE Load Data (mask)

Enter the Load resistance R1 in Ohms, Inductance L1 in Henries and the DC Source Voltage E in Volts.

Parameters

Load Resistance in Ohms: 2.5

Load Inductance in Henries: 6.5e-3

DC Source in Volts: 10

Block Parameters: Subsystem6

Single Phase Sine Wave AC Source (mask)

Enter the RMS line to Neutral Voltage in Volts and the supply frequency in Hertz.

Parameters

Line to Neutral RMS Voltage: 120

Supply Frequency in Hertz: 60

Block Parameters: Subsystem8

Load Resistance Data (mask)

Enter the Load resistance in Ohms

Parameters

Load Resistance in Ohms: 25

**FIGURE 3.3**
Single-phase FWDBR with interactive blocks.

the appropriate data required. One model can be used for different system parameters. In Figure 3.2, the selector switch can be double-clicked to select either the purely resistive load or the RLE load option. The value of the line-to-neutral root mean square (RMS) voltage, frequency, the value of RLE loads or that of the purely resistive load used are entered in the appropriate dialogue boxes in Figure 3.3. These values are tabulated in Table 3.1.

The various subsystems of this model are shown in Figure 3.4a–h. These are described as follows.

The single-phase sine-wave AC voltage source in Figure 3.4a is from the 'Sources' block in the 'Simulink' block set. The dialogue box for this is shown in Figure 3.3. The line-to-neutral RMS voltage in volts and the frequency in hertz are entered in this dialogue box. This line-to-neutral RMS voltage and frequency are internally multiplied by 1.414 and 2π, respectively. This

**TABLE 3.1**
Single-Phase FWDBR Parameters

| Sl. No. | Parameter | Value |
|---|---|---|
| 1 | Line-to-neutral RMS voltage | 120 V |
| 2 | Supply frequency | 60 Hz |
| 3 | RLE load | 2.5 Ω, 6.5e−3 H, 10 V |
| 4 | Purely resistive load | 25 Ω |

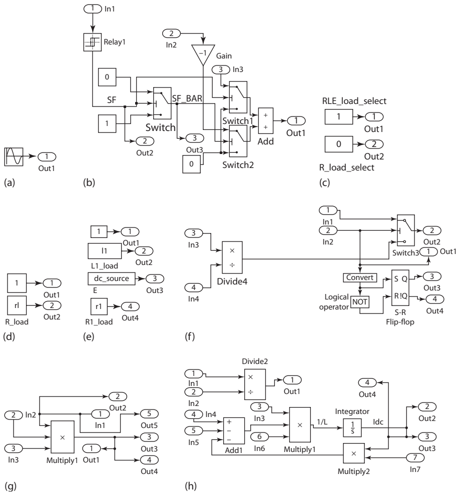

(a)
Out1
(b)
In1
Relay1
In2
Gain
In3
SF
SF_BAR
Switch
Switch1
Switch2
Add
Out1
Out2
Out3
(c)
RLE_load_select
R_load_select
Out1
Out2
(d)
R_load
rl
Out1
Out2
(e)
L1_load
dc_source
E
R1_load
r1
Out1
Out2
Out3
Out4
(f)
In1
In2
In3
In4
Divide4
Switch3
Convert
Logical operator
NOT
S-R Flip-flop
Out1
Out2
Out3
Out4
(g)
In1
In2
In3
Multiply1
Out1
Out2
Out3
Out4
Out5
(h)
Divide2
In1
In2
In3
In4
In5
In6
In7
Add1
Multiply1
Multiply2
1/L
Integrator
Idc
Out1
Out2
Out3
Out4

**FIGURE 3.4**
(a–h) Single-phase FWDBR model subsystems.

sine-wave output is passed to Relay1 in Figure 3.4b. Relay1 is a zero-crossing comparator whose output is the switch function SF, defined in Equation 3.7. The inverse switch function SF_BAR is generated using a switch from the Signal Routing block set, defined in Equation 3.8:

$$\left.\begin{array}{rll} \text{SF} = 1 & \text{for} & 0 \le \omega t \le \pi \\ 0 & \text{for} & \pi \le \omega t \le 2\pi \end{array}\right| \tag{3.7}$$

$$\left.\begin{array}{rll} \text{SF\_BAR} = 0 & \text{for} & 0 \le \omega t \le \pi \\ 1 & \text{for} & 0 \le \omega t \le \pi \end{array}\right| \tag{3.8}$$

The switch generating SF_BAR has 0 and 1 as its first $u(1)$ input and third $u(3)$ input, respectively, while the control or second $u(2)$ input is SF. The switch threshold is 0.5. The switch output is $u(1)$ when input $u(2)$ is greater than or equal to threshold value, else its output is $u(3)$. SF and SF_BAR are passed to the control input $u(2)$ of Switch1 and Switch2, respectively, in Figure 3.4b. The $u(1)$ input to Switch1 is the AC supply voltage $V_S$, while that for Switch2 is the negative of this supply voltage, $-V_S$. The $u(3)$ inputs to Switch1 and Switch2 are both zero. The threshold values for Switch1 and Switch2 are both 0.5. The Switch1 and Switch2 outputs are $+V_S$ and $-V_S$ when their respective $u(2)$ input is greater than or equal to the threshold value, else their outputs are zero. The output of Switch1 and Switch2 are added using the Add block. The output of this Add block is the rectified DC output voltage $U_{dc}$ ($V_{dc}$).

Referring to Figure 3.4b, the output voltage of the sum block $U_{dc}$ can be expressed as follows:

$$\left.\begin{aligned} U_{dc} &= \mathrm{SF}.(V_S) + \mathrm{SF\_BAR}.(-V_S) \\ &= V_S \quad \text{for} \quad 0 \le \omega.t \le \pi \\ &= -V_S \quad \text{for} \quad \pi \le \omega.t \le 2\pi \end{aligned}\right] \tag{3.9}$$

In Equation 3.9, $V_S$ is the sine-wave input voltage.

The type of load select module shown in Figure 3.4c has two constants, 1 and 0, as input to the single pole double throw (SPDT) switch. Double-clicking the SPDT switch in Figure 3.2 selects either the purely resistive load or the RLE load.

Figure 3.4d, e corresponds to the dialogue box for load resistance data and RLE load data, respectively, shown in Figure 3.3.

If the SPDT switch is thrown to 0 in Figure 3.2, then the purely resistive load R_LOAD is selected. Referring to Figure 3.4f, it is seen that the Divide4 block calculates 1/(R_LOAD), which is passed to the $u(3)$ input of Switch3. The 1/(L1_LOAD) input from Figure 3.4h is passed to the $u(1)$ input of Switch3. The control input $u(2)$ for Switch3 is from the SPDT switch connected to the output of Figure 3.4c. The threshold for Switch3 is 0.5, and output is either 1/(L1_LOAD) or 1/(R_LOAD), depending on whether the $u(2)$ input is 1 or 0, respectively. The $u(2)$ input of Switch3 is also connected to the S input and through a NOT gate to the R input of the S–R flip-flop, as shown in Figure 3.4f. If the SPDT switch is thrown to 0 or 1, the S–R flip-flop enables the bottom display or top display, respectively, in Figure 3.2.

With SPDT in the 0 or bottom position, the value 1/(R_LOAD) is selected. In Figure 3.4g, the DC output voltage $U_{dc}$ is multiplied by 1/(R_LOAD) and by RESET, which is 1, using the Multiplier1 block to obtain the DC load current $I_{dc}$.

If the SPDT switch is thrown to 1, then the RLE load in Figure 3.4e is selected. Referring to Figure 3.4h, it is seen that the Divide2 block calculates 1/(L1_LOAD), which is applied to the $u(1)$ input of Switch3 in Figure 3.4f. Referring to Figure 3.4f, the $u(2)$ input of this Switch3 is 1, which is greater than its threshold of 0.5 and selects output 1/(L1_LOAD). This $u(2)$ input also sets the S–R flip-flop and Q is HIGH and enables the top display for the RLE load.

In Figure 3.4h, the Add1, Multiply1, Multiply2 and Integrator blocks solve Equation 3.5 and the resulting output of the Integrator is the DC load current $I_{dc}$ with RLE load. The S–R latch enables the top display in Figure 3.2. The RMS and average value of load voltage $U_{dc}$ and the mean and RMS value of the load current and the average power output are displayed.

### 3.2.2 Simulation Results

A simulation of the model for single-phase FWDBR using the ode23t(mod. stiff/trapezoidal) solver for data given in Table 3.1 for the purely resistive load and the RLE load was conducted. The simulation results for purely resistive load are shown in Figure 3.5a–c and those for RLE load are shown in Figure 3.6a–c. The meter readings observed are tabulated in Table 3.2 for both cases.

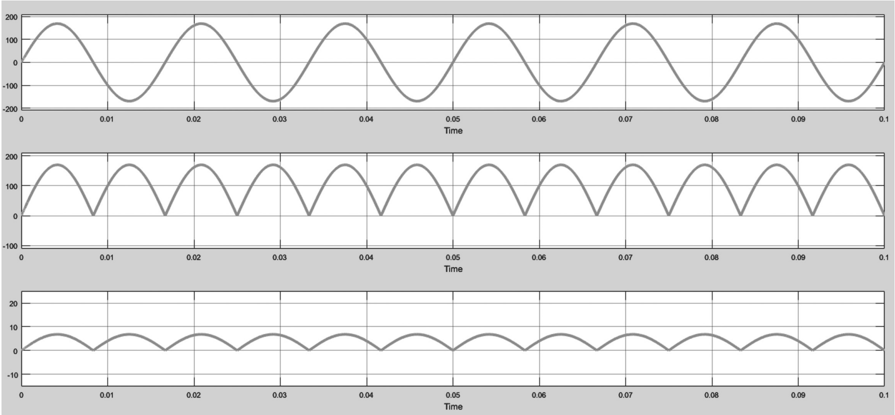


**FIGURE 3.5**
(a) Single-phase FWDBR with purely resistive load-source voltage volts. (b) Output voltage volts. (c) Load current in amps.

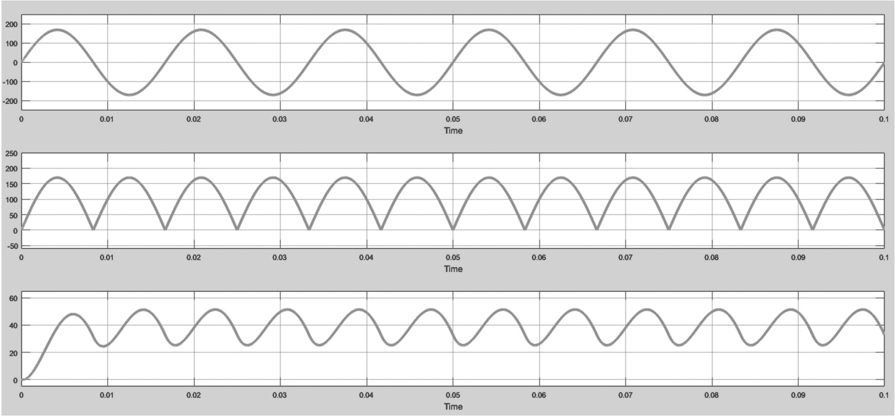


**FIGURE 3.6**
(a) Single-phase FWDBR with RLE load-source voltage volts. (b) Output voltage volts. (c) Load current in amps.

**TABLE 3.2**

Simulation Results for Single-Phase FWDBR

| Sl. No. | Type of Load | Udc(RMS) (V) | Udc(AVG) (V) | I_load(RMS) (A) | I_load(AVG) (A) | P_out (W) |
|---|---|---|---|---|---|---|
| 1 | R only | 120 | 108 | 4.799 | 4.321 | 466.8 |
| 2 | RLE | 120 | 108 | 40.3 | 39.21 | 4235 |

## 3.3 Single-Phase Full-Wave SCR Bridge Rectifier

The single-phase full-wave SCR bridge rectifier is also known as the *single-phase full-wave controlled bridge rectifier* (FWCBR) [1–4]. This is shown in Figure 3.7. Assuming pure resistive load, during the positive half-cycle of $V_S$, thyristors T1 and T2 are fired at an angle α and conduct from α to π. During the negative half-cycle of $V_S$, thyristors T3 and T4 are fired at angle (π + α) and conduct from (π + α) to 2π. Thus, by varying the firing angle α, the average voltage across the load can be varied. The system model for this FWCBR is developed combining the purely resistive load and RLE load in one model. For the RLE load, continuous load current conduction is assumed. In this case, with the RLE load, thyristors T1 and T2 conduct from α to (π + α) when fired at an angle α during the positive half-cycle of $V_S$ and thyristors T3 and T4 conduct from (π + α) to (2π + α), when fired at an angle (π + α) during the negative half-cycle of $V_S$. This model can be used for continuous conduction mode only with RLE load.

The essential derivation for output voltage and load current is shown here for purely resistive load.

$$V_{dc} = \frac{1}{\pi} * \left[ \int_{\alpha}^{\pi} V_m . \sin(\omega . t) . d(\omega . t) . \right] = \frac{V_m}{\pi} * \left[ 1 + \cos(\alpha) \right] \tag{3.10}$$

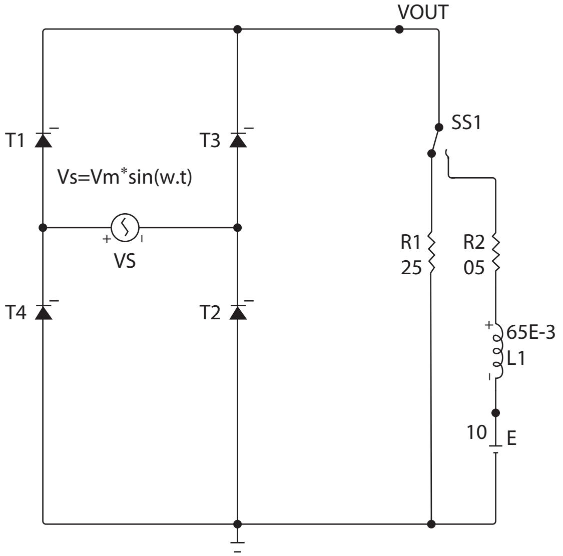


**FIGURE 3.7**
Single-phase full-wave SCR bridge rectifier.

$$V_{\text{rms}} = \sqrt{\frac{1}{\pi} * \left[ \int_{\alpha}^{\pi} V_m^2 . \sin^2(\omega . t) . d(\omega . t) \right]} = \frac{V_m}{\sqrt{2}} * \left[ \sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}} \right] \tag{3.11}$$

$$\text{Average input power } P_{in} = \frac{1}{\pi . R} \left[ \int_{\alpha}^{\pi} \left( V_m . \sin(\omega . t) \right)^2 . d(\omega . t) \right] \tag{3.12}$$

$$= \frac{V_m^2}{2R} * \left[ 1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi} \right] \tag{3.13}$$

The essential derivation for output voltage and load current is shown here for RLE load [1].

$$V_{dc} = \frac{1}{\pi} * \left[ \int_{\alpha}^{\pi+\alpha} V_m . \sin(\omega . t) . d(\omega . t) \right] = \frac{2V_m}{\pi} . \cos(\alpha) \tag{3.14}$$

$$V_{\text{rms}} = \sqrt{\frac{1}{\pi} * \left[ \int_{\alpha}^{\pi+\alpha} V_m^2 . \sin^2(\omega . t) . d(\omega . t) \right]} = \frac{V_m}{\sqrt{2}} \tag{3.15}$$

$$L . \frac{di_L}{dt} + R . i_L + E = V_m . \sin(\omega . t) \quad \text{for} \quad i_L \succ 0 \tag{3.16}$$

The solution gives

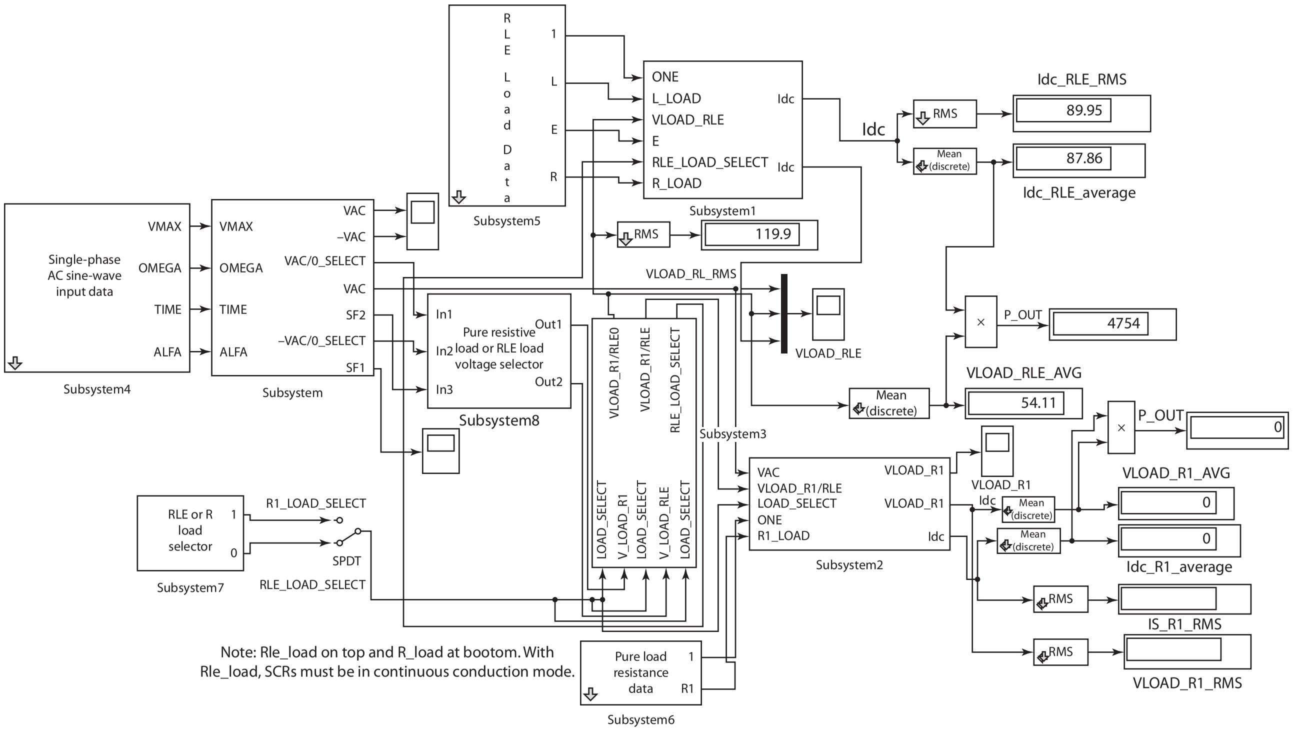
$$i_L = \frac{V_m}{Z} * \sin(\omega . t - \theta) - \frac{E}{R} + \left[ I_{LO} + \frac{E}{R} - \frac{V_m}{Z} * \sin(\alpha - \theta) \right] * e^{(R/L)*(\alpha/\omega - t)} \tag{3.17}$$

where $I_{LO} = I_{LI}$ and $\theta$ are given by

$$\left. \begin{aligned} I_{LO} = I_{L1} = & \frac{V_m - \sin(\alpha - \theta) - \sin(\alpha - \theta) * e^{-(R/L)*(\pi)/\omega}}{Z * \left( 1 - e^{-(R/L)*(\pi/\omega)} \right)} - \frac{E}{R} \quad \text{for } I_{LO} \succ 0 \\ \theta = \tan^{-1} & \left( \frac{\omega * L}{R} \right) \end{aligned} \right| \tag{3.18}$$

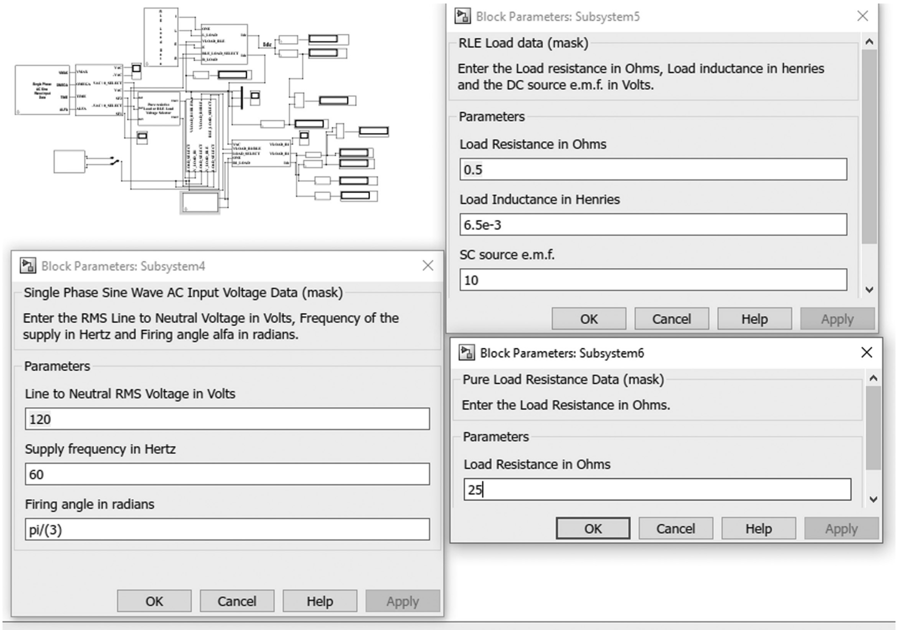
### 3.3.1 Model for Single-Phase FWCBR with Purely Resistive or with RLE Load

The system model for the single-phase FWCBR is shown in Figure 3.8 [5]. The purely resistive or RLE load selection is combined in one model. The various dialogue boxes are shown in Figure 3.9, where the user can enter


Single-phase
AC sine-wave
input data
VMAX
OMEGA
TIME
ALFA
Subsystem4
VMAX
OMEGA
TIME
ALFA
VAC
–VAC
VAC/0_SELECT
VAC
SF2
–VAC/0_SELECT
SF1
Subsystem
RLE Load Data
1
L
E
R
Subsystem5
ONE
L_LOAD
VLOAD_RLE
E
RLE_LOAD_SELECT
R_LOAD
Idc
Idc
Subsystem1
Idc
RMS
89.95
Idc_RLE_RMS
Mean (discrete)
87.86
Idc_RLE_average
RMS
119.9
VLOAD_RL_RMS
VLOAD_RLE
×
P_OUT
4754
Mean (discrete)
54.11
VLOAD_RLE_AVG
In1
In2
In3
Pure resistive load or RLE load voltage selector
Out1
Out2
Subsystem8
VLOAD_R1/RLE0
VLOAD_R1/RLE
RLE_LOAD_SELECT
LOAD_SELECT
V_LOAD_R1
LOAD_SELECT
V_LOAD_RLE
LOAD_SELECT
Subsystem3
VAC
VLOAD_R1/RLE
LOAD_SELECT
ONE
R1_LOAD
VLOAD_R1
VLOAD_R1
Idc
Subsystem2
VLOAD_R1
Idc
×
P_OUT
0
Mean (discrete)
0
VLOAD_R1_AVG
Mean (discrete)
0
Idc_R1_average
RMS
IS_R1_RMS
RMS
VLOAD_R1_RMS
RLE or R load selector
1
0
Subsystem7
R1_LOAD_SELECT
SPDT
RLE_LOAD_SELECT
Pure load resistance data
1
R1
Subsystem6

Note: Rle_load on top and R_load at bootom. With Rle_load, SCRs must be in continuous conduction mode.

**FIGURE 3.8**
Single-phase full-wave SCR bridge rectifier.



Block Parameters: Subsystem5

RLE Load data (mask)

Enter the Load resistance in Ohms, Load inductance in henries and the DC source e.m.f. in Volts.

Parameters

Load Resistance in Ohms: 0.5

Load Inductance in Henries: 6.5e-3

SC source e.m.f.: 10

Block Parameters: Subsystem4

Single Phase Sine Wave AC Input Voltage Data (mask)

Enter the RMS Line to Neutral Voltage in Volts, Frequency of the supply in Hertz and Firing angle alfa in radians.

Parameters

Line to Neutral RMS Voltage in Volts: 120

Supply frequency in Hertz: 60

Firing angle in radians: pi/(3)

Block Parameters: Subsystem6

Pure Load Resistance Data (mask)

Enter the Load Resistance in Ohms.

Parameters

Load Resistance in Ohms: 25

**FIGURE 3.9**
Single-phase full-wave SCR bridge rectifier with interactive blocks.

the appropriate data required. One model can be used for different system parameters. In Figure 3.8, the selector switch can be double-clicked to select either the purely resistive load or the RLE load option. The value of the line-to-neutral RMS voltage, the frequency, the value of RLE loads used and/or that of the purely resistive load used are entered in the appropriate dialogue boxes in Figure 3.9. These values are tabulated in Table 3.3. The various subsystems of this model are shown in Figure 3.10a–i. These are described next.

The blocks in Figure 3.10a, along with the mux and Fcn block in Figure 3.10b, generate the single-phase sine-wave AC input voltage $V_S$. The dialogue box for this is shown in Figure 3.9. The line-to-neutral RMS voltage (in volts), the frequency (in hertz) and the firing angle α are entered in this dialogue box. The line-to-neutral RMS voltage and frequency are internally multiplied by 1.414 and 2π respectively. Another Fcn1 block in Figure 3.10b generates the delayed sine-wave lagging by firing angle α with respect to the input sine wave. This delayed or lagging sine wave is passed to relay, which generates switch function SF1. The sine-wave input voltage $V_S$ from the Fcn block is passed to Relay1, which generates another switch function SF2. The switch functions SF1 and SF2 are defined in Equations 3.19 and 3.20.

$$\mathrm{SF1} = \begin{cases} 1 \quad \text{for} \quad (\alpha) \le \omega.t \le (\pi + \alpha) \\ 0 \quad \text{for} \quad (\pi + \alpha) \le \omega.t \le (2\pi + \alpha) \end{cases} \tag{3.19}$$

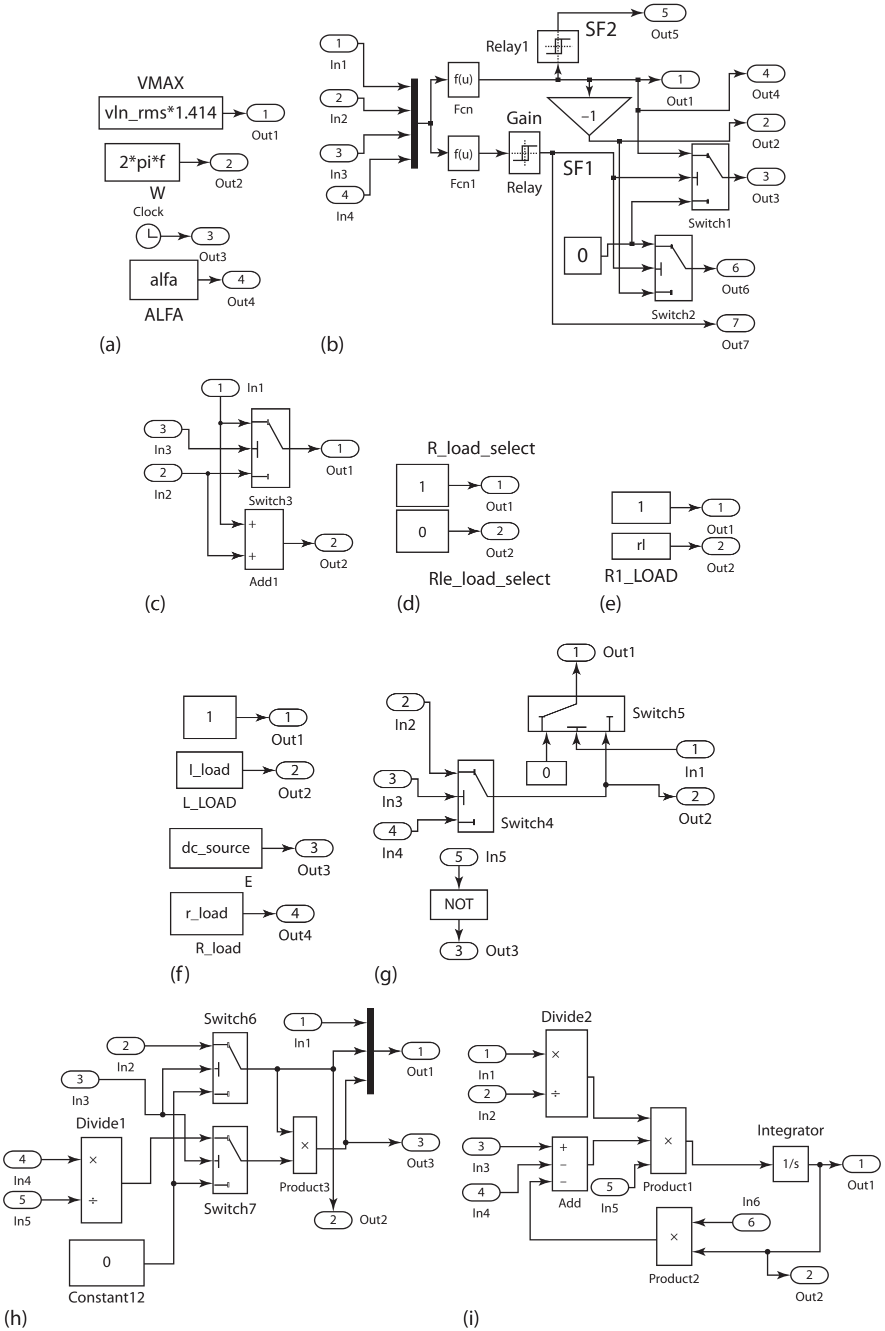

VMAX
vln_rms*1.414
1
Out1
2*pi*f
2
Out2
W
Clock
3
Out3
alfa
4
Out4
ALFA
(a)
1
In1
2
In2
3
In3
4
In4
f(u)
Fcn
f(u)
Fcn1
Gain
Relay
Relay1
SF2
5
Out5
−1
SF1
1
Out1
4
Out4
2
Out2
3
Out3
Switch1
0
6
Out6
Switch2
7
Out7
(b)
1
In1
3
In3
2
In2
Switch3
1
Out1
+
+
Add1
2
Out2
(c)
R_load_select
1
1
Out1
0
2
Out2
Rle_load_select
(d)
1
1
Out1
rl
2
Out2
R1_LOAD
(e)
1
1
Out1
l_load
2
Out2
L_LOAD
dc_source
3
Out3
E
r_load
4
Out4
R_load
(f)
1
Out1
Switch5
2
In2
3
In3
4
In4
Switch4
0
1
In1
2
Out2
5
In5
NOT
3
Out3
(g)
Switch6
2
In2
3
In3
1
In1
1
Out1
Divide1
4
In4
5
In5
×
÷
Switch7
×
Product3
3
Out3
2
Out2
0
Constant12
(h)
Divide2
1
In1
2
In2
×
÷
3
In3
4
In4
+
−
−
Add
5
In5
×
Product1
Integrator
1/s
1
Out1
In6
6
×
Product2
2
Out2
(i)

**FIGURE 3.10**
(a–i) Single-phase FWCBR model subsystems.

$$\mathrm{SF2} = \begin{cases} 1 & \text{for} \quad (0) \le \omega.t \le (\pi) \\ 0 & \text{for} \quad (\pi) \le \omega.t \le (2\pi) \end{cases} \tag{3.20}$$

Both Relay and Relay1 are zero-crossing comparators whose output is HIGH or logic 1 when the respective sine-wave input crosses zero and becomes positive, and their output is LOW or logic 0 when the respective sine-wave input crosses zero and goes negative. Switch1 and Switch2 have *u*(1) input $+V_S$ and 0, *u*(3) input 0 and $-V_S$, respectively, and the *u*(2) input for both is SF1. Both switches have a threshold value of 0.5. Switches 1 and 2 output $+V_S$ and 0 when their respective *u*(2) input is greater than or equal to the threshold value, else their outputs are 0 and $-V_S$, respectively. Referring to the mode of connection of Switch1 and Switch2 in Figure 3.10b, the respective outputs of Switch1 and 2 can be mathematically expressed as follows:

$$\text{Output of Switch1 Out3} = \mathrm{SF1}.V_S \tag{3.21}$$

$$\text{Output of Switch2 Out6} = (1-\mathrm{SF1}).(-V_S) \tag{3.22}$$

Switch1 and 2 output and SF2 are passed to the *u*(1), *u*(3) and *u*(2) input of Switch3, respectively, in Figure 3.10c. The threshold for Switch3 is 0.5 and output Switch1 value if *u*(2) input SF2 is greater than or equal to this threshold value, else output Switch2 value. The output of Switch3 in Figure 3.10c can be expressed mathematically as follows:

$$\text{Output of Switch3 Out1} = \mathrm{SF2}.(\mathrm{SF1}.V_S) + (1-\mathrm{SF2}).(1-\mathrm{SF1}).(-V_S) \tag{3.23}$$

The output of Switch3 can be expressed as follows from Equations 3.19, 3.20 and 3.23:

$$\begin{aligned} \text{Output of Switch3 Out1} &= +V_S \quad \text{for} \quad \alpha \le \omega.t \le \pi \\ &= -V_S \quad \text{for} \quad (\pi+\alpha) \le \omega.t \le 2\pi \end{aligned} \tag{3.24}$$

Equation 3.24 represents the output voltage of single-phase FWCBR with purely resistive load. In Figure 3.10c, the output of the Add1 block can be expressed as follows:

$$\begin{aligned} \text{Output of Add1 block Out2} &= +V_S \quad \text{for} \quad \alpha \le \omega.t \prec (\pi+\alpha) \\ &= -V_S \quad \text{for} \quad (\pi+\alpha) \le \omega.t \le (2\pi+\alpha) \end{aligned} \tag{3.25}$$

Equation 3.25 represents the output voltage of the single-phase FWCBR with RLE load in the *continuous conduction mode.*

The type of load select module shown in Figure 3.10d has two constants, 1 and 0, as input to the SPDT switch. Double-clicking the SPDT switch in Figure 3.8 selects either the purely resistive load or the RLE load.

Figure 3.10e, f corresponds to the dialogue box for pure load resistance data and RLE load data, respectively, shown in Figure 3.9.

If the SPDT switch is thrown to 1, then purely resistive load is selected. The Switch3 and Add1 block output of Figure 3.10c and the SPDT output of Figure 3.10d are applied to the $u(1)$, $u(3)$ and $u(2)$ input of Switch4 in Figure 3.10g. Switch4 has a threshold value of 0.5, and selects the purely resistive load voltage or RLE load voltage as output depending on its $u(2)$ input corresponding to whether the SPDT switch is 1 or 0. This Switch4 output and SPDT output are passed as $u(3)$ and $u(2)$ input to Switch5, whose $u(1)$ input is 0. Switch5 has a threshold value of 0.5 and its output is 0 if its $u(2)$ input corresponding to the SPDT switch is 1, and outputs the Switch4 value when its $u(2)$ input is 0. Thus, the Switch5 output is always the load voltage corresponding to the RLE load. The Switch4 output can be either the purely resistive or the RLE load voltage, depending on the position of the SPDT switch. The SPDT switch output is inverted using a NOT gate to enable selection of the RLE load.

Referring to Figure 3.10h, the Divide1 block calculates 1/(R1_LOAD), which is passed to the $u(1)$ input of Switch7, whose $u(3)$ input is 0, and the $u(2)$ input is from the SPDT switch output. The threshold is 0.5, and Switch7 output is either 1/(R1_LOAD) or 0, depending on whether the $u(2)$ input corresponding to the SPDT switch is 1 or 0. The Switch4 output from Figure 3.10g is passed to the $u(1)$ input of Switch6, whose $u(3)$ input is 0, and the $u(2)$ input is the output of the SPDT switch. The threshold for Switch6 is 0.5, and the output is the purely resistive load voltage or 0, depending on whether the $u(2)$ input corresponding to the SPDT switch output is 1 or 0. The Product3 block multiplies the Switch6 and Switch7 outputs, giving a DC load current with a purely resistive load.

RLE load is selected by throwing SPDT to 0. Referring to Figure 3.10f, g and i, it is seen that Switch4 and Switch5 output the load voltage across the RLE load. The Divide2 block calculates 1/(L_LOAD). The Add block, along with the Divide2, Product1, Product2 and Integrator blocks, solves Equation 3.16 to find the load current through the RLE load. Using the NOT gate in Figure 3.10g connected to the SPDT switch, the upper indicating meters are enabled for the RLE load and the lower indicating meters are enabled for the purely resistive load.

### 3.3.2 Simulation Results

The simulation of the single-phase FWCBR model was developed using the ode23t(mod. stiff/trapezoidal) solver for the data given in Table 3.3, for purely resistive and RLE loads. The simulation results for the purely resistive load are shown in Figure 3.11a–c and those for the RLE load are shown in Figure 3.12a–c. The meter readings observed are tabulated in Table 3.4 for both cases.

**TABLE 3.3**
Single-Phase FWCBR Simulation Parameters

| **Sl. No.** | **Parameter** | **Value** |
|---|---|---|
| 1 | Line-to-neutral RMS voltage | 120 V |
| 2 | Supply frequency | 60 Hz |
| 3 | RLE load | 0.5 Ω, 6.5e−3 H, 10 V |
| 4 | Purely resistive load | 25 Ω |
| 5 | Firing angle α | π/3 rad |

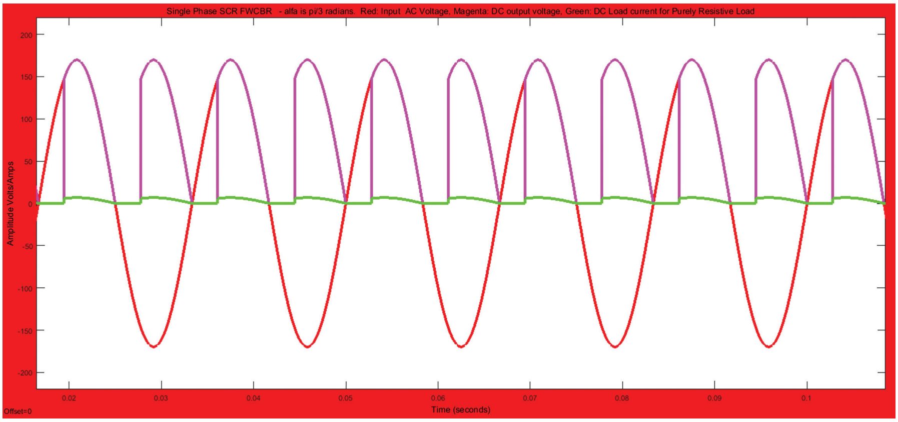


**FIGURE 3.11**
Single-phase FWCBR. Alfa is pi/3 radians. Red, input AC voltage; magenta, DC output voltage; green, DC load current for purely resistive load.

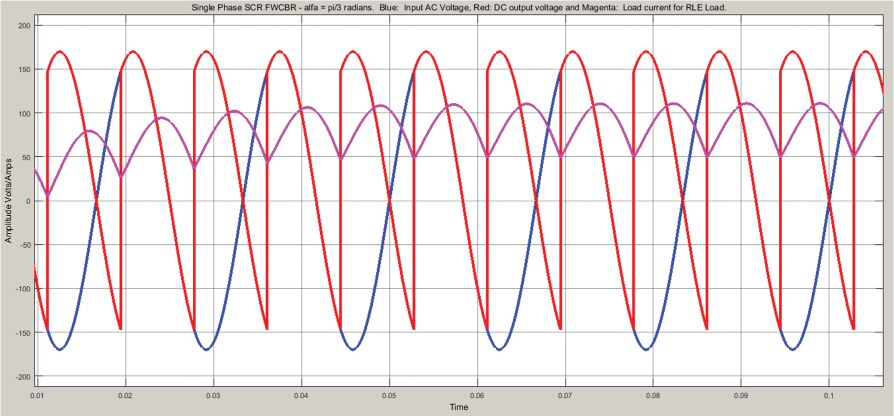


**FIGURE 3.12**
Single-phase FWCBR. Alfa is pi/3 radians. Blue, input AC voltage; red, DC output voltage; magenta, load current for RLE load.

**TABLE 3.4**

Single-Phase FWCBR: Simulation Results for α = π/3 rad

| Sl. No. | Type of Load | Vdc(RMS) (V) | Vdc(AVG) (V) | I_load(RMS) (A) | I_load(AVG) (A) | P_out (W) |
|---|---|---|---|---|---|---|
| 1 | R only | 107.5 | 81.07 | 4.301 | 3.243 | 262.9 |
| 2 | RLE | 120 | 54.11 | 90.06 | 88.01 | 4762 |

## 3.4 Three-Phase Full-Wave Diode Bridge Rectifier

The three-phase FWDBR schematic is shown in Figure 3.13. It is used for high-power applications. The diodes are numbered in conduction sequences and each diode conducts 120°. The conduction sequences for the diodes are: D1–D2, D3–D2, D3–D4, D5–D4, D5–D6, D1–D6, D1–D2 and so on, giving six pulses of ripples at the output voltage. The pair of diodes that are connected between that pair of lines having the highest amount of instantaneous line-to-line voltage will conduct [1–4].

The essential derivation for the purely resistive load is shown here [1–4]:

$$\left.\begin{aligned} V_{an} &= V_m.\sin(\omega t) \\ V_{bn} &= V_m.\sin(\omega t - 120) \\ V_{cn} &= V_m.\sin(\omega t - 240) \end{aligned}\right| \tag{3.26}$$

$$\left.\begin{aligned} V_{ab} &= \sqrt{3}.V_m.\sin(\omega t + 30) \\ V_{bc} &= \sqrt{3}.V_m.\sin(\omega t - 90) \\ V_{ca} &= \sqrt{3}.V_m.\sin(\omega t - 210) \end{aligned}\right| \tag{3.27}$$

The average output voltage $V_{dc}$ is derived as follows [1–4]:

$$\begin{aligned} V_{dc} &= \frac{6}{\pi} * \int_{\pi/6}^{\pi/2} V_m.\sin(\omega.t).d(\omega.t) \\ &= \frac{6}{\pi} * \int_{0}^{\pi/6} \sqrt{3} * V_m.\cos(\omega.t).d(\omega.t) \\ &= \frac{3\sqrt{3}.V_m}{\pi} = 1.654 * V_m \end{aligned} \tag{3.28}$$

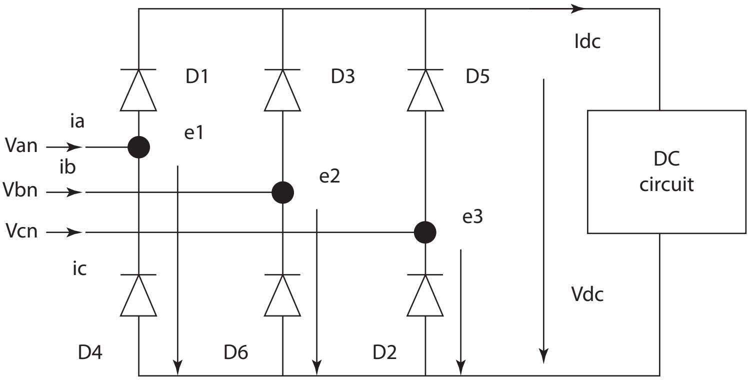


**FIGURE 3.13**
Three-phase FWDBR.

The RMS output voltage $V_{\text{rms}}$ is derived as follows [1–4]:

$$V_{\text{rms}} = \frac{6}{\pi} * \int_{\pi/6}^{\pi/2} V_m^2 * \sin^2(\omega.t).d(\omega.t)$$

$$= \frac{6}{\pi} * \int_{0}^{\pi/6} 3V_m^2 * \cos^2(\omega.t).d(\omega.t) \tag{3.29}$$

$$= V_m * \sqrt{\left[\frac{3}{2} + \frac{9.\sqrt{3}}{4\pi}\right]} = 1.6554 * V_m$$

If the load resistance is purely resistive, the peak or maximum current through the diode is $I_m = \sqrt{3}.V_m/R$, where $R$ is the load resistance. The RMS value of the diode current is derived as follows:

$$I_r = \sqrt{\left[\frac{4}{2\pi} * \int_{0}^{\pi/6} I_m^2 * \cos^2(\omega.t).d(\omega.t)\right]} \tag{3.30}$$

$$= 0.5518 * I_m$$

The RMS value of the supply current or line current is derived as follows:

$$I_S = \sqrt{\left[\frac{8}{2\pi} * \int_{0}^{\pi/6} I_m^2 * \cos^2(\omega.t).d(\omega.t)\right]} \tag{3.31}$$

$$= 0.7804 * I_m$$

where $I_m$ is the peak value of the three-phase line current (in Equations 3.30 and 3.31).

If $L_s$ is the source inductance in each of the three phases and $f$ is the supply frequency, then the average reduction in output voltage due to source or commutating inductances is given as follows [1–4]:

$$V_X = 6.f.L_S.I_{dc} \tag{3.32}$$

where $I_{dc}$ is the load current.

### 3.4.1 Model for Three-Phase FWDBR with Purely Resistive Load

Before describing the subsystems in detail, the development of the system model for the three-phase FWDBR is explained as follows:

The system model for the three-phase FWDBR is developed based on reference [6]. The Heaviside function $gk$ for $k$ = 1, 2, 3, … is defined in Figure 3.14. This Heaviside function determines whether the diode is conducting or in the blocking state [6]. In Figure 3.13, $e1$, $e2$ and $e3$ are the arm voltages and $u1$, $u2$ and $u3$ are the phase voltages. The relations connecting them are given here:

$$e1 = g1 * V_{dc} \tag{3.33}$$

$$e2 = g2 * V_{dc} \tag{3.34}$$

$$e3 = g3 * V_{dc} \tag{3.35}$$

$$u1 = f1 * V_{dc} \tag{3.36}$$

$$u2 = f2 * V_{dc} \tag{3.37}$$

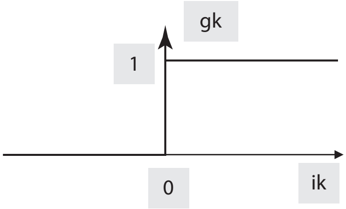


**FIGURE 3.14**
Definition of the $gk$ function ($k$=1,2,3,…).

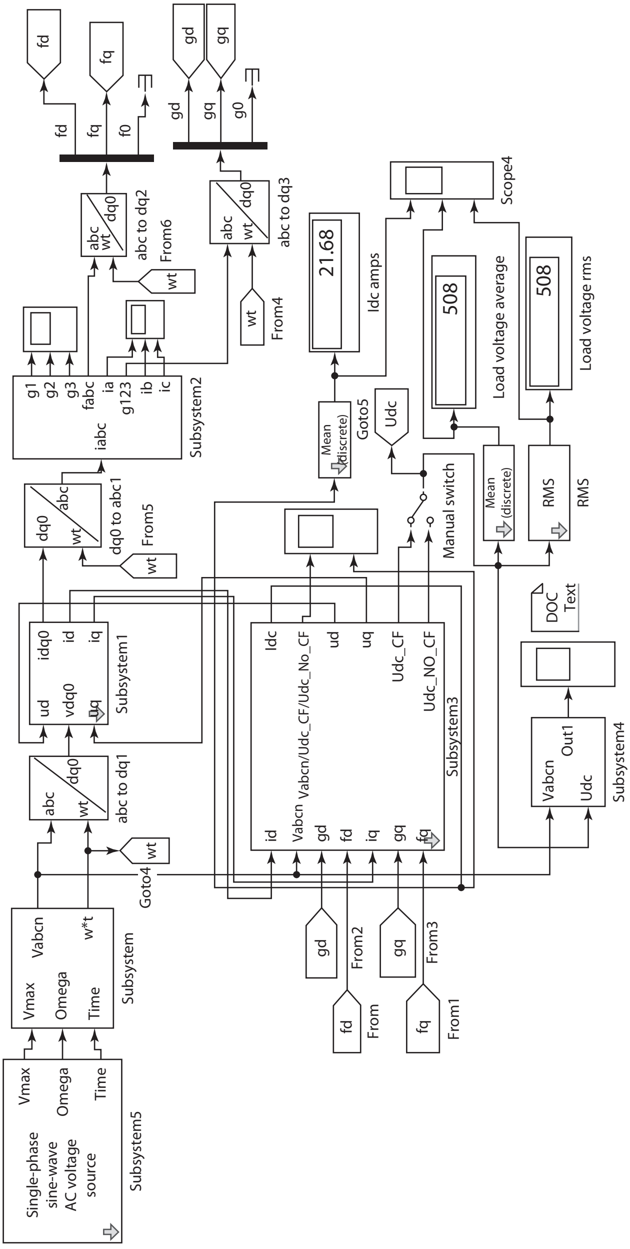

Single-phase sine-wave AC voltage source
Vmax
Omega
Time
Subsystem5
Vmax
Omega
Time
Vabcn
w*t
Subsystem
Goto4
wt
abc
wt
dq0
abc to dq1
ud
vdq0
uq
idq0
id
iq
Subsystem1
dq0
wt
abc
dq0 to abc1
wt
From5
iabc
g1
g2
g3
fabc
ia
g123
ib
ic
Subsystem2
abc
wt
dq0
abc to dq2
wt
From6
fd
fq
f0
fd
fq
abc
wt
dq0
abc to dq3
wt
From4
gd
gq
g0
gd
gq
id
Vabcn
gd
fd
iq
gq
fq
Vabcn/Udc_CF/Udc_No_CF
Idc
Vabcn/Udc_CF/Udc_No_CF
ud
uq
Udc_CF
Udc_NO_CF
Subsystem3
gd
From2
gq
From3
fd
From
fq
From1
Mean (discrete)
Goto5
Udc
21.68
Idc amps
Manual switch
Mean (discrete)
508
Load voltage average
RMS
RMS
508
Load voltage rms
Scope4
DOC Text
Vabcn
Udc
Out1
Subsystem4

**FIGURE 3.15**
Three-phase FWDBR.

$$u3 \ = f3 * V_{dc} \tag{3.38}$$

where functions *f*1, *f*2 and *f*3 are defined as follows:

$$f1 = \frac{2g1 - g2 - g3}{3} \tag{3.39}$$

$$f2 = \frac{2g2 - g3 - g1}{3} \tag{3.40}$$

$$f3 = \frac{2g3 - g1 - g1}{1} \tag{3.41}$$

The DC current is given here:

$$I_{dc} = g1.i1 + g2.i2 + g3.i3$$

If $R_f$ and $L_f$ are the resistance and inductance of each phase of the AC mains, then *e*1, *e*2 and *e*3 are related as follows:

$$e1 = R_f.i_a + L_f.\frac{di_a}{dt} + u1 \tag{3.43}$$

$$e2 = R_f.i_b + L_f.\frac{di_b}{dt} + u2 \tag{3.44}$$

$$e3 = R_f.i_c + L_f.\frac{di_c}{dt} + u3 \tag{3.45}$$

To simplify modelling and procedure, the *abc* to *dq* and *dq* to *abc* transformation is defined as given here:

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ \cos(\theta - 2\pi/3) & \sin(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) & \sin(\theta + 2\pi/3) \end{bmatrix} * \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{3.46}$$

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \end{bmatrix} * \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} \tag{3.47}$$

In Equations 3.46 and 3.47, *x* may be a voltage, current or Heaviside function. The *dq* axis voltages and load current $I_{dc}$ are defined as follows:

$$I_{dc} = gd.id + gq.iq \tag{3.48}$$

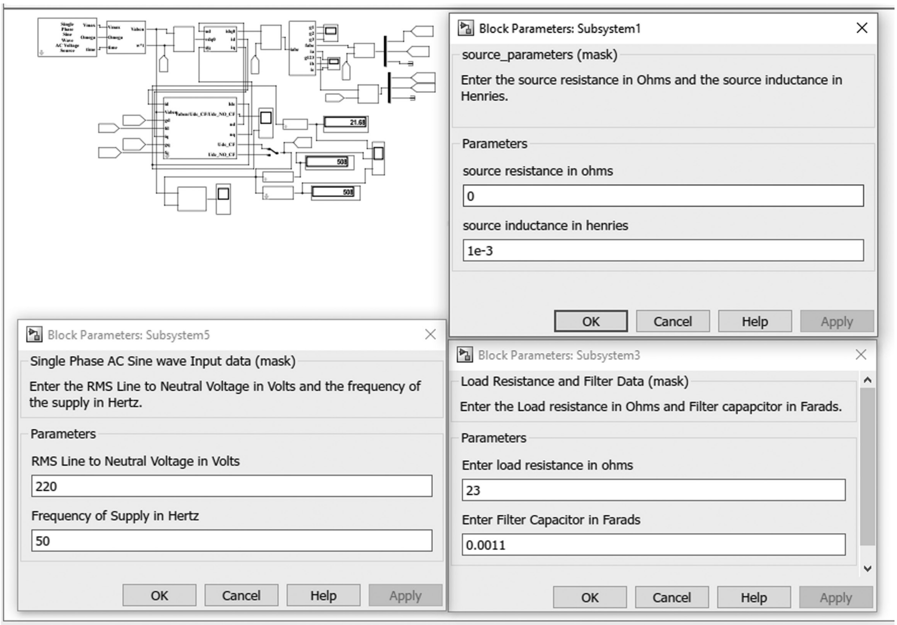
$$v_d = R_f.id + L_f.\frac{did}{dt} + ud \tag{3.49}$$

$$v_q = R_f.iq + L_f.\frac{diq}{dt} + uq \tag{3.50}$$

Equations 3.33 to 3.50 are used to develop the system model for the three-phase FWDBR.

The system model for the three-phase FWDBR is shown in Figure 3.15 [5, 6]. The various user dialogue boxes are shown in Figure 3.16. The user can enter the required data in the appropriate dialogue box. This model is suitable only for the purely resistive load. The various subsystems are shown in Figure 3.17a–f and are described as follows.

Figure 3.17a corresponds to the dialogue box in Figure 3.15, where the line-to-neutral RMS voltage in volts and frequency in hertz are entered. Figure 3.17b generates three-phase AC using the three-input mux and the three Fcn blocks. The *abc* to *dq*0 and *dq*0 to *abc* blocks are from the Power Systems Transformations block set, which is used for the axis transformation



Block Parameters: Subsystem1

source_parameters (mask)

Enter the source resistance in Ohms and the source inductance in Henries.

Parameters

source resistance in ohms: 0

source inductance in henries: 1e-3

Block Parameters: Subsystem5

Single Phase AC Sine wave Input data (mask)

Enter the RMS Line to Neutral Voltage in Volts and the frequency of the supply in Hertz.

Parameters

RMS Line to Neutral Voltage in Volts: 220

Frequency of Supply in Hertz: 50

Block Parameters: Subsystem3

Load Resistance and Filter Data (mask)

Enter the Load resistance in Ohms and Filter capapcitor in Farads.

Parameters

Enter load resistance in ohms: 23

Enter Filter Capacitor in Farads: 0.0011

**FIGURE 3.16**
Three-phase FWDBR with interactive blocks.

of voltage, current and Heaviside functions *gk* and *fk*. Figure 3.17c solves the equation for the *dq* axis line currents given by Equations 3.49 and 3.50. In Figure 3.17c, *rs* and *ls* represent the AC line resistance and inductance in each phase, corresponding to $R_f$ and $L_f$ in Equations 3.49 and 3.50. Figure 3.17c opens up the source parameters dialogue box shown in Figure 3.16. The *dq* axis line current is transformed to the *abc* axis line currents using the *dq*0 to *abc* block. Figure 3.17d has the *abc* axis line currents as inputs and generates the Heaviside functions *g*1, *g*2 and *g*3 for the three phases as defined in

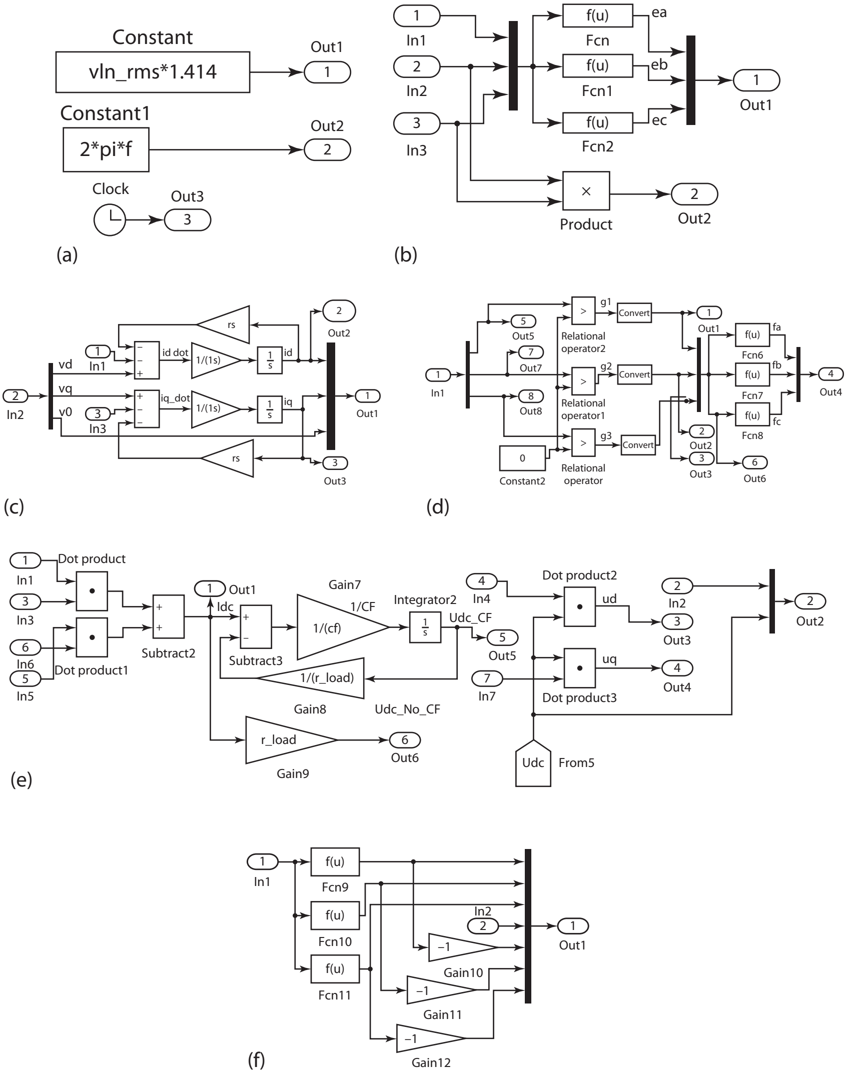

Constant
vln_rms*1.414
Out1
1
Constant1
2*pi*f
Out2
2
Clock
Out3
3
(a)
1
In1
2
In2
3
In3
f(u)
Fcn
f(u)
Fcn1
f(u)
Fcn2
ea
eb
ec
1
Out1
×
Product
2
Out2
(b)
2
In2
vd
vq
v0
1
In1
3
In3
id dot
iq_dot
1/(1s)
1/(1s)
1/s
1/s
id
iq
rs
rs
2
Out2
1
Out1
3
Out3
(c)
1
In1
5
Out5
7
Out7
8
Out8
0
Constant2
>
Relational operator2
Relational operator1
Relational operator
g1
g2
g3
Convert
Convert
Convert
1
Out1
2
Out2
3
Out3
f(u)
Fcn6
f(u)
Fcn7
f(u)
Fcn8
fa
fb
fc
4
Out4
6
Out6
(d)
1
In1
3
In3
6
In6
5
In5
Dot product
Dot product1
Subtract2
1
Out1
Idc
Subtract3
Gain7
1/CF
1/(cf)
Integrator2
1/s
Udc_CF
5
Out5
1/(r_load)
Gain8
Udc_No_CF
r_load
Gain9
6
Out6
4
In4
Dot product2
ud
7
In7
Dot product3
uq
2
In2
3
Out3
4
Out4
2
Out2
Udc
From5
(e)
1
In1
f(u)
Fcn9
f(u)
Fcn10
f(u)
Fcn11
In2
2
−1
Gain10
−1
Gain11
−1
Gain12
1
Out1
(f)

**FIGURE 3.17**
Three-phase FWDBR model subsystems.

Figure 3.14, and then using $g1$, $g2$ and $g3$, the functions $fa$, $fb$ and $fc$ are generated as defined by Equations 3.39 to 3.41, where $f1$, $f2$ and $f3$ correspond to $fa$, $fb$ and $fc$. Heaviside functions $g1$, $g2$, $g3$ and $f1$, $f2$, $f3$ are transformed to their corresponding $dq$ axis equivalent using $abc$ to $dq0$ blocks as shown in Figure 3.15. Figure 3.17e opens the 'Load Resistance and Filter Data' dialogue box, which is shown in Figure 3.16. In Figure 3.17e, load current $I_{dc}$ is calculated using Equation 3.48 using inputs $id$, $gd$, $iq$, $gq$, two dot product multipliers and an Add block.

This value of $I_{dc}$ is used to calculate $I_{dc} * R$ using the Gain9 block to find the load voltage $V_{dc}$(Udc_NO_CF) without filter, where $R$ is the load resistance. With the capacitor filter $C_F$ in parallel to the load resistance, $V_{dc}$(Udc_CF) is calculated by calculating the capacitor filter current $I_C$ as follows:

$$\left.\begin{aligned} I_C &= I_{dc} - \left(V_{dc} / R\right) \\ V_{dc} &= \frac{1}{C_F}\int I_C.dt \end{aligned}\right] \tag{3.51}$$

Equation 3.51 is solved using the Subtract3, Gain7, Gain8 and Integrator2 modules in Figure 3.17e. Further, Figure 3.17e is used to find the $dq0$ axis phase voltages $ud$ and $uq$ using $V_{dc}$(Udc) and $fd$, $fq$ as inputs and two dot product multiplier blocks. Figure 3.17f is used to find the three line-to-line voltages and their inverted values using three Fcn blocks and three gain blocks.

In Figure 3.15, the DC output voltage $U_{dc}$ can be selected with or without the capacitor filter by using the SPDT marked Manual Switch.

The values of the RMS line-to-neutral voltage in volts, frequency in hertz, source resistance in ohms, source inductance in henries, load resistance in ohms and filter capacitor in farads are entered in the appropriate dialogue box in Figure 3.16. These values are shown in Table 3.5 [6].

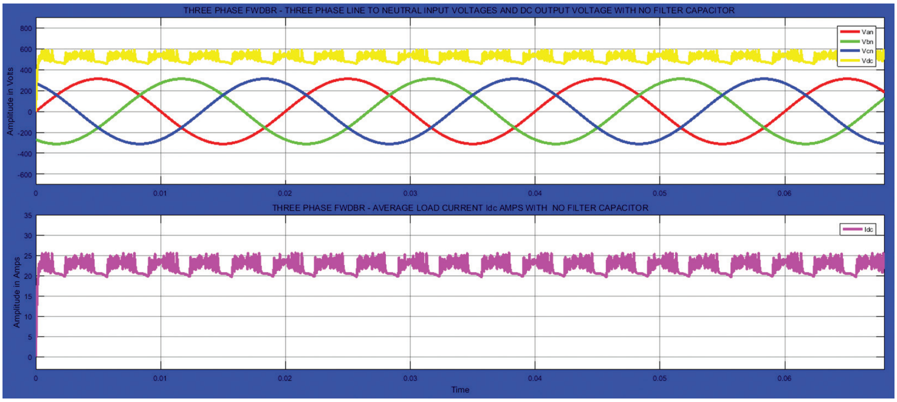


**FIGURE 3.18**
Three-phase FWDBR. (a–d) Three-phase line-to-neutral input voltages and DC output voltage with no filter capacitor. (e) Average load current Idc amps with no filter capacitor.

**TABLE 3.5**

Three-Phase FWDBR: Parameters

| Sl. No | Parameters | Value |
|---|---|---|
| 1 | Line-to-neutral RMS voltage | 220 V |
| 2 | Supply frequency | 50 Hz |
| 3 | Source resistance | 0 Ω |
| 4 | Source inductance | 1e–3 H |
| 5 | Load resistance | 23 Ω |
| 6 | Filter capacitance | 0.0011 F |

### 3.4.2 Simulation Results

The simulation of the three-phase FWDBR was carried out using the ode1(Euler) fixed-step solver for the purely resistive load, first by excluding the filter capacitor from the circuit and then by including the filter capacitor, for the data shown in Table 3.5. The simulation results of input voltage, output voltage and average load current excluding the filter capacitor from the circuit are shown in Figure 3.18a–e and Figure 3.19a–g. The simulation results for these including the filter capacitor are shown in Figure 3.20a–e and Figure 3.21a–g. The values of the RMS, average load voltage and average load current observed for both cases by simulation are recorded in Table 3.6. The average and RMS value of load voltage by calculation using Equations 3.28 and 3.29 yield 514.5 and 515 V respectively. The reduction in the output voltage due to source inductance of 1 mH was calculated using Equation 3.32 and the net value of the output voltage was found to be 507.9 V. The average load current calculated using the formula comes to 22.37 A. The respective

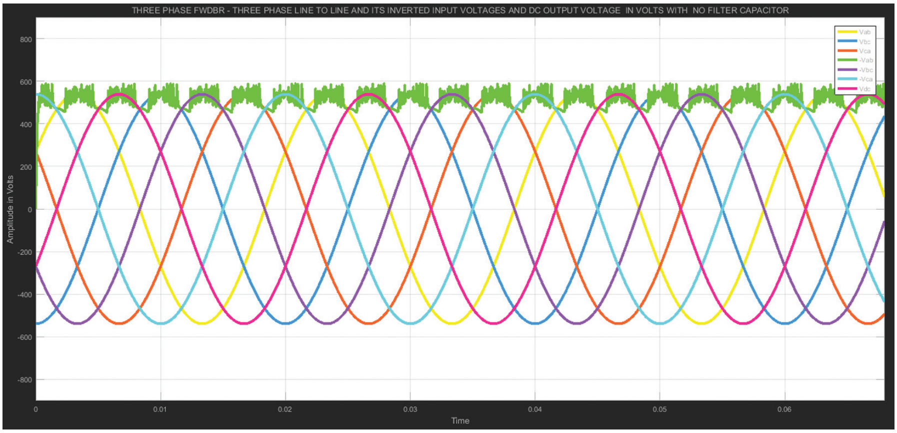


**FIGURE 3.19**

Three-phase FWDBR. Three-phase line to line and its inverted input voltages and DC output voltage in volts with no filter capacitor.

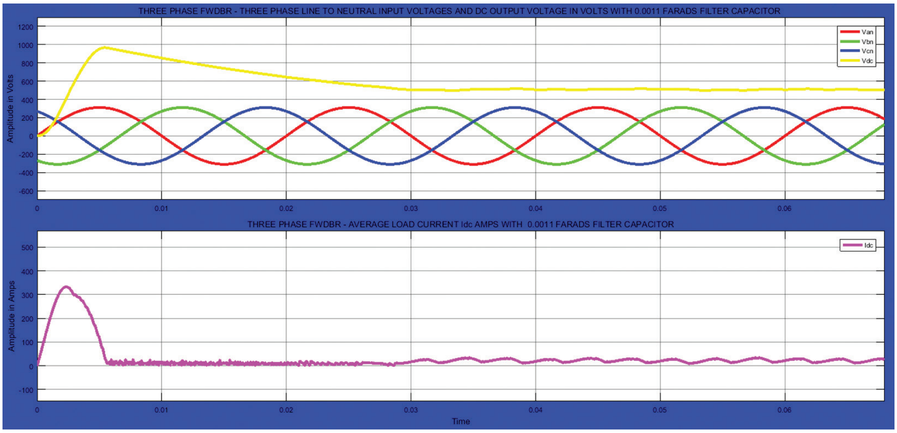


**FIGURE 3.20**
Three-phase FWDBR. (a–d) Three-phase line-to-neutral input voltages and DC output voltage in volts with 0.0011 farads filter capacitor. (e) Average load current ldc amps with 0.0011 farads capacitor.

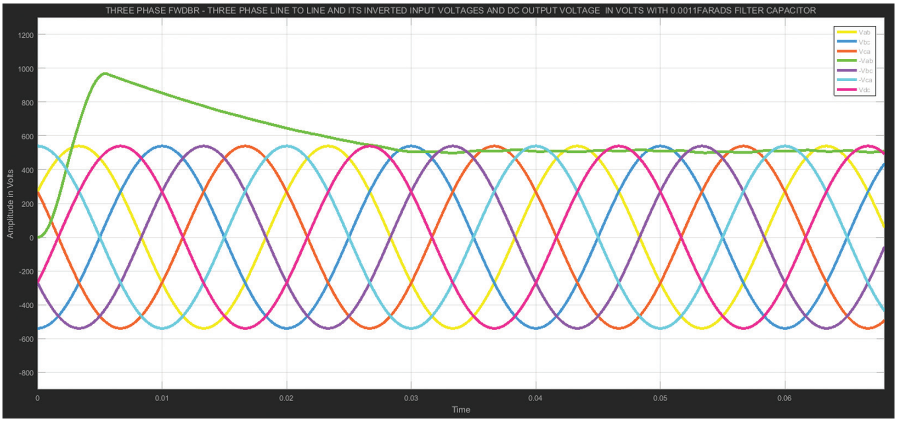


**FIGURE 3.21**
Three-phase FWDBR. Three-phase line to line and its inverted input voltages and DC output voltage in volts with 0.0011 farads filter capacitor.

**TABLE 3.6**
Simulation Results for Three-Phase FWDBR

| Sl. No. | RMS Load Voltage (V) | Average Load Voltage (V) | Average Load Current (A) | Remarks |
|---|---|---|---|---|
| **1** | 511 | 509.6 | 22.15 | No filter capacitor |
| **2** | **508** | **508** | **21.68** | With filter capacitor of 0.0011 farads |

values recorded in Table 3.6 by simulation closely agree with the theoretically calculated values [6].

## 3.5 Conclusions

The interactive model for the single-phase FWDBR based on the equations describing the system is presented. One model is suitable for either a purely resistive load or an RLE load. The type of load is easily selected using the selector switch. The simulation results in Figures 3.5 and 3.6 and the values in Table 3.2 agree well with reference [1]. The interactive model for the single-phase FWCBR based on the equations describing the system is presented. One model is suitable for either a purely resistive load or an RLE load. The type of load is easily selected using the selector switch. The simulation results in Figures 3.11 and 3.12 and the calculated values in Table 3.4 agree well with reference [1]. A novel method of system modelling the three-phase FWDBR using the Heaviside function is presented. The method is very similar to the one discussed in reference [6], except that here *abc* to *dq* and *dq* to *abc* transformations are used instead of *abc* to αβ and αβ to *abc* transformations. The recorded values of the average and RMS load voltage and load current in Table 3.6 by simulation agree closely with the corresponding values calculated using the formula.

## References

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# 4

# *Interactive Models for DC to AC Converters*

## 4.1 Introduction

In this chapter, the building of interactive system models for DC to AC converters, also known as *inverters*, is presented. Inverter circuits use silicon-controlled rectifiers (SCRs), BJTs, MOSFETs, IGBTs and GTOs. Here, initially, circuit models for three-phase 180° mode and 120° mode inverters using semiconductor switches such as BJTs are presented. Then, the switching function concept is used to develop system models for the inverter for these two modes of gate drive. These interactive models have pop-up menus or dialogue boxes where the required data relating to the DC to AC converter are entered by the user. These system models use modules from the Simulink® block set, which solve the governing equations relating to the relevant DC to AC converter. Here, the governing equations are the gate drive pattern for the two modes of inverter operation. No semiconductor circuit component is used in the system model.

## 4.2 Three-Phase 180° Mode Inverter

The three-phase 180° mode inverter topology is shown in Figure 4.1, where each switch M1 to M6 may be semiconductor components such as BJTs, MOSFETs, IGBTs or GTOs [1–4]. The switches M1 to M6 are as marked in Figure 4.1. Assume gate drives in Figure 4.1 have a period $T$, so that the output voltage of this inverter has a frequency of $(1/T)$ Hz. Pulse width modulation (PWM) is *not* considered here for simplicity. Then, each gate drive instance of turn ON and turn OFF duration in degrees are as marked in Figure 4.1. Each gate drive for switches M1 to M6 in order has a pulse ON duration of $(T/2)$ s or 180° and their instance or start of turn ON time between consecutive switches from M1 to M6 differ by $(T/6)$ s or 60°. A three-phase balanced resistive load is used. The DC link voltage $V_{dc}$ is 100 V and the output frequency of this inverter is 50 Hz. The PSIM simulation of the three-phase 180° mode 50 Hz inverter is shown in Figures 4.2a–c and 4.3a–c. Figure 4.2a–c show, respectively, three-phase line-to-ground, line-to-line and line-to-neutral voltages.

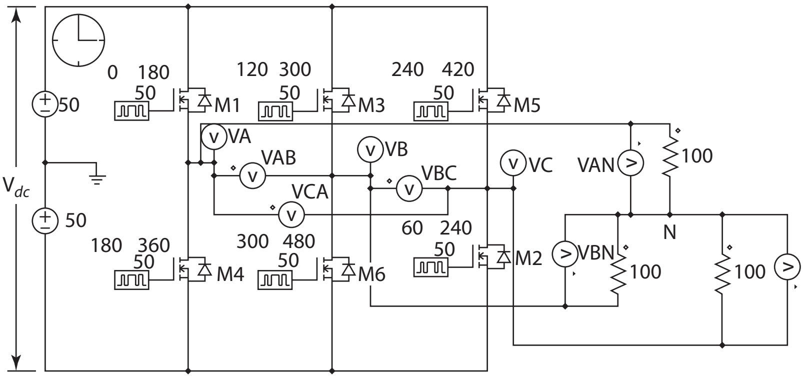


**FIGURE 4.1**
Three-phase 180° mode inverter.

The harmonic spectrum of the line-to-ground, line-to-line and line-to-neutral voltages are shown in Figure 4.3a–c respectively.

### 4.2.1 Analysis of Line-to-Line Voltage

Analysis of the line-to-line voltage of the three-phase 180° mode inverter is carried out in this section. The line-to-line voltage $V_{ry}$ is shown in Figure 4.2b. The theoretical derivation of the line-to-neutral voltage waveform is shown in Section 4.2.2. Shifting the axis of Figure 4.2b by π/6 makes the function $f(-t) = -f(+t)$ odd. The even harmonics are zero. The Fourier coefficient $b_n$ can be defined as follows:

$$b_n = \frac{4}{\pi} * \left[ \int_{\pi/6}^{\pi/2} V_{dc} * \sin(n.\omega.t).d(\omega.t) \right]$$

$$= \frac{4.V_{dc}}{n.\pi} * \left[ \cos\left(\frac{n.\pi}{6}\right) \right] \quad \text{for} \quad n = 1, 3, 5, 7 \ldots \tag{4.1}$$

The line-to-line voltage $V_{ry}$ can be expressed by a Fourier series, as follows:

$$V_{ry} = \sum_{1,3,5,7,\ldots}^{\infty} \frac{4.V_{dc}}{n.\pi} * \left[ \cos\left(\frac{n.\pi}{6}\right) * \sin\left(n.\omega.t + \frac{n.\pi}{6}\right) \right] \tag{4.2}$$

The RMS value of $V_{ry}$ is given as follows:

$$V_{ry\_\mathrm{rms}} = \sqrt{\left[ \frac{1}{\pi} * \int_{0}^{2\pi/3} V_{dc}^2 * d(\omega.t) \right]}$$

$$= \sqrt{\frac{2}{3}} * V_{dc} = 0.8165 * V_{dc} \tag{4.3}$$

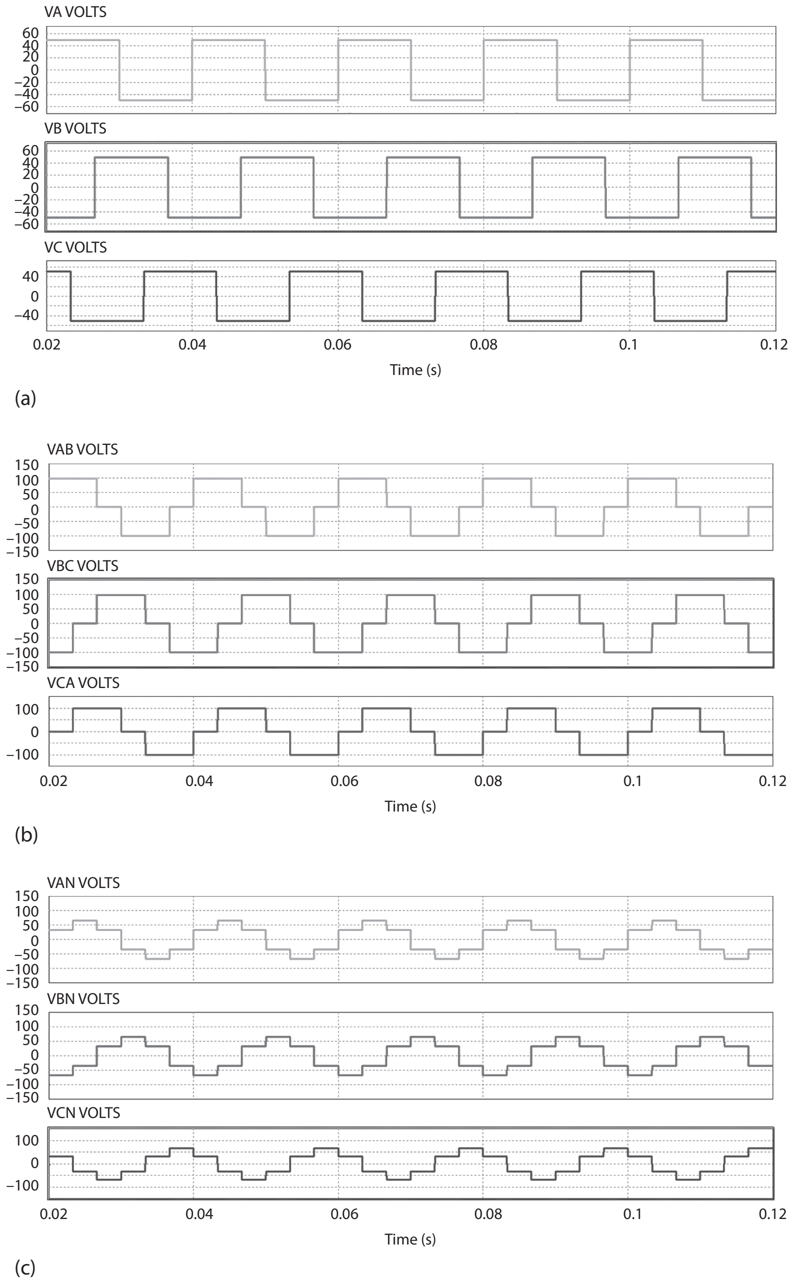


**FIGURE 4.2**
Three-phase 180° mode inverter. (a) Line-to-ground voltages. (b) Line-to-line voltages. (c) Line-to-neutral voltages.

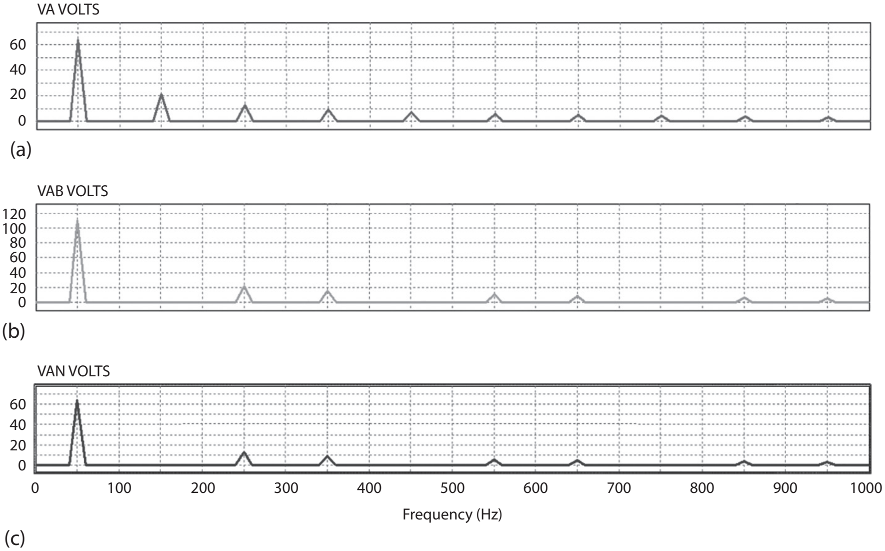


**FIGURE 4.3**
Three-phase 180° mode inverter: harmonic spectrum of (a) line-to-ground voltage, (b) line-to-line voltage, and (c) line-to-neutral voltage.

The RMS value of the fundamental component of $V_{ry}$ is given as follows:

$$V_{ry1\_\mathrm{rms}} = \frac{4.V_{dc}.\cos\left(\dfrac{\pi}{6}\right)}{\sqrt{2}.\pi} = \frac{\sqrt{6}}{\pi} * V_{dc} \tag{4.4}$$

The peak value of the fundamental component of the line-to-line voltage of a three-phase 180° mode inverter works out to 110.3 V for a DC link voltage of 100 V, which agrees with the one displayed in Figure 4.3b.

### 4.2.2 Analysis of Line-to-Neutral Voltage

In the following section, the root mean square (RMS) value and fast Fourier transform (FFT) of the line-to-neutral voltage of a six-step 180° mode inverter are derived.

For clarity, the line-to-neutral voltage of a three-phase 180° mode inverter is derived by simulation using PSIM, shown in Figure 4.1. A resistive star-connected load is used for convenience only, as an inductive load may give rise to voltage spikes in the waveform. The simulated line-to-neutral voltage is shown in Figure 4.2c. A three-phase 50 Hz waveform is generated. The waveform can be theoretically derived as follows:

By taking the ground $g$ as the midpoint of the two DC voltage sources, the line-to-ground voltages $V_{rg}$, $V_{yg}$ and $V_{bg}$ can be easily derived for three-phase

180° mode gate drive, by observation of Figure 4.1. This waveform is described as follows:

$$\begin{aligned} V_{rg} &= +\frac{V_{dc}}{2} \quad \text{for} \quad 0 \le \omega t \le \pi \\ &= -\frac{V_{dc}}{2} \quad \text{for} \quad \pi \le \omega t \le 2\pi \end{aligned} \tag{4.5}$$

$$\begin{aligned} V_{yg} &= +\frac{V_{dc}}{2} \quad \text{for} \quad 2\pi/3 \le \omega t \le 5\pi/3 \\ &= -\frac{V_{dc}}{2} \quad \text{for} \quad 0 \le \omega t \le 2\pi/3 \quad \text{and} \\ &\qquad\quad \text{for} \quad 5\pi/3 \le \omega t \le 2\pi \end{aligned} \tag{4.6}$$

$$\begin{aligned} V_{bg} &= +\frac{V_{dc}}{2} \quad \text{for} \quad 0 \le \omega t \le \pi/3 \quad \text{and} \\ &\qquad\quad \text{for} \quad 4\pi/3 \le \omega t \le 2\pi \\ &= -\frac{V_{dc}}{2} \quad \text{for} \quad \pi/3 \le \omega t \le 4\pi/3 \end{aligned} \tag{4.7}$$

Equations 4.5 to 4.7 confirm well the simulated waveform for three-phase line-to-ground voltage shown in Figure 4.2a.

Then, we have the following line-to-line voltage values:

$$V_{ry} = V_{rg} - V_{yg} \tag{4.8}$$

$$V_{yb} = V_{yg} - V_{bg} \tag{4.9}$$

$$V_{br} = V_{bg} - V_{rg} \tag{4.10}$$

From Equations 4.8 to 4.10, it is possible to derive the three-phase line-to-neutral voltages of a star-connected load, using the following relation:

$$\begin{vmatrix} V_{rn} \\ V_{yn} \\ V_{bn} \end{vmatrix} = \frac{1}{3} * \begin{vmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{vmatrix} * \begin{vmatrix} V_{ry} \\ V_{yb} \\ V_{br} \end{vmatrix} \tag{4.11}$$

Such a theoretically derived waveform agrees well with the one shown in Figure 4.2c.

The waveform derived by using Equations 4.5 to 4.11 gives the following coordinates for $V_{rn}$:

(0, $+V_{dc}/3$), ($\pi/3$, $+V_{dc}/3$), ($\pi/3$, $+2V_{dc}/3$), ($2\pi/3$, $+2V_{dc}/3$), ($2\pi/3$, $+V_{dc}/3$), ($\pi$, $+V_{dc}/3$), ($\pi$, $-V_{dc}/3$), ($4\pi/3$, $-V_{dc}/3$), ($4\pi/3$, $-2V_{dc}/3$), ($5\pi/3$, $-2V_{dc}/3$), ($5\pi/3$, $-V_{dc}/3$), ($2\pi$, $-V_{dc}/3$), ($2\pi$, $+V_{dc}/3$) and so on. These coordinates agree well with Figure 4.2c. Referring to Figure 4.2c and noting the coordinates given here, we have the following equation for the RMS value of line-to-neutral voltage:

$$V_{rn\_\text{rms}} = \sqrt{\frac{1}{\pi} * \left[ \frac{V_{dc}^2}{9} * \int_0^{\pi/3} d(\omega.t) + \frac{4.V_{dc}^2}{9} * \int_{\pi/3}^{2\pi/3} d(\omega.t) + \frac{V_{dc}^2}{9} * \int_{2\pi/3}^{\pi} d(\omega.t) \right]} \tag{4.12}$$

$$= \frac{\sqrt{2} * V_{dc}}{3} \tag{4.13}$$

The Fourier transform of the line-to-neutral voltage $V_{rn}$ is derived as follows:

Referring to Figure 4.2c, the axis of symmetry is the origin where $f(-t) = -f(+t)$ and the function is odd. Thus, the Fourier coefficient $b_n$ is given by the following:

$$b_n = \frac{2}{\pi} * \left[ \int_0^{\pi/3} \frac{V_{dc}}{3} * \sin(n.\omega.t).d(\omega.t) + \int_{\pi/3}^{2\pi/3} \frac{2V_{dc}}{3} * \sin(n.\omega.t).d(\omega.t) \right.$$
$$\left. + \int_{2\pi/3}^{\pi} \frac{V_{dc}}{3} * \sin(n.\omega.t).d(\omega.t) \right]$$
$$= \frac{2V_{dc}}{3\pi.n} * \left[ 1 - \cos\left(\frac{n.\pi}{3}\right) + 2 * \left( \cos\left(\frac{n.\pi}{3}\right) - \cos\left(\frac{2n.\pi}{3}\right) \right) \right.$$
$$\left. + \cos\left(\frac{2n.\pi}{3}\right) - \cos(n.\pi) \right] \tag{4.14}$$

$$= \sum_{n=1,5,7\ldots}^{\infty} \frac{2V_{dc}}{3\pi.n} * \left[ 1 + \cos\left(\frac{n.\pi}{3}\right) - \cos\left(\frac{2n.\pi}{3}\right) - \cos(n.\pi) \right] \tag{4.15}$$

Substituting $n = 1,2,3,\ldots$, we have the following general expression for the FFT of the line-to-neutral voltage:

$$V_{rn} = \frac{2V_{dc}}{\pi} * \left[ \sin(\omega.t) + \frac{1}{5} * \sin(5\omega.t) + \frac{1}{7} * \sin(7\omega.t) + \ldots \right] \tag{4.16}$$

The RMS value of the fundamental component of $V_{rn}$ is given here:

$$V_{rn1(\mathrm{rms})} = \frac{\sqrt{2}.V_{dc}}{\pi} \tag{4.17}$$

For a DC link voltage of 100 V, the peak fundamental component of $V_{rn}$ given by Equation 4.17 is 63.675 V, which agrees well with the simulation results shown in Figure 4.3c.

### 4.2.3 Total Harmonic Distortion

The output voltage of the three-phase inverter contains harmonics and, hence, the waveform is distorted. Total harmonic distortion (THD) is a measure of the closeness between a distorted waveform and its fundamental component. Thus, THD is the ratio of the RMS value of the distorted waveform and the RMS value of its fundamental component. The THD of the voltage waveform is defined here:

$$\mathrm{THD} = \sqrt{\left(\frac{V_{S\_\mathrm{RMS}}}{V_{S1\_\mathrm{RMS}}}\right)^2 - 1} \tag{4.18}$$

The same definition for THD given by Equation 4.18 holds good for currents as well.

Using Equations 4.3, 4.4, 4.13, 4.17 and 4.18, the THD of the line-to-line and line-to-neutral voltages are calculated as follows:

$$\text{THD of } V_{LL} = \sqrt{\left(\frac{2.V_{dc}^2/3}{6V_{dc}^2/\pi^2}\right) - 1} = 30.9\% \tag{4.19}$$

$$\text{THD of } V_{LN} = \sqrt{\left(\frac{2.V_{dc}^2/9}{2.V_{dc}^2/\pi^2}\right) - 1} = 30.9\% \tag{4.20}$$

### 4.2.4 Model for Three-Phase 180° Mode Inverter

The model of the three-phase 180° mode inverter is shown in Figure 4.4 [5–8]. The various dialogue boxes where users may enter data are given in Figure 4.5. The dialogue boxes mainly correspond to entering the frequency of switching the inverter and its DC link voltage. The phase advance is entered as zero. The details of the various subsystems of Figure 4.4 are shown in Figure 4.6a to d. The functions of the various subsystems are explained here:

Figure 4.6a is the subsystem for the three-phase 180° mode inverter gate drive parameters. The corresponding dialogue box is shown in Figure 4.5.

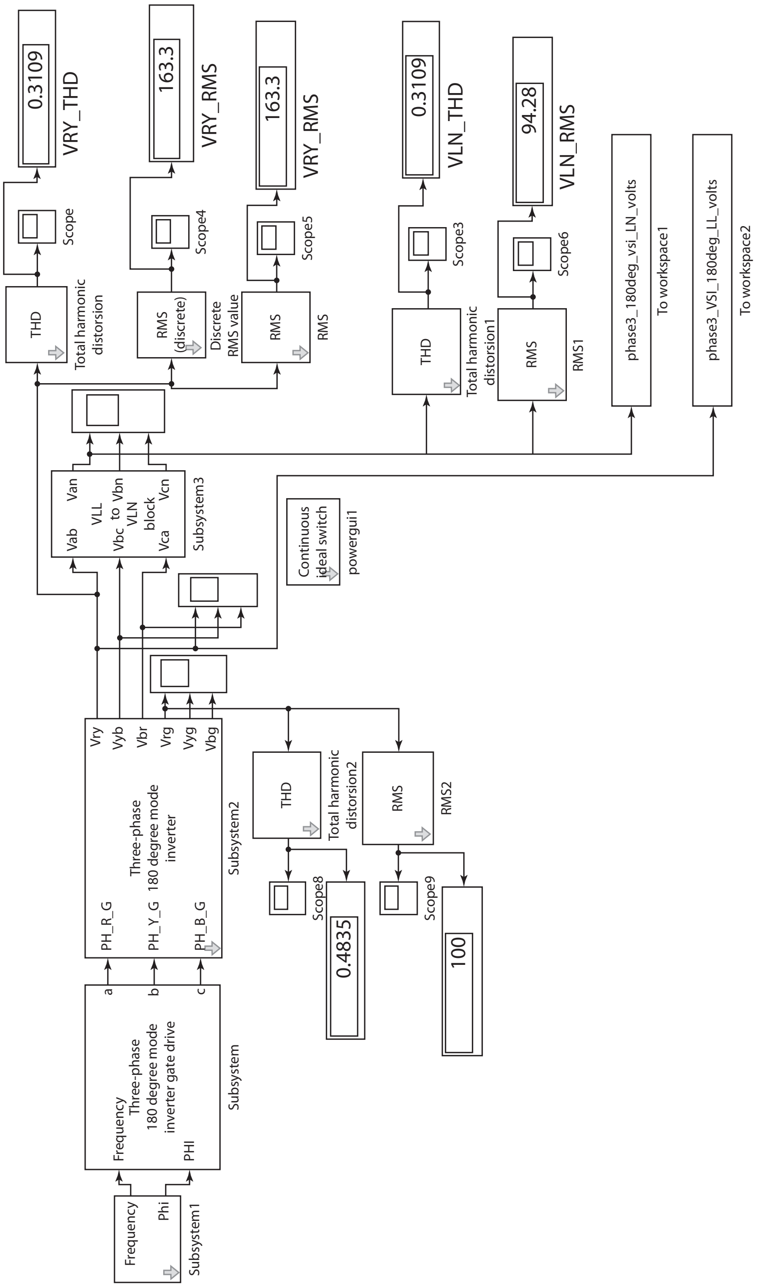
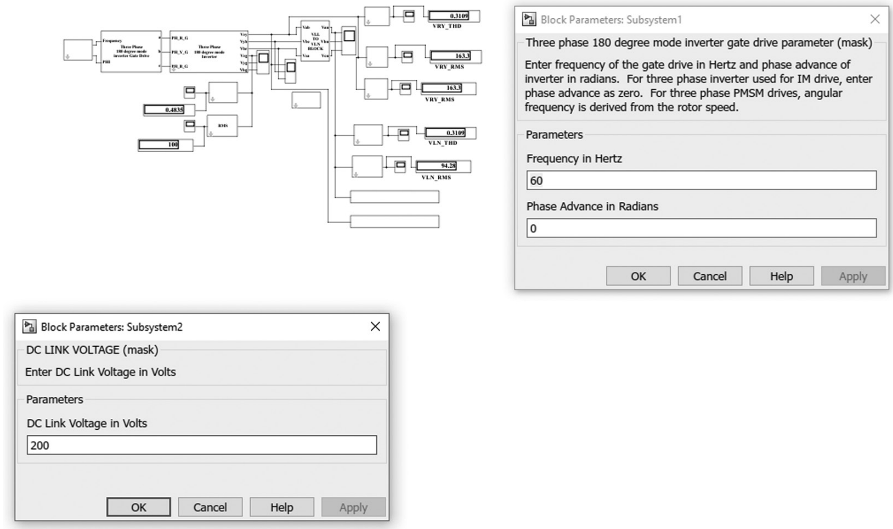

Frequency
Phi
Subsystem1
Frequency
Three-phase
180 degree mode
inverter gate drive
PHI
Subsystem
a
b
c
PH_R_G
PH_Y_G
PH_B_G
Three-phase
180 degree mode
inverter
Subsystem2
Vry
Vyb
Vbr
Vrg
Vyg
Vbg
THD
Total harmonic
distorsion2
Scope8
0.4835
RMS
RMS2
Scope9
100
Continuous
ideal switch
powergui1
Vab
Vbc
Vca
VLL
to
VLN
block
Van
Vbn
Vcn
Subsystem3
THD
Total harmonic
distorsion
Scope
0.3109
VRY_THD
RMS
(discrete)
Discrete
RMS value
Scope4
163.3
VRY_RMS
RMS
RMS
Scope5
163.3
VRY_RMS
THD
Total harmonic
distorsion1
Scope3
0.3109
VLN_THD
RMS
RMS1
Scope6
94.28
VLN_RMS
phase3_180deg_vsi_LN_volts
To workspace1
phase3_VSI_180deg_LL_volts
To workspace2

**FIGURE 4.4**
Model of a three-phase 180° mode inverter.


Frequency
PHI
Three Phase 180 degree mode inverter Gate Drive
a
b
c
PH_R_G
PH_Y_G
PH_B_G
Three Phase 180 degree mode Inverter
Vry
Vyb
Vbr
Vrg
Vyg
Vbg
Vab
Vbc
Vca
VLL TO VLN BLOCK
Van
Vbn
Vcn
0.3109
VRY_THD
163.3
VRY_RMS
163.3
VRY_RMS
0.3109
VLN_THD
94.28
VLN_RMS
0.4835
RMS
100

Block Parameters: Subsystem1

Three phase 180 degree mode inverter gate drive parameter (mask)

Enter frequency of the gate drive in Hertz and phase advance of inverter in radians. For three phase inverter used for IM drive, enter phase advance as zero. For three phase PMSM drives, angular frequency is derived from the rotor speed.

Parameters

Frequency in Hertz: 60

Phase Advance in Radians: 0

OK
Cancel
Help
Apply

Block Parameters: Subsystem2

DC LINK VOLTAGE (mask)

Enter DC Link Voltage in Volts

Parameters

DC Link Voltage in Volts: 200

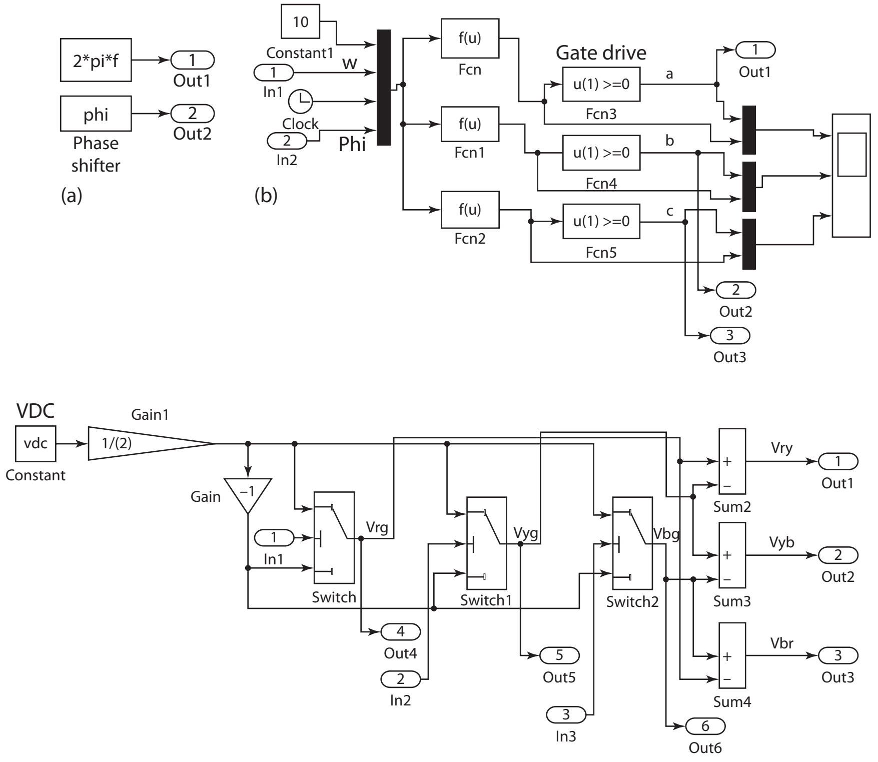
OK
Cancel
Help
Apply

**FIGURE 4.5**
Model of a three-phase 180° mode inverter with interactive blocks.

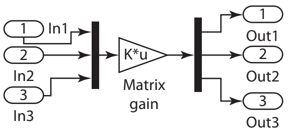
The frequency entered is 60 Hz and the phase advance is zero. This frequency is internally multiplied by 2π to obtain the angular frequency to generate the sine wave and the gate drive for the inverter.

The outputs of Figure 4.6a are passed to the four-input mux in Figure 4.6b. In Figure 4.6b, the three Fcn blocks, Fcn, Fcn1 and Fcn2, connected to the four-input mux, generate a three-phase sine wave at the frequency entered with the phase advance added. The three-phase sine-wave output is connected to three Fcn blocks, Fcn3, Fcn4 and Fcn5, which compare the respective $u(1)$ inputs with 0, generate logic 1 if $u(1)$ is greater than or equal to zero, else output logic 0. The output of the three Fcn blocks Fcn3, Fcn4 and Fcn5 are the switch functions $a$, $b$ and $c$.

The output $a$, $b$ and $c$ of the three Fcn blocks in Figure 4.6b are passed to the second $u(2)$ input of the three threshold switches, Switch, Switch1 and Switch2, respectively, in Figure 4.6c. One half of the DC link voltages $+V_{dc}/2$ and $-V_{dc}/2$ is generated using a constant block and two gain blocks, Gain and Gain1, as shown in Figure 4.6c. The $u(1)$ and $u(3)$ input to these three threshold switches are $+V_{dc}/2$ and $-V_{dc}/2$, respectively. When the $u(2)$ input to these three threshold switches is greater than or equal to the threshold value of 0.5, the outputs of these switches equal $+V_{dc}/2$, else the outputs equal $-V_{dc}/2$. Thus, the three switches generate the three-phase line-to-ground voltages $V_{rg}$, $V_{yg}$ and $V_{bg}$, respectively. These line-to-ground voltages are subtracted in pairs using subtract blocks Sum2, Sum3 and Sum4 to generate the three-phase line-to-line voltages $V_{ry}$, $V_{yb}$ and $V_{br}$, respectively. Figure 4.6c opens up the dialogue box shown in Figure 4.5 for the DC link voltage. The DC link voltage entered is 200 V.


2*pi*f
1
Out1
phi
2
Out2
Phase shifter
(a)
10
Constant1
w
1
In1
Clock
2
In2
Phi
(b)
f(u)
Fcn
f(u)
Fcn1
f(u)
Fcn2
Gate drive
u(1) >=0
Fcn3
u(1) >=0
Fcn4
u(1) >=0
Fcn5
a
b
c
1
Out1
2
Out2
3
Out3
VDC
vdc
Constant
Gain1
1/(2)
Gain
−1
1
In1
Switch
Vrg
Switch1
Vyg
Switch2
Vbg
4
Out4
2
In2
5
Out5
3
In3
6
Out6
Sum2
Vry
1
Out1
Sum3
Vyb
2
Out2
Sum4
Vbr
3
Out3

(c) Six-step 180 degree mode inverter


1
In1
2
In2
3
In3
K*u
Matrix gain
1
Out1
2
Out2
3
Out3

Vll to vln block

(d)

**FIGURE 4.6**
(a–d) Three-phase 180° mode inverter model subsystems.

The three-phase line-to-line voltages $V_{ry}$, $V_{yb}$ and $V_{br}$ are respectively applied to the three-input mux shown in Figure 4.6d. The Matrix Gain block in Figure 4.6d multiplies $V_{ry}$, $V_{yb}$ and $V_{br}$ by the matrix defined in Equation 4.11 to obtain the line-to-neutral voltages $V_{rn}$, $V_{yn}$ and $V_{bn}$ as the output of the demux block.

The THD and RMS values of the line-to-line and line-to-neutral voltages are measured using appropriate measurement blocks from the Power Systems block set. The Powergui from the Power Systems block set is used to display the harmonic spectrum of the line-to-neutral and line-to-line voltages.

### 4.2.5 Simulation Results

The simulation of the three-phase 180° mode inverter model was carried out using the ode23t (mod. stiff/trapezoidal) solver. The three-phase line-to-ground voltages, line-to-line voltages and line-to-neutral voltages are shown in Figures 4.7a to c, 4.8a to c and 4.9a to c, respectively. The RMS and THD values of the line-to-line voltages are shown in Figure 4.10a and b and those corresponding to the line-to-neutral voltages are shown in Figure 4.11a and b, respectively. The harmonic spectrum of the line-to-line voltages is shown in Figure 4.12a and b and that corresponding to the line-to-neutral voltages is shown in Figure 4.13a and b, respectively. The results observed for the THD and RMS values of the line-to-line and line-to-neutral voltages by simulation

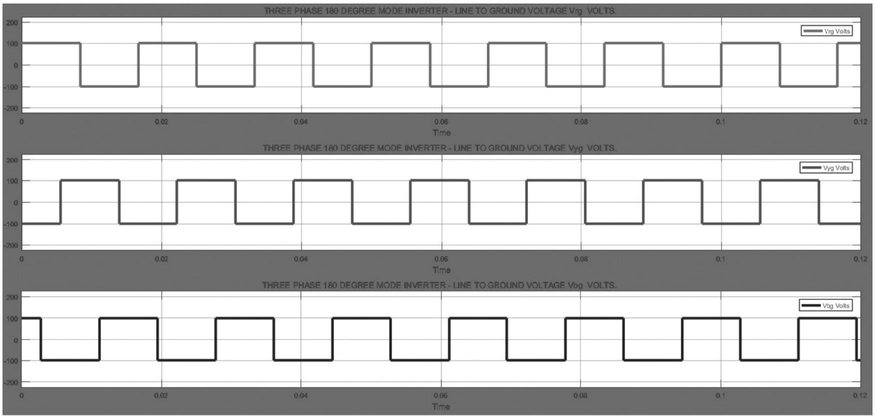


**FIGURE 4.7**
Three-phase 180° mode inverter. Line-to-ground voltage: (a) $V_{rg}$ V, (b) $V_{yg}$ V and (c) $V_{bg}$ V.

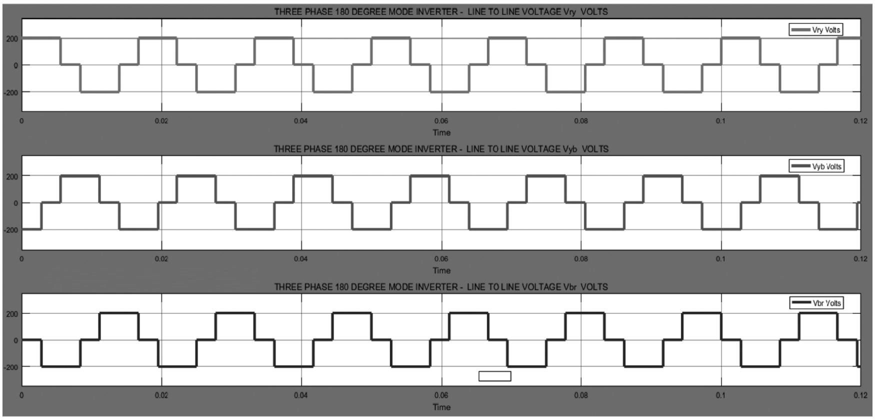


**FIGURE 4.8**
Three-phase 180° mode. Line-to-line voltage: (a) $V_{ry}$ V, (b) $V_{yb}$ V and (c) $V_{br}$ V.

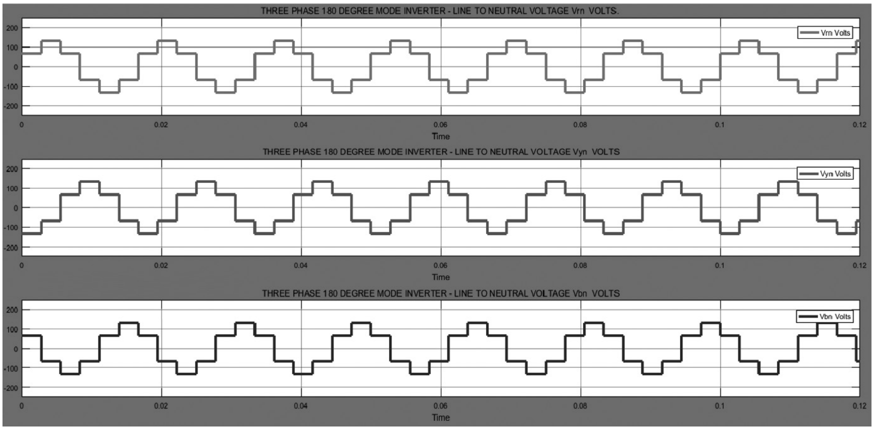


**FIGURE 4.9**
Three-phase 180° mode inverter. Line-to-neutral voltage: (a) $V_{rn}$ V, (b) $V_{yn}$ V and (c) $V_{bn}$ V.

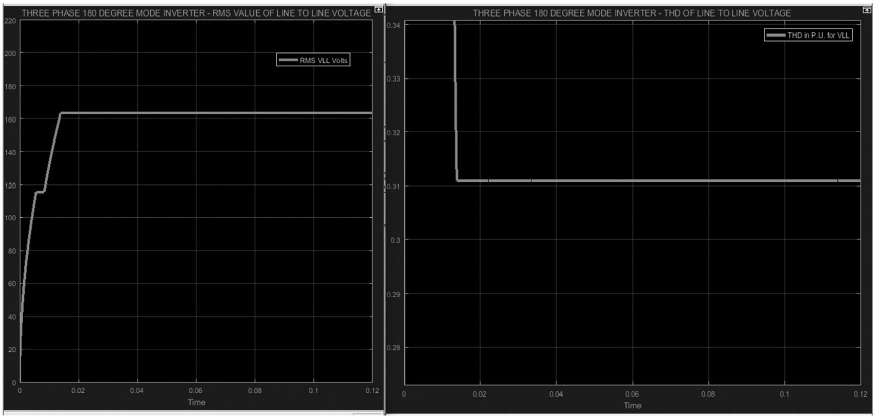


**FIGURE 4.10**
Three-phase 180° mode inverter. (a) RMS value of line-to-line voltage. (b) THD of line-to-line voltage.

are also tabulated in Table 4.1. The theoretically calculated THD and RMS values of the line-to-line and line-to-neutral voltages using Equations 4.3, 4.4, 4.13 and 4.17 are tabulated in Table 4.2.

## 4.3 Three-Phase 120° Mode Inverter

The three-phase inverter shown in Figure 4.1 can also be driven by 120° mode gate drive.

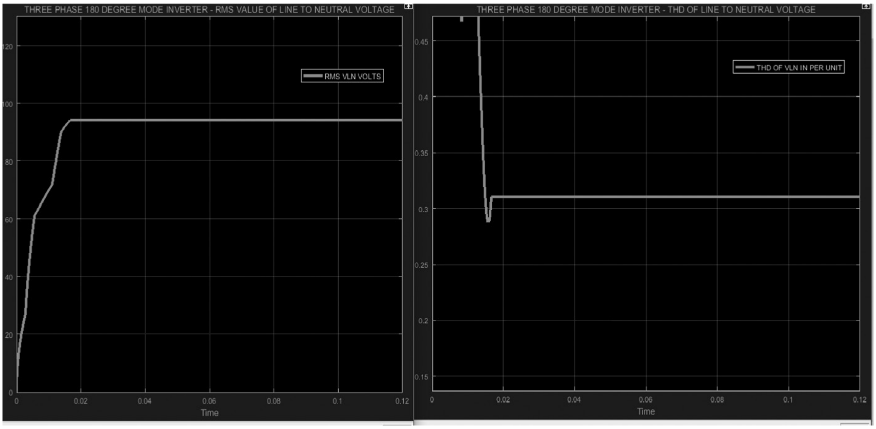
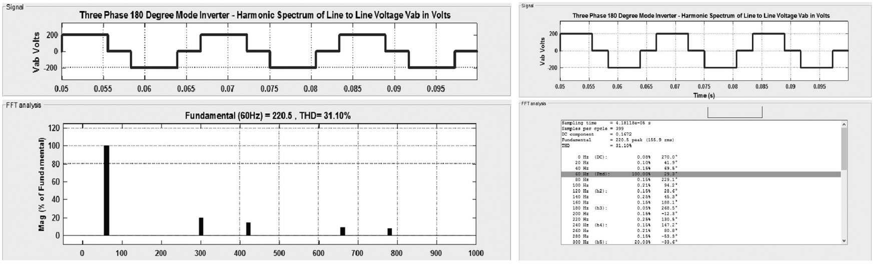


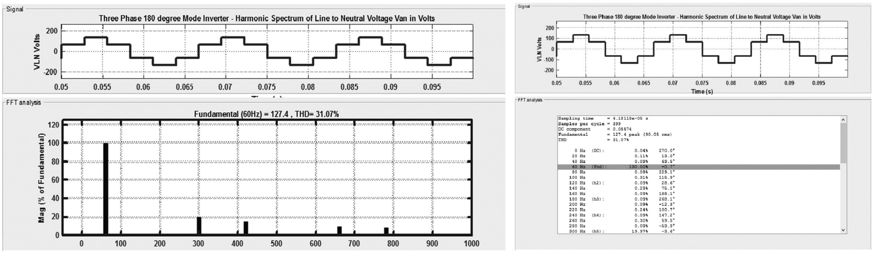
**FIGURE 4.11**
Three-phase 180° mode inverter. (a) RMS value of line-to-neutral voltage. (b) THD of line-to-neutral voltage.


Signal
Three Phase 180 Degree Mode Inverter - Harmonic Spectrum of Line to Line Voltage Vab in Volts
Vab Volts
200
0
-200
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
Time (s)
FFT analysis
Fundamental (60Hz) = 220.5 , THD= 31.10%
Mag (% of Fundamental)
120
100
80
60
40
20
0
0
100
200
300
400
500
600
700
800
900
1000

```
Sampling time     = 4.18118e-05 s
Samples per cycle = 399
DC component      = 0.1672
Fundamental       = 220.5 peak (155.9 rms)
THD               = 31.10%

     0 Hz  (DC):         0.08%    270.0°
    20 Hz                0.10%     41.9°
    40 Hz                0.15%     69.5°
    60 Hz  (Fnd):      100.00%     29.3°
    80 Hz                0.15%    229.1°
   100 Hz                0.21%     94.2°
   120 Hz  (h2):         0.15%     28.6°
   140 Hz                0.25%     45.3°
   160 Hz                0.15%    188.1°
   180 Hz  (h3):         0.05%    268.5°
   200 Hz                0.15%    -12.3°
   220 Hz                0.25%    130.5°
   240 Hz  (h4):         0.15%    147.2°
   260 Hz                0.21%     80.8°
   280 Hz                0.15%    -53.3°
   300 Hz  (h5):        20.03%    -33.6°
```

**FIGURE 4.12**
(a,b) Three-phase 180° mode inverter: harmonic spectrum of line-to-line voltage $V_{ab}$ in volts.


Signal
Three Phase 180 degree Mode Inverter - Harmonic Spectrum of Line to Neutral Voltage Van in Volts
VLN Volts
200
100
0
-100
-200
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
Time (s)
FFT analysis
Fundamental (60Hz) = 127.4 , THD= 31.07%
Mag (% of Fundamental)
120
100
80
60
40
20
0
0
100
200
300
400
500
600
700
800
900
1000

```
Sampling time     = 4.18118e-05 s
Samples per cycle = 399
DC component      = 0.05574
Fundamental       = 127.4 peak (90.05 rms)
THD               = 31.07%

     0 Hz  (DC):         0.04%    270.0°
    20 Hz                0.11%     13.0°
    40 Hz                0.09%     69.5°
    60 Hz  (Fnd):      100.00%     -0.7°
    80 Hz                0.09%    229.1°
   100 Hz                0.31%    115.9°
   120 Hz  (h2):         0.09%     28.6°
   140 Hz                0.23%     75.1°
   160 Hz                0.09%    188.1°
   180 Hz  (h3):         0.09%    268.1°
   200 Hz                0.09%    -12.3°
   220 Hz                0.24%    100.7°
   240 Hz  (h4):         0.09%    147.2°
   260 Hz                0.30%     59.5°
   280 Hz                0.09%    -53.3°
   300 Hz  (h5):        19.97%     -3.6°
```

**FIGURE 4.13**
(a,b) Three-phase 180° mode inverter: harmonic spectrum of line-to-neutral voltage $V_{an}$ in volts.

**TABLE 4.1**

Three-Phase 180° Mode Inverter: Simulation Results

| Sl.No. | Frequency(Hz) | DC Link Voltage (V) | THD of $V_{LL}$ (Per Unit) | RMS $V_{LL}$ (V) | THD of $V_{LN}$ (Per Unit) | RMS $V_{LN}$ (V) |
|---|---|---|---|---|---|---|
| 1 | 60 | 200 | 0.3109 | 163.3 | 0.3109 | 94.28 |

**TABLE 4.2**

Three-Phase 180° Mode Inverter: Calculated Values

| Sl. No. | Frequency (Hz) | DC Link Voltage (V) | THD of $V_{LL}$ (Per Unit) | RMS $V_{LL}$ (V) | THD of $V_{LN}$ (Per Unit) | RMS $V_{LN}$ (V) |
|---|---|---|---|---|---|---|
| 1 | 60 | 200 | 0.309 | 163.28 | 0.309 | 94.27 |

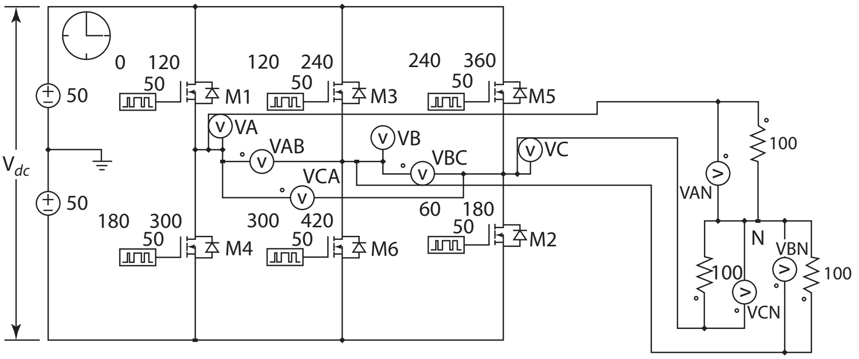


**FIGURE 4.14**
Three-phase inverter: 120° mode.

The three-phase 120° mode inverter topology is shown in Figure 4.14. The switches M1 to M6 are as marked in Figure 4.14. Assume that the gate drives in Figure 4.14 have a period $T$, so that the output voltage of this inverter has a frequency of $(1/T)$ Hz. PWM is not considered here for simplicity. Then, each gate drive instance of turn ON and turn OFF duration in degrees are as marked in Figure 4.14. Each gate drive M1 to M6 in order has a pulse ON duration of $(T/3)$ s or 120° and their instance or start of turn ON time between successive switches from M1 to M6 differ by $(T/6)$ s or 60°. A three-phase balanced resistive load is used. The DC link voltage $V_{dc}$ is 100 V and the output frequency of this inverter is 50 Hz. The PSIM simulation of the three-phase 120° mode 50 Hz inverter is shown in Figures 4.15a to c, 4.16a to c and 4.17a to c. Figure 4.18a to c shows the harmonic spectrum of the three-phase line-to-ground, line-to-line and line-to-neutral voltages, respectively.

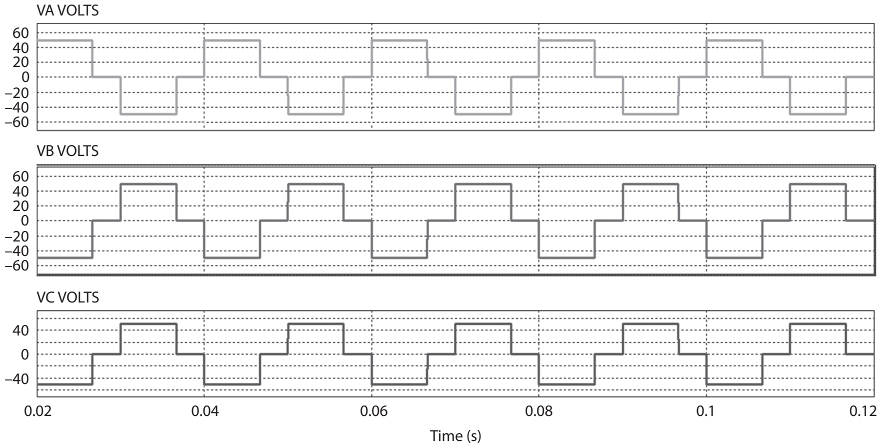


**FIGURE 4.15**
(a–c) Three-phase 120° mode inverter: line-to-ground voltage.

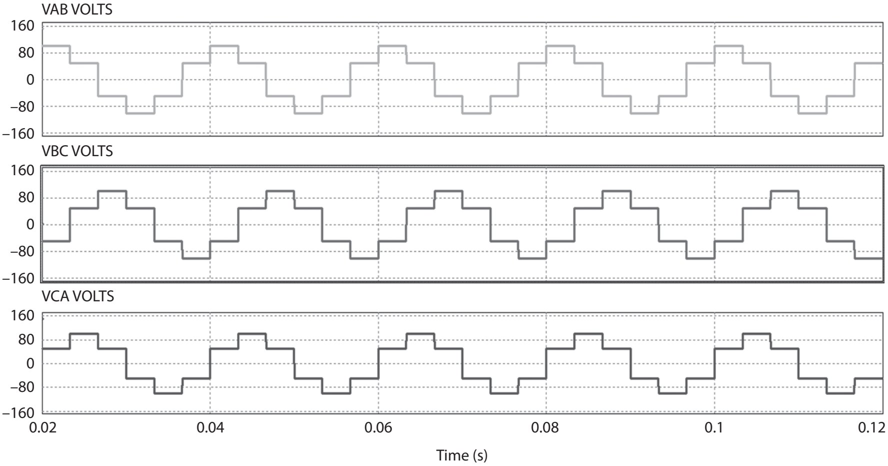


**FIGURE 4.16**
(a–c) Three-phase 120° mode inverter: line-to-line voltage.

### 4.3.1 Analysis of Line-to-Line Voltage

Analysis of the line-to-line voltage of the three-phase 120° mode inverter is carried out in this section. The line-to-line voltage $V_{ry}$ is shown in Figure 4.16a. The theoretical derivation of the line-to-neutral voltage waveform is shown in Section 4.3.2. Shifting the axis of Figure 4.16a by $\pi/3$ makes the

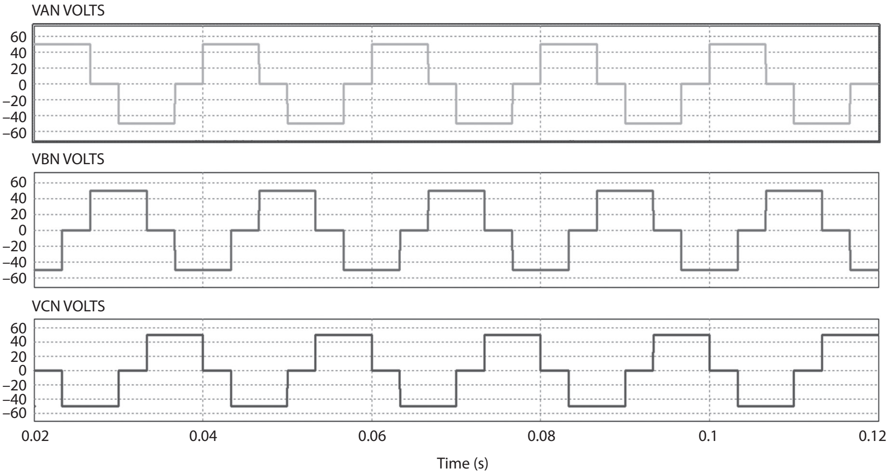


**FIGURE 4.17**
(a–c) Three-phase 120° mode inverter: line-to-neutral voltage.

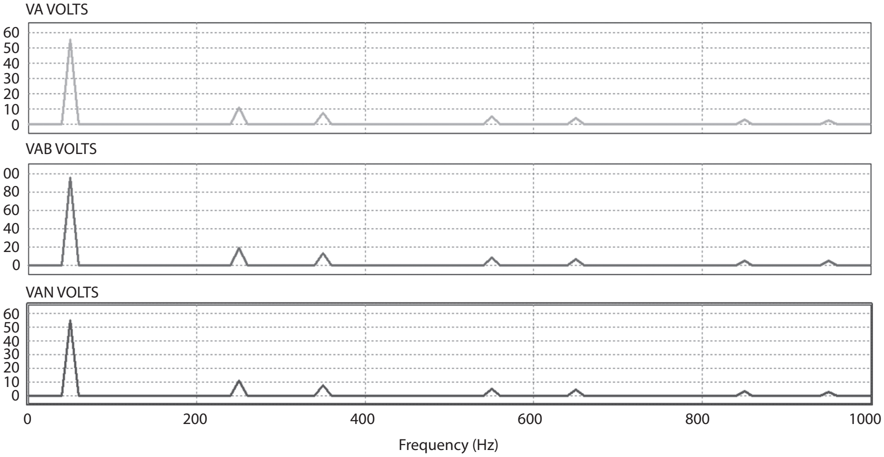


**FIGURE 4.18**
Three-phase 120° mode inverter: harmonic spectrum of (a) line-to-ground voltage, (b) line-to-line voltage and (c) line-to-neutral voltage.

function $f(-t) = -f(+t)$ odd. The even harmonics are zero. The Fourier coefficient $b_n$ can be defined as follows:

$$b_n = \frac{4}{\pi} * \left[ \int_0^{\pi/3} \frac{V_{dc}}{2} * \sin(n\omega.t).d(\omega.t) + \int_{\pi/3}^{\pi/2} V_{dc} * \sin(n\omega.t).d(\omega.t) \right]$$
$$= \sum_{n=1,3,5,7,\ldots}^{\infty} \frac{2V_{dc}}{\pi.n} * \left[ 1 + \cos\left( \frac{n.\pi}{3} \right) \right] \tag{4.21}$$

The line-to-line voltage $V_{ry}$ can be expressed by a Fourier series, as follows:

$$V_{ry} = \sum_{n=1,3,5,7,\ldots}^{\infty} \frac{2V_{dc}}{\pi.n} * \left[1+\cos\left(\frac{n.\pi}{3}\right) * \sin\left(n.\omega.t+\frac{n.\pi}{3}\right)\right] \tag{4.22}$$

The RMS value of $V_{ry}$ is given as follows:

$$V_{ry\_\text{rms}} = \sqrt{\frac{1}{\pi} * \left[\int_0^{\pi/3} V_{dc}^2 * d(\omega.t) + \int_{\pi/3}^{2\pi/3} \frac{V_{dc}^2}{4} * d(\omega.t) + \int_{2\pi/3}^{\pi} \frac{V_{dc}^2}{4} * d(\omega.t)\right]} \tag{4.23}$$

$$= \frac{V_{dc}}{\sqrt{2}}$$

The RMS value of the fundamental component of $V_{ry}$ from Equation 4.22 is given here:

$$V_{ry1\_\text{rms}} = \frac{3}{\sqrt{2}} * \left[\frac{V_{dc}}{\pi}\right] \tag{4.24}$$

The peak value of the fundamental component of $V_{ry}$ shown in Figure 4.18b agrees well with Equation 4.24 for a DC link voltage of 100 V.

### 4.3.2 Analysis of Line-to-Neutral Voltage

In the following section, the RMS value and FFT of the line-to-neutral voltage of a six-step 120° mode inverter are derived. For clarity, the line-to-neutral voltage of a three-phase 120° mode inverter is derived by simulation using PSIM, shown in Figure 4.14. A resistive star-connected load is used for convenience only, as an inductive load may give rise to voltage spikes in the waveform. The simulated line-to-neutral voltage is shown in Figure 4.17a to c. A three-phase 50 Hz waveform is generated. The DC link voltage used is 100 V. The waveform can be theoretically derived as follows:

Referring to Figure 4.14, by taking the ground $g$ as the midpoint of the two DC voltage sources forming the DC link, the line-to-ground voltages $V_{rg}$, $V_{yg}$ and $V_{bg}$ can be easily derived for the three-phase 120° mode gate drive, by observation of Figure 4.14 and its gate drive pattern discussed here. This waveform is described as follows:

$$\begin{aligned} V_{rg} &= +V_{dc}/2 \quad \text{for} \quad 0 \le \omega t \le 2\pi/3 \\ &= 0 \quad \text{for} \quad 2\pi/3 \le \omega t \le \pi \\ &= -V_{dc}/2 \quad \text{for} \quad \pi \le \omega t \le 5\pi/3 \\ &= 0 \quad \text{for} \quad 5\pi/3 \le \omega t \le 2\pi \end{aligned} \tag{4.25}$$

$$
\begin{aligned}
V_{yg} &= +V_{dc}/2 \quad \text{for} \quad 2\pi/3 \le \omega t \le 4\pi/3 \\
&= 0 \quad \text{for} \quad 4\pi/3 \le \omega t \le 5\pi/3 \\
&= -V_{dc}/2 \quad \text{for} \quad 5\pi/3 \le \omega t \le 2\pi \quad \text{and} \\
&\qquad \text{for} \quad 0 \le \omega t \le \pi/3 \\
&= 0 \quad \text{for} \quad \pi/3 \le \omega t \le 2\pi/3
\end{aligned} \tag{4.26}
$$

$$
\begin{aligned}
V_{bg} &= +V_{dc}/2 \quad \text{for} \quad 4\pi/3 \le \omega t \le 2\pi \\
&= 0 \quad \text{for} \quad 0 \le \omega t \le \pi/3 \\
&= -V_{dc}/2 \quad \text{for} \quad \pi/3 \le \omega t \le \pi \\
&= 0 \quad \text{for} \quad \pi \le \omega t \le 4\pi/3
\end{aligned} \tag{4.27}
$$

From Equations 4.25, 4.26 and 4.27, the line-to-line voltages can be expressed as follows:

$$V_{ry} = V_{rg} - V_{yg} \tag{4.28}$$

$$V_{yb} = V_{yg} - V_{bg} \tag{4.29}$$

$$V_{br} = V_{bg} - V_{rg} \tag{4.30}$$

The line-to-neutral voltages $V_{rn}$, $V_{yn}$ and $V_{bn}$ can be derived as follows:

$$\begin{vmatrix} V_{rn} \\ V_{yn} \\ V_{bn} \end{vmatrix} = \frac{1}{3} * \begin{vmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{vmatrix} * \begin{vmatrix} V_{ry} \\ V_{yb} \\ V_{br} \end{vmatrix} \tag{4.31}$$

The waveform derived using Equation 4.31 looks much the same as shown in Figure 4.17a to c.

The waveform derived by using Equations 4.25 to 4.31 gives the following coordinates for $V_{rn}$:

(0, 0), (0, $+V_{dc}/2$), ($2\pi/3$, $+V_{dc}/2$), ($2\pi/3$, 0), ($\pi$, 0), ($\pi$, $-V_{dc}/2$), ($5\pi/3$, $-V_{dc}/2$), ($5\pi/3$, 0), ($2\pi$, 0), ($2\pi$, $+V_{dc}/2$) and so on.

Referring to Figure 4.17a and noting the coordinates given here, we have the following equation for the RMS value of the line-to-neutral voltage:

$$V_{rn\_\text{rms}} = \sqrt{\frac{1}{\pi} * \int_0^{2\pi/3} \left[\frac{V_{dc}^2}{4}\right] .d(\omega.t)} = \frac{V_{dc}}{\sqrt{6}} \tag{4.32}$$

The Fourier transform of the line-to-neutral voltage $V_{rn}$ is derived as follows:

Referring to Figure 4.17a, the axis of symmetry is shifted by π/6 from the origin where $f(-t) = -f(+t)$ and the function is odd. The even harmonics are zero. Thus, the Fourier coefficient $b_n$ is given by the following equation:

$$\begin{aligned} b_n &= \frac{2}{\pi} * \left[ \int_{\pi/6}^{5\pi/6} \frac{V_{dc}}{2} * \sin(n.\omega.t).d(\omega.t) \right] \\ &= \frac{2V_{dc}}{n.\pi} * \cos\left(\frac{n.\pi}{6}\right) \mathit{for}\ n = 1,3,5,7\ldots \end{aligned} \tag{4.33}$$

The line-to-neutral voltage $V_{rn}$ can be expressed by a Fourier series, as follows:

$$V_{rn} = \sum_{1,3,5,7,\ldots}^{\infty} \frac{2V_{dc}}{n.\pi} * \cos\left(\frac{n.\pi}{6}\right) * \sin\left(n.\omega.t + \frac{n.\pi}{6}\right) \tag{4.34}$$

The RMS value of the fundamental component of $V_{rn}$ from Equation 4.34 is given here:

$$V_{rn1\_\mathrm{rms}} = \sqrt{\frac{3}{2}} * \left[\frac{V_{dc}}{\pi}\right] \tag{4.35}$$

The peak value of the fundamental component of $V_{rn}$ shown in Figure 4.18c agrees well with Equation 4.35.

### 4.3.3 Total Harmonic Distortion

The THD of the voltage wave form is defined by Equation 4.18 in Section 4.2.3.

Using Equations 4.23, 4.24, 4.32 and 4.35, the THD of the line-to-line and line-to-neutral voltages are calculated as follows:

$$\text{THD of } V_{LL} = \sqrt{\frac{V_{dc}^2/2}{9.V_{dc}^2/2.\pi^2} - 1} = 30.9\% \tag{4.36}$$

$$\text{THD of } V_{LN} = \sqrt{\frac{V_{dc}^2/6}{3.V_{dc}^2/2.\pi^2} - 1} = 30.9\% \tag{4.37}$$

### 4.3.4 Model of Three-Phase 120° Mode Inverter

The model of the three-phase 120° mode inverter is shown in Figure 4.19 [8]. The various dialogue boxes where the user may enter data are given in Figure 4.20. The dialogue boxes mainly correspond to entering the frequency of switching the inverter and its DC link voltage. The phase advance is entered as zero. The details of the various subsystems of Figure 4.19 are shown in Figure 4.21a to d. The functions of the various subsystems are explained next.

Figure 4.21a corresponds to the dialogue box with the name 'Three-phase 120 degree mode inverter gate drive' shown in Figure 4.20. A value of 60 is entered in the dialogue box corresponding to the inverter switching frequency and zero corresponding to the phase advance. This frequency is internally multiplied by 2π to obtain the angular switching frequency of the inverter. PWM is not considered in this model.

The three-phase 120° mode inverter gate drive block is shown in Figure 4.21b. The four inputs to the mux are the arbitrary constant, angular switching frequency, time and switching angle advance. The three-phase sine-wave AC with angular frequency corresponding to the frequency entered with phase advance added is generated using the Fcn1, Fcn2 and Fcn3 blocks. Each of the three-phase AC outputs are then compared in Schmitt trigger relay comparators; Relay1, 2 and 3 are used as zero-crossing comparators. The output of Relay1, 2 and 3 becomes logic 1 when the respective input crosses zero and becomes positive and their output becomes logic 0 when their respective input crosses zero and becomes negative.

The three-phase 120° mode inverter block is shown in Figure 4.21c. The *a*, *b*, *c* outputs of Relay1, 2 and 3 are passed in pairs to three Fcn blocks, Fcn6, Fcn7 and Fcn8, using three two-input mux. The three Fcn blocks Fcn6, 7 and 8 subtract the two inputs to their respective mux. Each of the three Subtract blocks are passed to a pair of zero-comparison blocks. The Fcn3 block outputs logic 1 when the input $u(1)$ is greater than zero, else outputs logic 0. Similarly, the Fcn4 block outputs logic 1 when the input $u(1)$ is less than zero, else outputs logic 0. The same logic holds good for zero-comparison block pairs Fcn5–Fcn9 and Fcn10–Fcn11. The outputs of Fcn3 and Fcn4 are passed to the $u(2)$ input of threshold Switch and Switch1, respectively. The $u(1)$ inputs for Switch and Switch1 are, respectively, $+V_{dc}/2$ and $-V_{dc}/2$ and the $u(3)$ inputs to both switches are zeros. Both Switch and Switch1 output $u(1)$ when $u(2)$ is greater than or equal to the threshold value of 0.5, else their output is $u(3)$. The output of Switch and Switch1 are connected to the Add block. The same principle holds good for the switch pairs corresponding to the Fcn5–Fcn9 and Fcn10–Fcn11 block pairs. Thus, each of the Add blocks generate the line-to-ground voltages, $V_{rg}$, $V_{yg}$ and $V_{bg}$, respectively. The three-phase line-to-ground voltages are subtracted in pairs using the three Subtract blocks marked Add3, Add4 and Add5 to generate the three-phase line-to-line voltages $V_{ry}$, $V_{yb}$ and $V_{br}$.

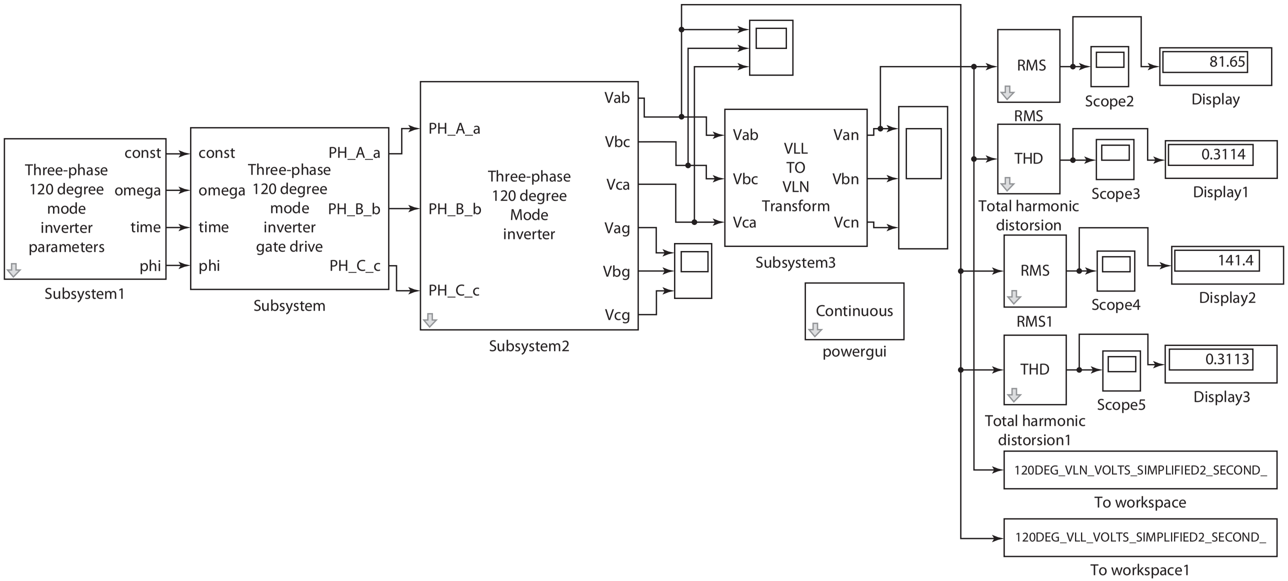
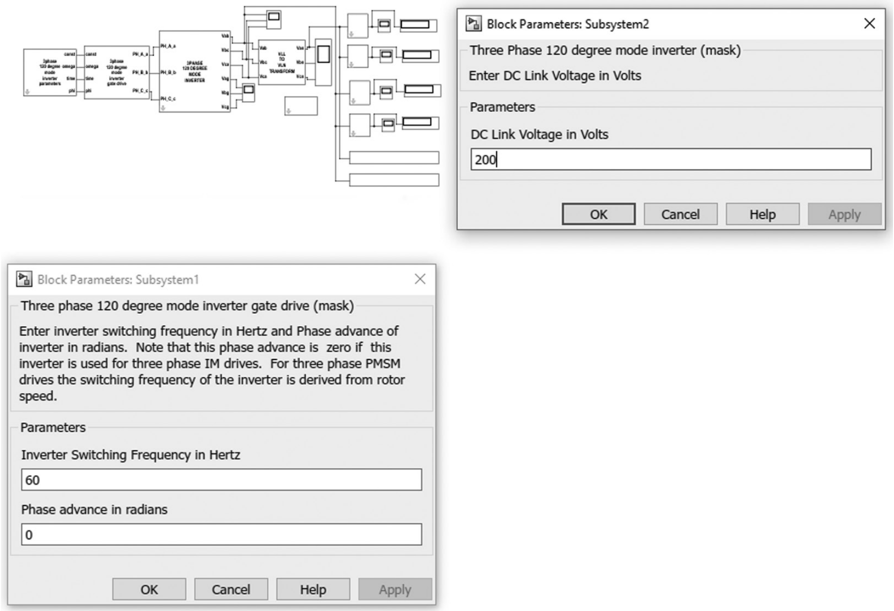

Three-phase
120 degree
mode
inverter
parameters
const
omega
time
phi
Subsystem1
const
omega
time
phi
Three-phase
120 degree
mode
inverter
gate drive
PH_A_a
PH_B_b
PH_C_c
Subsystem
PH_A_a
PH_B_b
PH_C_c
Three-phase
120 degree
Mode
inverter
Vab
Vbc
Vca
Vag
Vbg
Vcg
Subsystem2
Vab
Vbc
Vca
VLL
TO
VLN
Transform
Van
Vbn
Vcn
Subsystem3
Continuous
powergui
RMS
RMS
Scope2
81.65
Display
THD
Total harmonic
distorsion
Scope3
0.3114
Display1
RMS
RMS1
Scope4
141.4
Display2
THD
Total harmonic
distorsion1
Scope5
0.3113
Display3
120DEG_VLN_VOLTS_SIMPLIFIED2_SECOND_
To workspace
120DEG_VLL_VOLTS_SIMPLIFIED2_SECOND_
To workspace1

**FIGURE 4.19**
Three-phase 120° mode inverter.


3phase 120 degree mode inverter parameters
const
omega
time
phi
3phase 120 degree mode inverter gate drive
PH_A_a
PH_B_b
PH_C_c
3PHASE 120 DEGREE MODE INVERTER
Vab
Vbc
Vca
Vag
Vbg
Vcg
VLL TO VLN TRANSFORM
Van
Vbn
Vcn

Block Parameters: Subsystem2

Three Phase 120 degree mode inverter (mask)

Enter DC Link Voltage in Volts

Parameters

DC Link Voltage in Volts

200

OK
Cancel
Help
Apply

Block Parameters: Subsystem1

Three phase 120 degree mode inverter gate drive (mask)

Enter inverter switching frequency in Hertz and Phase advance of inverter in radians. Note that this phase advance is zero if this inverter is used for three phase IM drives. For three phase PMSM drives the switching frequency of the inverter is derived from rotor speed.

Parameters

Inverter Switching Frequency in Hertz

60

Phase advance in radians

0

OK
Cancel
Help
Apply

**FIGURE 4.20**
Three-phase 120° mode inverter with interactive blocks.

The line-to-line to line-to-neutral voltage transformation block is shown in Figure 4.21d. The three line-to-line voltages $V_{ry}$, $V_{yb}$ and $V_{br}$ are passed to a Matrix Gain block using a three-input mux. The gain matrix $K$ of the Matrix Gain block is defined by Equation 4.31. The three-phase line-to-neutral voltages $V_{rn}$, $V_{yn}$ and $V_{bn}$ are obtained at the output of the demux block.

Apart from this, the RMS and THD blocks from the Power Systems block set are used to measure the RMS value and THD of the line-to-line and line-to-ground voltages. Scopes are used to display the three-phase line-to-ground, line-to-line and line-to-neutral voltages. The Powergui from the Power Systems block set is used for harmonic analysis of the line-to-line and line-to-neutral voltages.

### 4.3.5 Simulation Results

A simulation of the model of the three-phase 120° mode inverter was carried out using the ode23t (mod. stiff/trapezoidal) solver. The DC link voltage and frequency entered were 200 V and 60 Hz, respectively. The three-phase line-to-ground voltages, line-to-line voltages and line-to-neutral voltages are shown in Figure 4.22a to c, Figures 4.23a to c and 4.24a to c, respectively. The RMS and THD values of the line-to-line voltages are shown in Figure 4.25a and b and those corresponding to the line-to-neutral voltages are shown in Figure 4.26a and b, respectively. The harmonic spectrum of the line-to-line

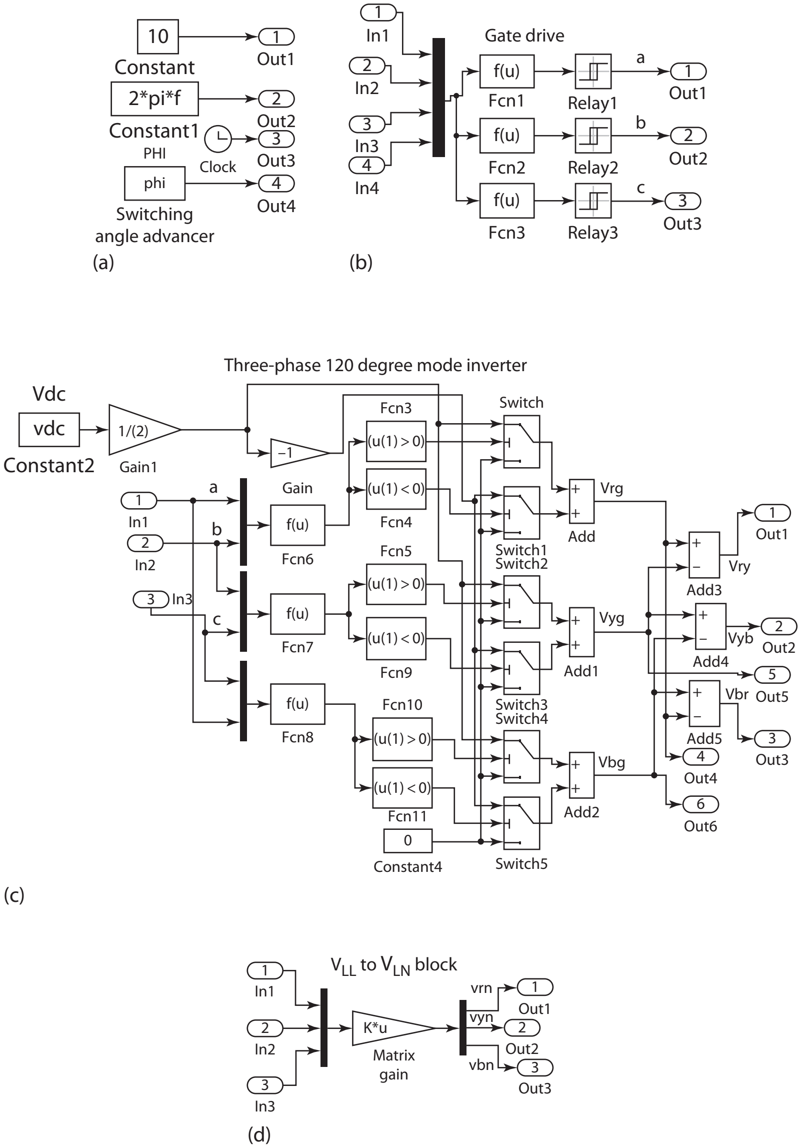

10
Constant
1
Out1
2*pi*f
2
Out2
Constant1
PHI
3
Out3
Clock
phi
4
Out4
Switching angle advancer
(a)
1
In1
2
In2
3
In3
4
In4
Gate drive
f(u)
Fcn1
Relay1
a
Out1
f(u)
Fcn2
Relay2
b
Out2
f(u)
Fcn3
Relay3
c
Out3
(b)
Three-phase 120 degree mode inverter
Vdc
vdc
Constant2
1/(2)
Gain1
−1
Gain
Fcn3
(u(1) > 0)
(u(1) < 0)
Fcn4
Fcn5
(u(1) > 0)
(u(1) < 0)
Fcn9
Fcn10
(u(1) > 0)
(u(1) < 0)
Fcn11
0
Constant4
a
b
c
1
In1
2
In2
3
In3
f(u)
Fcn6
f(u)
Fcn7
f(u)
Fcn8
Switch
Switch1
Switch2
Switch3
Switch4
Switch5
Add
Vrg
Add1
Vyg
Add2
Vbg
Add3
Vry
Add4
Vyb
Add5
Vbr
1
Out1
2
Out2
3
Out3
4
Out4
5
Out5
6
Out6
(c)
$V_{LL}$ to $V_{LN}$ block
1
In1
2
In2
3
In3
K*u
Matrix gain
vrn
vyn
vbn
1
Out1
2
Out2
3
Out3
(d)

**FIGURE 4.21**
(a–d) Three-phase 120° mode inverter subsystems.

voltages is shown in Figure 4.27a and b and that corresponding to the line-to-neutral voltages is shown in Figure 4.28a and b, respectively. These simulation results are also tabulated in Table 4.3. The theoretically calculated values for the THD and RMS values of the line-to-line and line-to-neutral voltages using Equations 4.23, 4.24, 4.32, 4.35, 4.36 and 4.37 are tabulated in Table 4.4.

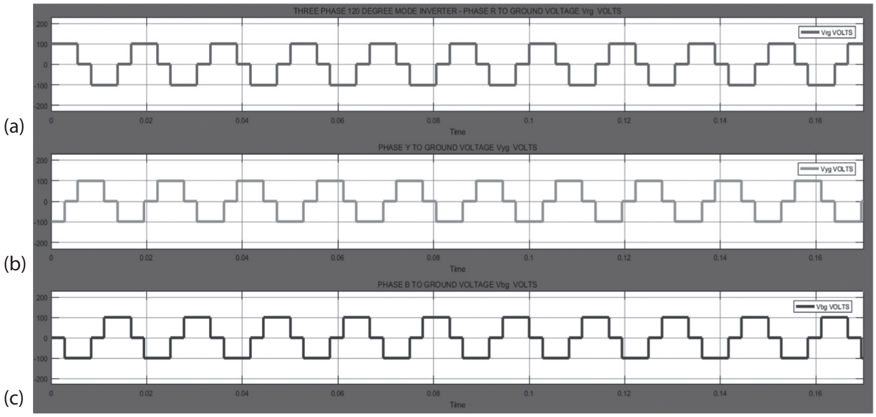


**FIGURE 4.22**
Three-phase 120° mode inverter. (a) Phase R to ground voltage $V_{rg}$ V. (b) Phase Y to ground voltage $V_{yg}$ V. (c) Phase B to ground voltage $V_{bg}$ V.

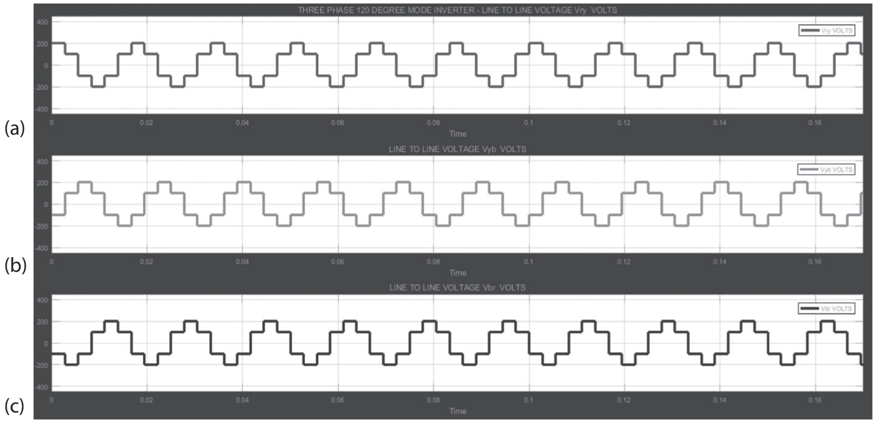


**FIGURE 4.23**
Three-phase 120° mode inverter. (a) Line-to-line voltage $V_{ry}$ V. (b) Line-to-line voltage $V_{yb}$ V. (c) Line-to-line voltage $V_{br}$ V.

## 4.4 Three-Phase Sine PWM Technique

Many industrial applications require voltage control of inverters to maintain constant output voltage irrespective of variations in the input DC voltage and for constant voltage and frequency control requirements. This is achieved by PWM, commonly known as *pulse width modulation (PWM) technique* [1–4].

The sine PWM is the most fundamental and widely used technique for voltage control of inverters. The principle of generation of the gating pulse for a three-phase sine PWM inverter using op-amps is shown in Figure 4.29a,

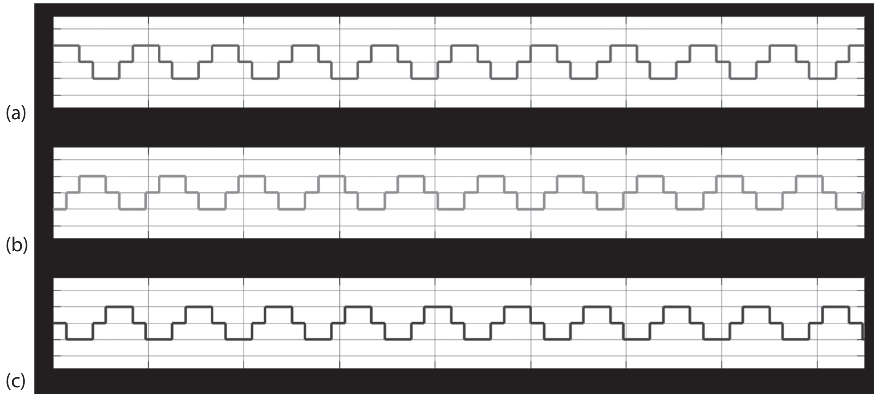


**FIGURE 4.24**
(a–c) Three-phase 120° mode inverter – line to neutral voltage in volts.

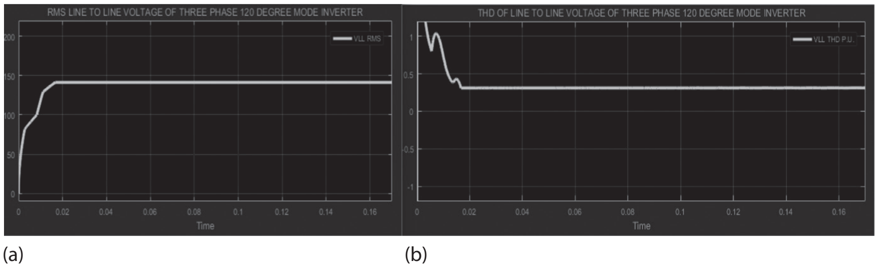


**FIGURE 4.25**
(a) RMS and (b) THD of line-to-line voltage of three-phase 120° mode inverter.

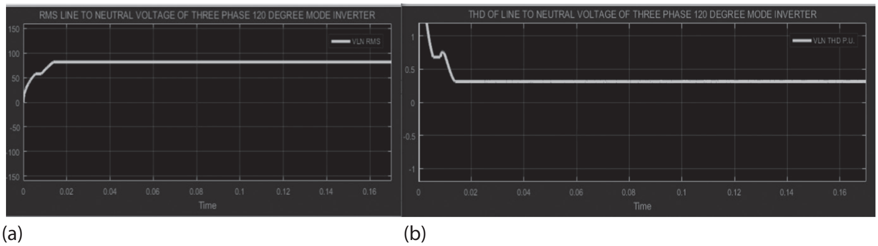
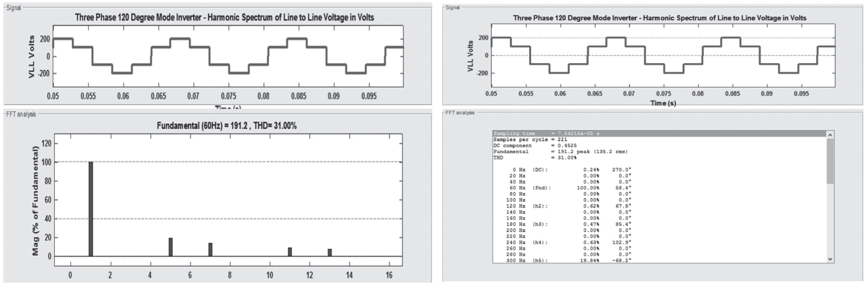


**FIGURE 4.26**
(a) RMS and (b) THD of line-to-neutral voltage of three-phase 120° mode inverter.

using Microcap 11. Three-phase AC modulating signals at the switching frequency of $f_m$ Hz of the inverter is generated. This three-phase modulating signal is compared with the triangular carrier wave of frequency $f_C$ Hz in a comparator, and the resulting pulse width modulated output pulse and its respective inverted pulse are used to drive the semiconductor switches in each phase of the three-phase inverter. The three-phase 50 Hz AC sine modulating signal, triangular carrier signal of frequency 2 kHz and the resulting

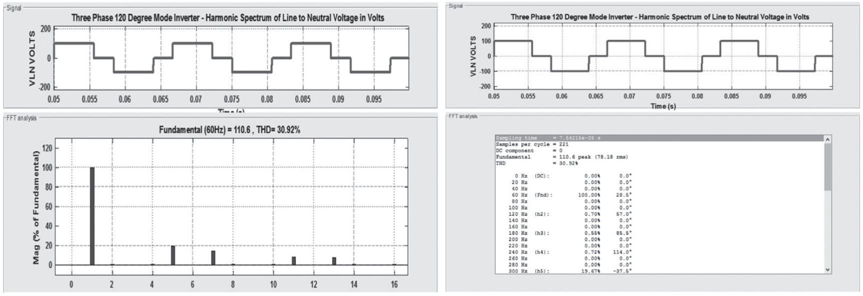


```
Sampling time     = 7.54215e-05 s
Samples per cycle = 221
DC component      = 0.4525
Fundamental       = 191.2 peak (135.2 rms)
THD               = 31.00%

     0 Hz  (DC):          0.24%    270.0°
    20 Hz                 0.00%      0.0°
    40 Hz                 0.00%      0.0°
    60 Hz  (Fnd):       100.00%     58.4°
    80 Hz                 0.00%      0.0°
   100 Hz                 0.00%      0.0°
   120 Hz  (h2):          0.62%     67.8°
   140 Hz                 0.00%      0.0°
   160 Hz                 0.00%      0.0°
   180 Hz  (h3):          0.47%     85.4°
   200 Hz                 0.00%      0.0°
   220 Hz                 0.00%      0.0°
   240 Hz  (h4):          0.63%    102.9°
   260 Hz                 0.00%      0.0°
   280 Hz                 0.00%      0.0°
   300 Hz  (h5):         19.84%    -68.2°
```

(a) (b)

**FIGURE 4.27**
(a,b) Three-phase 120° mode inverter: harmonic spectrum of line-to-line voltage in volts.



```
Sampling time     = 7.54215e-05 s
Samples per cycle = 221
DC component      = 0
Fundamental       = 110.6 peak (78.18 rms)
THD               = 30.92%

     0 Hz  (DC):          0.00%      0.0°
    20 Hz                 0.00%      0.0°
    40 Hz                 0.00%      0.0°
    60 Hz  (Fnd):       100.00%     28.5°
    80 Hz                 0.00%      0.0°
   100 Hz                 0.00%      0.0°
   120 Hz  (h2):          0.70%     57.0°
   140 Hz                 0.00%      0.0°
   160 Hz                 0.00%      0.0°
   180 Hz  (h3):          0.55%     85.5°
   200 Hz                 0.00%      0.0°
   220 Hz                 0.00%      0.0°
   240 Hz  (h4):          0.72%    114.0°
   260 Hz                 0.00%      0.0°
   280 Hz                 0.00%      0.0°
   300 Hz  (h5):         19.67%    -37.5°
```

(a) (b)

**FIGURE 4.28**
(a,b) Three-phase 120° mode inverter: harmonic spectrum of line-to-neutral voltage in volts.

**TABLE 4.3**

Three-Phase 120° Mode Inverter: Simulation Results

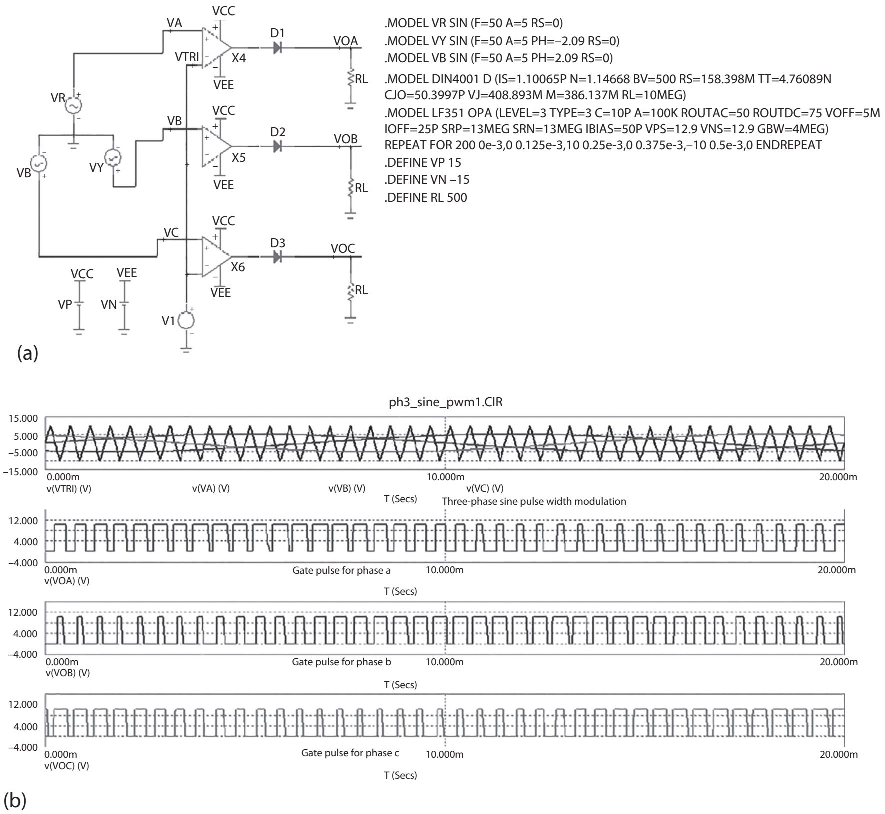
| Sl. No. | Frequency (Hz) | DC Link Voltage (V) | THD of $V_{LL}$ (Per Unit) | RMS $V_{LL}$ (V) | THD of $V_{LN}$ (Per Unit) | RMS $V_{LN}$ (V) |
|---|---|---|---|---|---|---|
| 1 | 60 | 200 | 0.3113 | 141.4 | 0.3114 | 81.65 |

**TABLE 4.4**

Three-Phase 120° Mode Inverter: Calculated Values

| Sl. No. | Frequency (Hz) | DC Link Voltage (V) | THD of $V_{LL}$ (Per Unit) | RMS $V_{LL}$ (V) | THD of $V_{LN}$ (Per Unit) | RMS $V_{LN}$ (V) |
|---|---|---|---|---|---|---|
| 1 | 60 | 200 | 0.309 | 141.44 | 0.309 | 81.66 |

gate pulse drive for the three-phase inverter are shown in Figure 4.29b by simulation using Microcap 11. The three-phase inverter frequency output will be 50 Hz. If $A_m$ and $A_C$ are the peak values of the sine modulating signal and the triangle carrier and their respective frequencies are $f_m$ and $f_C$,



```
.MODEL VR SIN (F=50 A=5 RS=0)
.MODEL VY SIN (F=50 A=5 PH=–2.09 RS=0)
.MODEL VB SIN (F=50 A=5 PH=2.09 RS=0)
.MODEL DIN4001 D (IS=1.10065P N=1.14668 BV=500 RS=158.398M TT=4.76089N
CJO=50.3997P VJ=408.893M M=386.137M RL=10MEG)
.MODEL LF351 OPA (LEVEL=3 TYPE=3 C=10P A=100K ROUTAC=50 ROUTDC=75 VOFF=5M
IOFF=25P SRP=13MEG SRN=13MEG IBIAS=50P VPS=12.9 VNS=12.9 GBW=4MEG)
REPEAT FOR 200 0e-3,0 0.125e-3,10 0.25e-3,0 0.375e-3,–10 0.5e-3,0 ENDREPEAT
.DEFINE VP 15
.DEFINE VN –15
.DEFINE RL 500
```

VCC
VA
VTRI
X4
VEE
D1
VOA
RL
VR
VB
VY
VB
VCC
X5
VEE
D2
VOB
RL
VC
VCC
X6
VEE
D3
VOC
RL
VCC
VEE
VP
VN
V1
(a)
ph3_sine_pwm1.CIR
15.000
5.000
–5.000
–15.000
0.000m
10.000m
20.000m
v(VTRI) (V)
v(VA) (V)
v(VB) (V)
v(VC) (V)
T (Secs)
Three-phase sine pulse width modulation
12.000
4.000
–4.000
0.000m
Gate pulse for phase a
10.000m
20.000m
v(VOA) (V)
T (Secs)
12.000
4.000
–4.000
0.000m
Gate pulse for phase b
10.000m
20.000m
v(VOB) (V)
T (Secs)
12.000
4.000
–4.000
0.000m
Gate pulse for phase c
10.000m
20.000m
v(VOC) (V)
T (Secs)
(b)

**FIGURE 4.29**
(a) Three-phase sine PWM and (b) gate pulse for three-phase sine PWM inverter.

then amplitude modulation and frequency modulation indices $M$ and $FM$ are defined as shown here:

$$M = \frac{A_m}{A_C} \tag{4.38}$$

$$FM = \frac{f_C}{f_m} \tag{4.39}$$

The region where $0 < M \leq 1$ is called the *linear region* or *undermodulation region*, and the region where $M > 1$ is called the *overmodulation region*. In the linear region, the maximum value of the fundamental component of the output line-to-line voltage $v_{ab1}$ can be expressed as given in Equation 4.40:

$$v_{ab1} = \frac{M.\sqrt{3}.V_{dc}}{2} \quad \text{for} \quad M \le 1 \tag{4.40}$$

where $V_{dc}$ is the DC link input voltage of the three-phase inverter.

In the overmodulation region, the maximum value of the *n*th harmonic component of the line-to-line voltage output of the three-phase inverter is given by Equation 4.41:

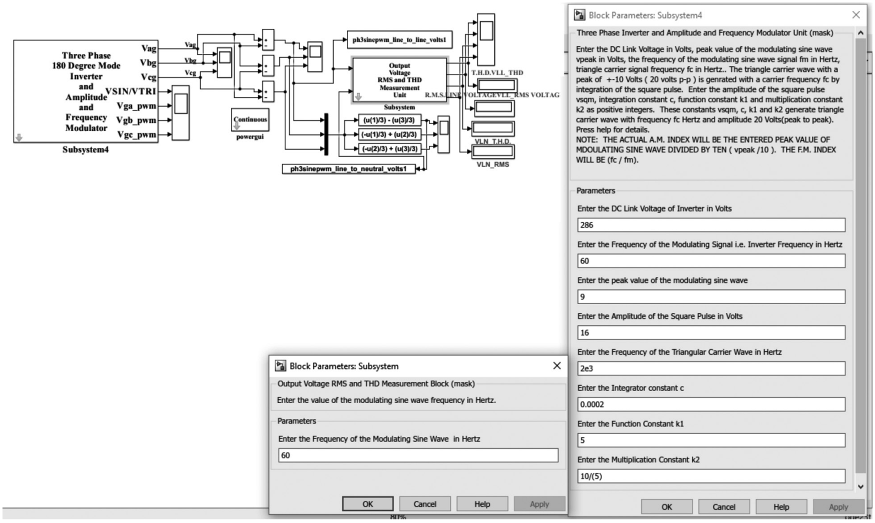
$$v_{abn} = \frac{4.\sqrt{3}.V_{dc}}{2.n.\pi} \quad \text{for} \quad M > 1 \tag{4.41}$$

Thus, by varying the value of *M*, the output voltage of the three-phase inverter can be controlled.

### 4.4.1 Model for Three-Phase Sine PWM Inverter

The model for the three-phase sine PWM inverter with interactive blocks is shown in Figure 4.30 [7,8]. The various dialogue boxes are shown in Figure 4.30. The various subsystem detailed schematics are shown in Figure 4.31a to e. The various subsystems are explained as follows:

The three subsystems 'Switching Function Generator', 'Three-Phase Sine PWM Generator' and 'Three-Phase VSI' in Figure 4.31a correspond to the dialogue box 'Three-Phase Inverter and Amplitude and Frequency Modulator Unit' and its model subsystems shown in Figure 4.31b to d. In Figure 4.31b, the three-phase AC with amplitude 1 V and frequency $f_m$ (60 Hz) of the sine-wave


Three Phase
180 Degree Mode
Inverter
and
Amplitude
and
Frequency
Modulator
Vag
Vbg
Vcg
VSIN/VTRI
Vga_pwm
Vgb_pwm
Vgc_pwm
Subsystem4
Vag
Vbg
Vcg
Continuous
powergui
ph3sinepwm_line_to_line_volts1
Output
Voltage
RMS and THD
Measurement
Unit
Subsystem
T.H.D.VLL_THD
R.M.S.LINE VOLTAGEVLL_RMS VOLTAG
(u(1)/3) - (u(3)/3)
(-u(1)/3) + (u(2)/3)
(-u(2)/3) + (u(3)/3)
VLN_T.H.D.
VLN_RMS
ph3sinepwm_line_to_neutral_volts1
OK
Cancel
Help
Apply
OK
Cancel
Help
Apply

Block Parameters: Subsystem

Output Voltage RMS and THD Measurement Block (mask)

Enter the value of the modulating sine wave frequency in Hertz.

Parameters

Enter the Frequency of the Modulating Sine Wave  in Hertz

60

Block Parameters: Subsystem4

Three Phase Inverter and Amplitude and Frequency Modulator Unit (mask)

Enter the DC Link Voltage in Volts, peak value of the modulating sine wave vpeak in Volts, the frequency of the modulating sine wave signal fm in Hertz, triangle carrier signal frequency fc in Hertz.. The triangle carrier wave with a peak of  +-10 Volts ( 20 volts p-p ) is genrated with a carrier frequency fc by integration of the square pulse.  Enter the amplitude of the square pulse vsqm, integration constant c, function constant k1 and multiplication constant k2 as positive integers.  These constants vsqm, c, k1 and k2 generate triangle carrier wave with frequency fc Hertz and amplitude 20 Volts(peak to peak).
Press help for details.
NOTE:  THE ACTUAL A.M. INDEX WILL BE THE ENTERED PEAK VALUE OF MDOULATING SINE WAVE DIVIDED BY TEN ( vpeak /10 ).  THE F.M. INDEX WILL BE (fc / fm).

Parameters

Enter the DC Link Voltage of Inverter in Volts

286

Enter the Frequency of the Modulating Signal i.e. Inverter Frequency in Hertz

60

Enter the peak value of the modulating sine wave

9

Enter the Amplitude of the Square Pulse in Volts

16

Enter the Frequency of the Triangular Carrier Wave in Hertz

2e3

Enter the Integrator constant c

0.0002

Enter the Function Constant k1

5

Enter the Multiplication Constant k2

10/(5)

**FIGURE 4.30**
Model of three-phase sine PWM inverter with interactive blocks.

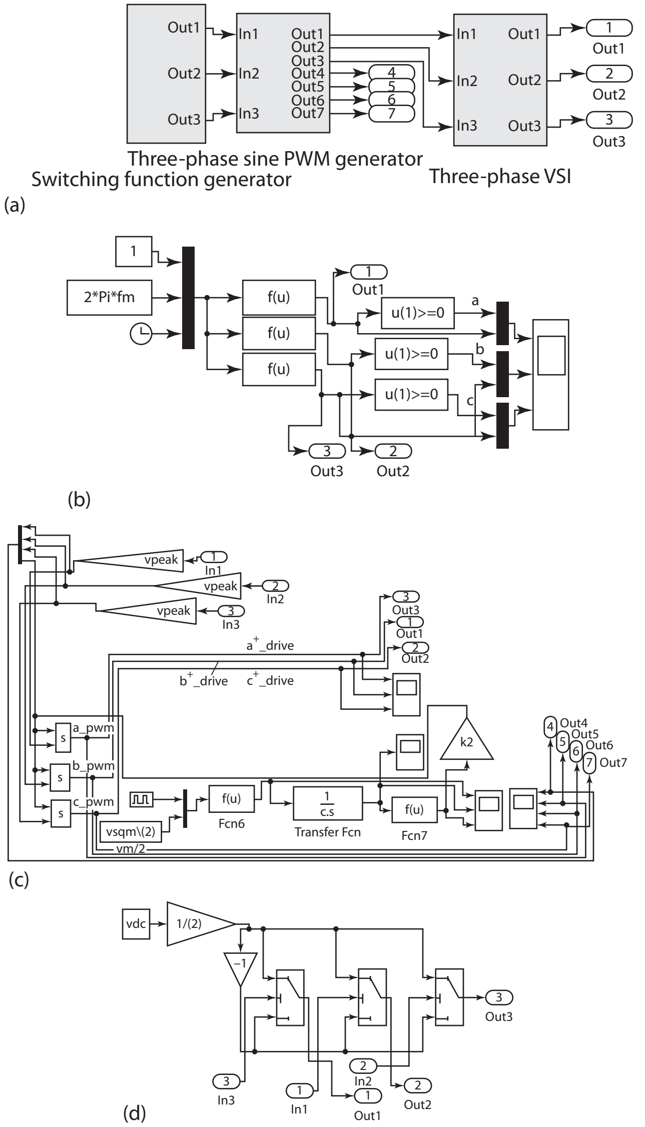
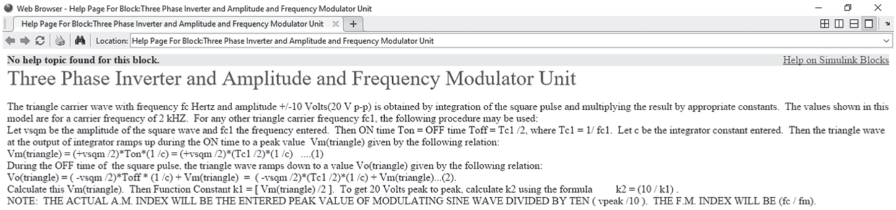

Out1
Out2
Out3
In1
In2
In3
Out1
Out2
Out3
Out4
Out5
Out6
Out7
4
5
6
7
In1
In2
In3
Out1
Out2
Out3
1
Out1
2
Out2
3
Out3
Three-phase sine PWM generator
Switching function generator
Three-phase VSI
(a)
1
2*Pi*fm
f(u)
f(u)
f(u)
1
Out1
u(1)>=0
u(1)>=0
u(1)>=0
a
b
c
3
Out3
2
Out2
(b)
vpeak
1
In1
vpeak
2
In2
vpeak
3
In3
3
Out3
1
Out1
2
Out2
a+_drive
b+_drive
c+_drive
s
a_pwm
s
b_pwm
s
c_pwm
vsqm\(2)
vm/2
f(u)
Fcn6
1
c.s
Transfer Fcn
f(u)
Fcn7
k2
4 Out4
5 Out5
6 Out6
7 Out7
(c)
vdc
1/(2)
−1
3
Out3
2
In2
2
Out2
3
In3
1
In1
1
Out1
(d)

**FIGURE 4.31**
(a–e) Three-phase sine PWM inverter model subsystems.

modulating signal is generated using three Fcn blocks connected to the mux. The three-phase AC output of this sine-wave modulating signal is passed to three Gain blocks with gain $v_{peak}$ in Figure 4.31c. The output of these three Gain blocks are three-phase sine-wave modulating signals with a peak value of $v_{peak}$. The triangle carrier wave of frequency $f_C$ (2 kHz) is generated by integration of the square pulse whose amplitude is $V_{sqm}$ and frequency $f_C$ Hz. The Fcn6 block


Web Browser - Help Page For Block:Three Phase Inverter and Amplitude and Frequency Modulator Unit
Help Page For Block:Three Phase Inverter and Amplitude and Frequency Modulator Unit
Location: Help Page For Block:Three Phase Inverter and Amplitude and Frequency Modulator Unit
Help on Simulink Blocks

**No help topic found for this block.**

Three Phase Inverter and Amplitude and Frequency Modulator Unit

The triangle carrier wave with frequency fc Hertz and amplitude +/-10 Volts(20 V p-p) is obtained by integration of the square pulse and multiplying the result by appropriate constants. The values shown in this model are for a carrier frequency of 2 kHZ. For any other triangle carrier frequency fc1, the following procedure may be used:
Let vsqm be the amplitude of the square wave and fc1 the frequency entered. Then ON time Ton = OFF time Toff = Tc1 /2, where Tc1 = 1/ fc1. Let c be the integrator constant entered. Then the triangle wave at the output of integrator ramps up during the ON time to a peak value Vm(triangle) given by the following relation:
Vm(triangle) = (+vsqm /2)*Ton*(1 /c) = (+vsqm /2)*(Tc1 /2)*(1 /c) ....(1)
During the OFF time of the square pulse, the triangle wave ramps down to a value Vo(triangle) given by the following relation:
Vo(triangle) = ( -vsqm /2)*Toff * (1 /c) + Vm(triangle) = ( -vsqm /2)*(Tc1 /2)*(1 /c) + Vm(triangle)...(2).
Calculate this Vm(triangle). Then Function Constant k1 = [ Vm(triangle) /2 ]. To get 20 Volts peak to peak, calculate k2 using the formula k2 = (10 / k1) .
NOTE: THE ACTUAL A.M. INDEX WILL BE THE ENTERED PEAK VALUE OF MODULATING SINE WAVE DIVIDED BY TEN ( vpeak /10 ). THE F.M. INDEX WILL BE (fc / fm).

(e)

**FIGURE 4.31 (CONTINUED)**
(a–e) Three-phase sine PWM inverter model subsystems.

subtracts this square pulse from $V_{sqm}/2$ generating square wave with positive and negative peaks of $+V_{sqm}/2$ and $-V_{sqm}/2$, respectively. This is then multiplied by a constant of integration $1/c$ to obtain a triangle carrier wave with a maximum value of $+V_m$(triangle) and minimum value of zero. This triangle carrier wave is then subtracted from the constant $k1$ to obtain a triangle carrier wave with positive and negative peaks of $+V_m$(triangle)/2 and $-V_m$(triangle)/2, respectively, using the Fcn7 block. The value of $k1$ is $+V_m$(triangle)/2. The output of the Fcn7 block is then multiplied by $k2$ to obtain a triangle carrier wave with positive and negative peaks of +10 V and –10 V, respectively. The value of $k2$ is $10/k1$. The values shown in the dialogue box are to generate a carrier wave of 2 kHz frequency. For any other frequency of the carrier wave, the method shown in Figure 4.31e can be used. The values relating to the DC link voltage of the three-phase inverter, modulating signal frequency (i.e. inverter frequency), amplitude of the modulating signal $v_{peak}$, $V_{sqm}$, $f_C$, $c$, $k1$ and $k2$ are entered in the appropriate box. The amplitude modulation index $M$ is the value entered of the sine modulating signal peak value, $v_{peak}/10$. This triangle carrier wave and the three-phase modulating sine-wave AC are compared in the three relational operator blocks used as comparators. The three comparators output the three-phase gating pulses *a_pwm*, *b_pwm* and *c_pwm* for the three-phase inverter. Figure 4.31d shows the model of the three-phase inverter. The gating pulses *a_pwm*, *b_pwm* and *c_pwm* are passed to the $u(2)$ input of three threshold switches. The $u(1)$ and $u(3)$ inputs to these three switches are the $+V_{dc}/2$ and $-V_{dc}/2$ inputs. The threshold value for these three switches is 0.5. When the respective $u(2)$ input of these three switches becomes logic 1, the output is $+V_{dc}/2$, and when it is logic 0, the output is $-V_{dc}/2$. Thus, three-phase line-to-ground voltage is generated.

### 4.4.2 Simulation Results

A system model simulation of the three-phase sine PWM inverter was carried out for an amplitude modulation index $M$ of 0.9 in the undermodulation region and for an index $M$ of 1.1 in the overmodulation region. The DC link voltage was 286 V. The sine modulating signal frequency was 60 Hz and the triangle carrier frequency was 2 kHz. The simulation results for $M = 0.9$ are shown in Figure 4.32 and the harmonic spectrum of the line-to-line and line-to-neutral voltages in

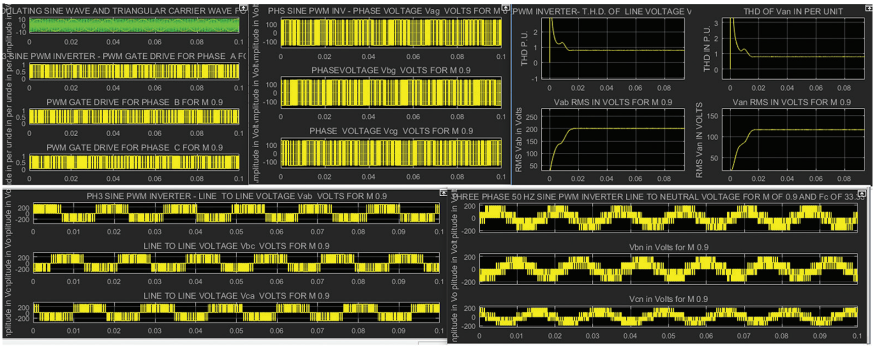

LATING SINE WAVE AND TRIANGULAR CARRIER WAVE F
INE PWM INVERTER - PWM GATE DRIVE FOR PHASE A F
PWM GATE DRIVE FOR PHASE B FOR M 0.9
PWM GATE DRIVE FOR PHASE C FOR M 0.9
PHS SINE PWM INV - PHASE VOLTAGE Vag VOLTS FOR M
PHASEVOLTAGE Vbg VOLTS FOR M 0.9
PHASE VOLTAGE Vcg VOLTS FOR M 0.9
PWM INVERTER- T.H.D. OF LINE VOLTAGE V
THD P.U.
Vab RMS IN VOLTS FOR M 0.9
RMS Vab in Volts
THD OF Van IN PER UNIT
THD IN P.U.
Van RMS IN VOLTS FOR M 0.9
RMS Van IN VOLTS
PH3 SINE PWM INVERTER - LINE TO LINE VOLTAGE Vab VOLTS FOR M 0.9
LINE TO LINE VOLTAGE Vbc VOLTS FOR M 0.9
LINE TO LINE VOLTAGE Vca VOLTS FOR M 0.9
HREE PHASE 50 HZ SINE PWM INVERTER LINE TO NEUTRAL VOLTAGE FOR M OF 0.9 AND Fc OF 33
Vbn in Volts for M 0.9
Vcn in Volts for M 0.9

**FIGURE 4.32**
Three-phase sine PWM inverter simulation results for $M=0.9$.

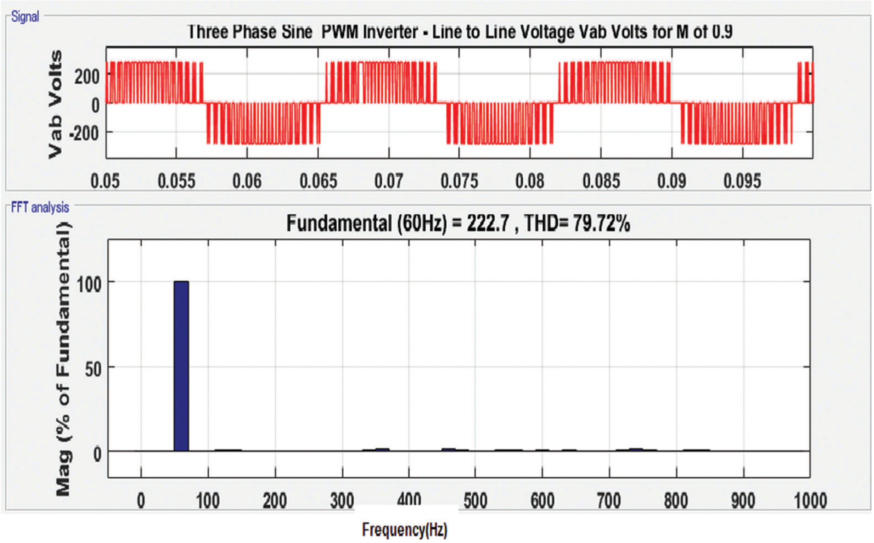


**FIGURE 4.33**
Three-phase sine PWM inverter: harmonic spectrum of line-to-line voltage for $M=0.9$.

Figures 4.33 and 4.34 respectively. The simulation results and harmonic spectrum for an amplitude modulation index of 1.1 are shown in Figures 4.35, 4.36 and 4.37, respectively. Simulation results are tabulated in Table 4.5.

## 4.5 Conclusions

For the three-phase 180° mode inverter, Tables 4.1 and 4.2 reveal that the THD of the line-to-line voltage and line-to-neutral voltage by simulation and calculation differ by a small percentage of 0.615% in both cases. The

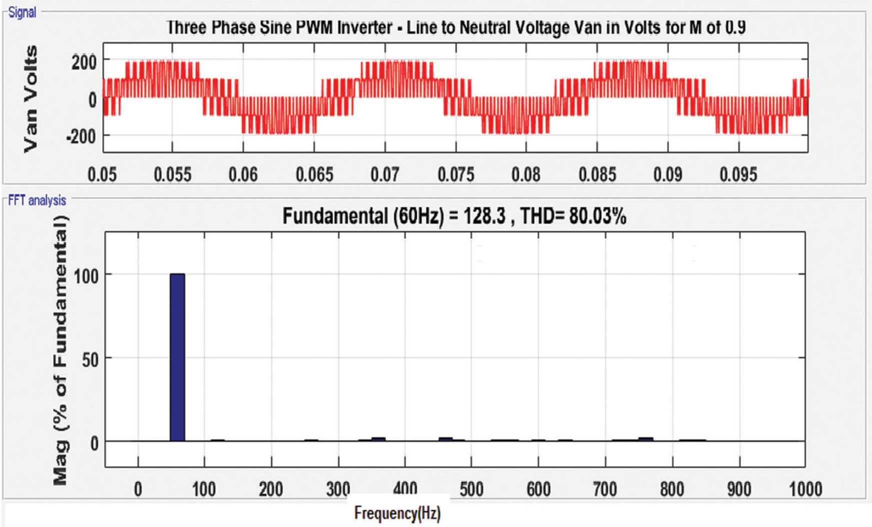


**FIGURE 4.34**
Three-phase sine PWM inverter: harmonic spectrum of line-to-neutral voltage for $M = 0.9$.

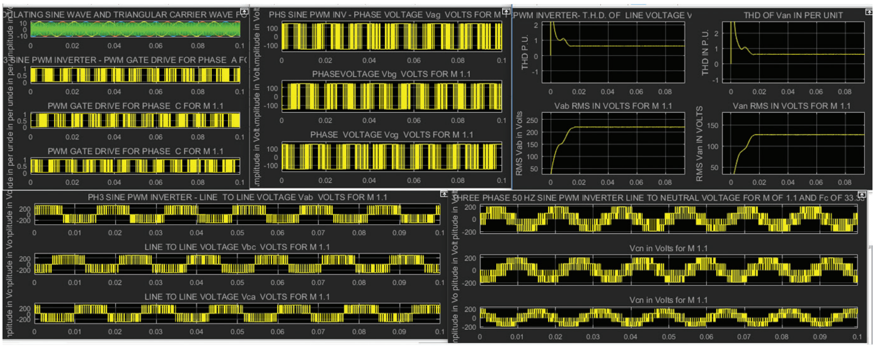

DULATING SINE WAVE AND TRIANGULAR CARRIER WAVE FO
3 SINE PWM INVERTER - PWM GATE DRIVE FOR PHASE A FC
PWM GATE DRIVE FOR PHASE C FOR M 1.1
PWM GATE DRIVE FOR PHASE C FOR M 1.1
PHS SINE PWM INV - PHASE VOLTAGE Vag VOLTS FOR M
PHASEVOLTAGE Vbg VOLTS FOR M 1.1
PHASE VOLTAGE Vcg VOLTS FOR M 1.1
PWM INVERTER- T.H.D. OF LINE VOLTAGE V
THD P.U.
THD OF Van IN PER UNIT
THD IN P.U.
Vab RMS IN VOLTS FOR M 1.1
RMS Vab in Volts
Van RMS IN VOLTS FOR M 1.1
RMS Van IN VOLTS
PH3 SINE PWM INVERTER - LINE TO LINE VOLTAGE Vab VOLTS FOR M 1.1
LINE TO LINE VOLTAGE Vbc VOLTS FOR M 1.1
LINE TO LINE VOLTAGE Vca VOLTS FOR M 1.1
THREE PHASE 50 HZ SINE PWM INVERTER LINE TO NEUTRAL VOLTAGE FOR M OF 1.1 AND Fc OF 33.33
Vcn in Volts for M 1.1
Vcn in Volts for M 1.1

**FIGURE 4.35**
Three-phase sine PWM inverter simulation results for $M = 1.1$.

difference in the RMS value for the line-to-line voltage and that for the line-to-neutral voltage by simulation and calculation is negligible. The simulation results in Table 4.3 for the model of three-phase 120° mode inverter reveals that the RMS values of the line-to-line and line-to-neutral voltages are close to the theoretically calculated values using the formula given in Table 4.4. The simulation result for the THD value of the line-to-line voltage differs by around 0.74% and that of the line-to-neutral voltage by around 0.776% compared with the theoretically calculated value. An interactive model for sine PWM of three-phase 180° mode inverter is also presented.

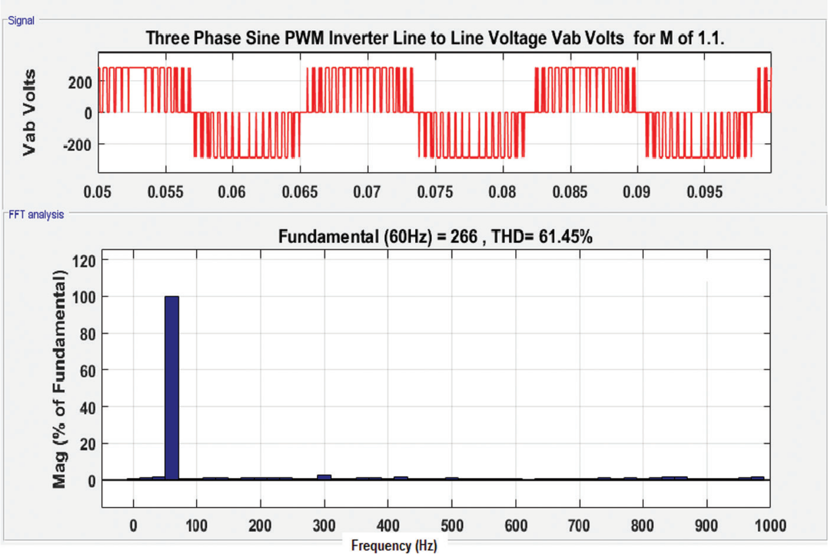


**FIGURE 4.36**
Three-phase sine PWM inverter: harmonic spectrum of line-to-line voltage for $M = 1.1$.

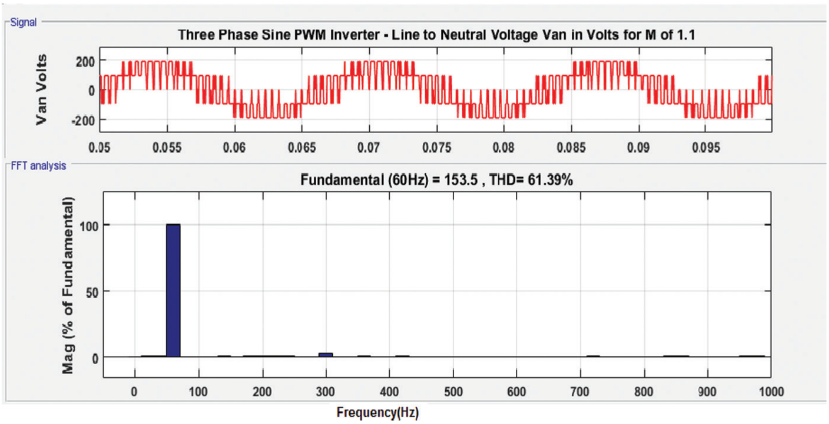


**FIGURE 4.37**
Three-phase sine PWM inverter: harmonic spectrum of line-to-neutral voltage for $M = 1.1$.

**TABLE 4.5**

Three-Phase Sine PWM Inverter: Simulation Results

| Sl. No. | DC Link Voltage (V) | Amplitude Modulation Index | RMS $V_{ab}$ (V) | THD $V_{ab}$ (Per Unit) | RMS $V_{an}$ (V) | THD $V_{an}$ (Per Unit) |
|---|---|---|---|---|---|---|
| 1 | 286 | 0.9 | 201.8 | 0.7923 | 116.3 | 0.7944 |
| 2 | 286 | 1.1 | 219.8 | 0.6134 | 126.6 | 0.6186 |

## References

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5. B.K. Lee and M. Ehsani: "A simplified functional model for 3-phase voltage source inverter using switching function concept"; *IEEE IECON '99*; San Jose, CA, November–December 1999, Vol.1, pp. 462–467.
6. B.K. Lee and M. Ehsani: "A simplified functional simulation model for three-phase voltage source inverter using switching function concept", *IEEE Transactions on Industrial Electronics*; Vol.48, No.2, April 2001; pp. 309–321.
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8. N.P.R. Iyer: "Matlab/Simulink modules for modelling and simulation of power electronic converters and electric drives", M.E. by research thesis, University of Technology Sydney, NSW, 2006, Chapter 4.

# 5

# *Interactive Models for DC to DC Converters*

## 5.1 Introduction

DC to DC converters are used for transforming the DC input voltage from one voltage level to the DC output voltage at another voltage level. There are three fundamental topologies for DC to DC converters, such as buck, boost and buck–boost converters. These are second-order converters, and have a semiconductor switch, a diode, one inductor, one capacitor and one load resistor and a DC input voltage source. Advanced converters, known as *fourth-order converters*, use a DC input voltage source, two inductors and two capacitors, along with one or more semiconductor switches, diodes and a load resistor. Fourth-order converters can be built by cascading any two second-order converter topologies. Additionally, Cuk, single-ended primary inductance converter (SEPIC), Zeta and Luo converters fall under the category of fourth-order converters. Buck converters find applications in switched mode power supplies, as is also the case with buck–boost converters. Boost converters are used for power factor improvement of AC–DC–AC converters used for AC drives. Cuk and SEPIC converters are used as power factor pre-regulators. These DC–DC converters are also used for charging mobile phones and laptops.

This chapter mainly deals with the interactive system modelling of fundamental topologies of second-order DC–DC converters such as buck, boost and buck–boost. The switching function concept is used to model these converters. The developed models are valid as long as the inductor current is continuous or the converter is in the continuous conduction mode (CCM) or the discontinuous conduction mode (DCM).

## 5.2 Buck Converter Analysis in Continuous Conduction Mode

The buck converter topology using a BJT switch is shown in Figure 5.1 [1–6]. This switch can be any one of MOSFET, IGBT or GTO. The switch is driven by an external pulse width modulation (PWM) drive whose period is *T* and

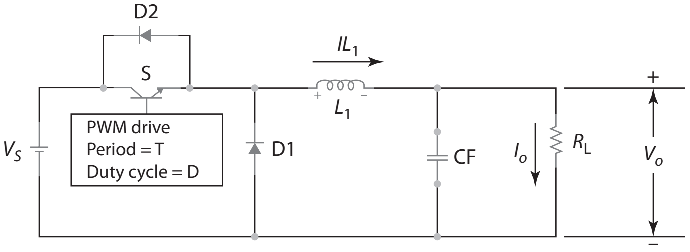


**FIGURE 5.1**
Buck converter.

duty cycle is $D$. Figure 5.2a,b shows the equivalent circuit of Figure 5.1 when the switch is ON from 0 to $DT$ s and OFF from $DT$ to $T$ s, respectively. This analysis assumes CCM, that is, the inductor current is continuous or always greater than zero. Noting that the change in inductor current during the ON time and OFF time is equal or the average inductor current over one switching cycle is zero, the following equation can be derived.

$$\frac{(V_S - V_O).D.T}{L_1} + \frac{(-V_O).(1-D).T}{L_1} = 0 \tag{5.1}$$

$$\frac{V_O}{V_S} = D \tag{5.2}$$

During the switch ON time, the inductor current grows linearly and reaches a maximum value $I_{L1\max}$ and during the switch OFF period, the inductor current decays and reaches a minimum value $I_{L1\min}$. The buck converter waveforms for the CCM operation are shown in Figure 5.3. Referring to Figure 5.3a, the average inductor current $I_{L1}$ can be expressed as follows:

$$\begin{aligned} I_{L1} &= \frac{1}{T} * \left[ \frac{T}{2} * (I_{L1\max} - I_{L1\min}) + T * I_{L1\min} \right] \\ &= \frac{1}{2} * (I_{L1\max} + I_{L1\min}) \end{aligned} \tag{5.3}$$

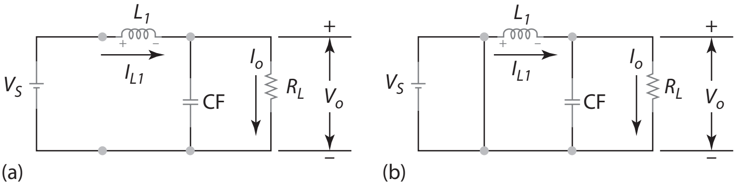


**FIGURE 5.2**
Buck converter equivalent circuits. (a) Switch ON for $0 < t \le D.T$ s. (b) Switch OFF for $D.T < t \le T$ s.

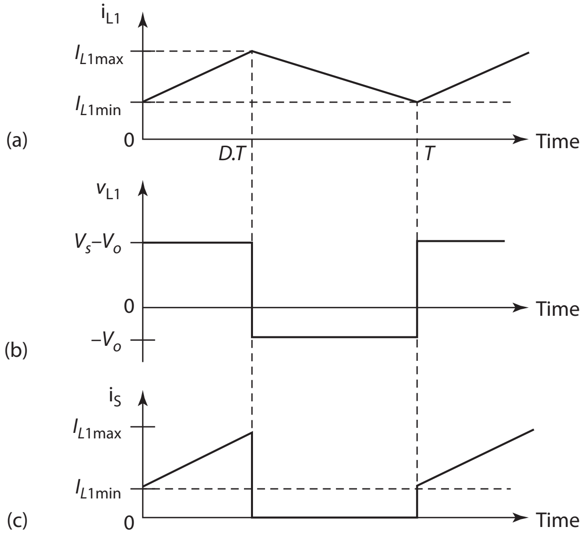


**FIGURE 5.3**
Buck converter waveforms in CCM. (a) Inductor current. (b) Inductor voltage. (c) Input current.

The inductor current during the switch ON and OFF intervals flows through the load resistor. The average load current $I_O$ is given here:

$$I_O = \frac{V_O}{R_L} = \frac{1}{2} * \left(I_{L1\max} + I_{L1\min}\right) \tag{5.4}$$

The maximum and minimum inductor currents are given by $I_{L1\max} = I_O + (\Delta i_{L1}/2)$ and $I_{L1\min} = I_O - (\Delta i_{L1}/2)$, respectively. The inductor current ripple is $\Delta i_{L1} = (V_S - V_O) * D.T/L_1$. Using Equation 5.2, the maximum and minimum inductor currents are given here:

$$\left.\begin{aligned} I_{L1\max} &= D.V_S * \left[\frac{1}{R_L} + \frac{(1-D) * T}{2L_1}\right] \\ I_{L1\min} &= D.V_S * \left[\frac{1}{R_L} - \frac{(1-D) * T}{2L_1}\right] \end{aligned}\right| \tag{5.5}$$

The critical inductance $L_{1\text{crit}}$ required to maintain CCM is obtained by equating $I_{L1\min}$ to zero. This gives the following value for $L_{1\text{crit}}$.

$$L_{1\text{crit}} = \frac{(1-D) * T * R_L}{2} \tag{5.6}$$

In this derivation, fsw = (1/$T$) is the switching frequency in hertz, $L_1$ is the inductor in henries and $R_L$ is the load resistor in ohms.

## 5.3 Buck Converter Analysis in Discontinuous Conduction Mode

In DCM, there exists a short interval of time during which the inductor current is zero. The equivalent circuit for the DCM operation of the buck converter is shown in Figure 5.4. Figure 5.4c corresponds to the DCM operation. The inductor current and inductor voltage waveforms for DCM operation are shown in Figure 5.5. The average inductor current over one switching cycle is zero. This can be expressed as shown:

$$\frac{(V_S - V_O) * D.T}{L_1} + \frac{-V_O * (D_1 - D).T}{L_1} = 0 \tag{5.7}$$

$$\frac{V_O}{V_S} = \frac{D}{D_1} \tag{5.8}$$

Referring to Figure 5.5a, using Equation 5.8, the average inductor current $I_{L1}$ is derived as follows:

$$\begin{aligned} I_{L1} &= \frac{1}{T} * \left[ \left( \frac{D_1 * T}{2} \right) * \left( \frac{V_O * (D_1 - D) * T}{L_1} \right) \right] \\ &= \frac{V_O * D_1 * (D_1 - D) * T}{2L_1} \\ &= \frac{V_O * (D_1^2 - D_1 * D) * T}{2L_1} \end{aligned} \tag{5.9}$$

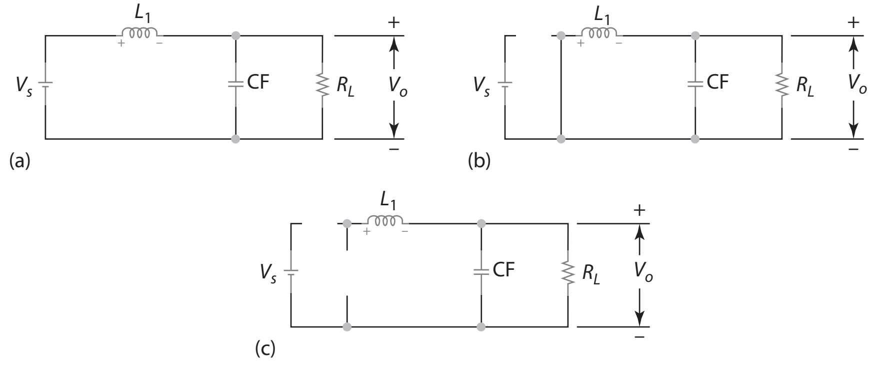


**FIGURE 5.4**
Buck converter equivalent circuits in DCM. (a) Switch ON. (b) Switch OFF. (c) Inductor current is zero.

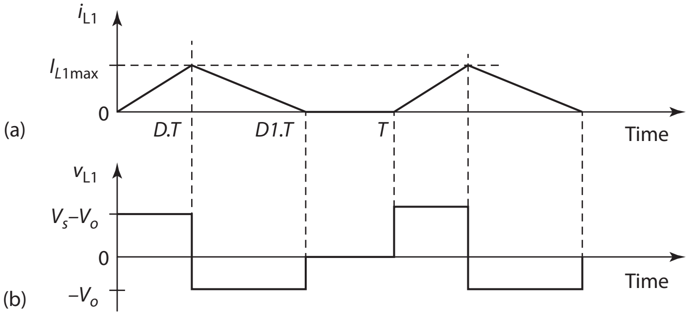


**FIGURE 5.5**
Buck converter waveforms in DCM. (a) Inductor current. (b) Inductor voltage.

Because the average inductor current $I_{L1}$ and the load current $I_O$ are equal, we have the following:

$$\frac{V_O}{R_L} = \frac{V_O * \left(D_1^2 - D_1 * D\right) * T}{2L_1} \tag{5.10}$$

Solving Equation 5.10, the value of $D_1$ and the voltage gain $V_O/V_S$ for DCM are given here:

$$\begin{aligned} D_1^2 - D_1.D - \frac{2.L_1}{R_L.T} &= \quad 0 \\ D_1 &= \frac{D}{2} \pm \sqrt{\frac{D^2}{4} + \frac{2.L_1}{R_L.T}} \end{aligned} \tag{5.11}$$

$$M = \frac{V_O}{V_S} = \frac{D}{\dfrac{D}{2} \pm \sqrt{\dfrac{D^2}{4} + \dfrac{2.L_1}{R_L.T}}} \tag{5.12}$$

Equations 5.11 and 5.12 give two values for $D_1$ and $M$, of which only one is valid.

## 5.4 Model of Buck Converter in CCM and DCM

Models for the buck converter are available in references [7–13]. The switching function concept is used to model the buck converter [7–13]. Buck converter model parameters are shown in Table 5.1. The development of the model is given as follows:

**TABLE 5.1**

Buck Converter Model Parameters

| Sl. No. | Input Voltage $V_S$ (V) | Switching Period $T$ (s) | Duty Cycle $D$ | Inductor $L_1$ (H) | Filter Capacitor $C_F$ (F) | Load Resistor $R_L$ (Ω) | Remarks |
|---|---|---|---|---|---|---|---|
| 1 | 12 | 0.2E−3 | 5/12 | 200E−6 | 47E−6 | 2.5 | CCM |
| 2 | 12 | 0.2E−3 | 5/12 | 50E−6 | 470E−6 | 2.5 | DCM |

Referring to Figures 5.2 and 5.4, the following equations can be derived for CCM and DCM operation.

$$\left.\begin{aligned} i_{L1\_dot} &= \frac{(V_S - V_O)}{L_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(-V_O)}{L_1} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{5.13}$$

Now, for the switch $S$, the switching function SF is defined as follows for CCM operation:

$$\left.\begin{aligned} \text{SF} &= 1 \quad \text{for} \quad 0 \le t \le D.T \\ &= 0 \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{5.14}$$

For the inductor current $i_{L1}$, another switch function SF_IL1 is defined:

$$\left.\begin{aligned} \text{SF\_IL1} &= 1 \quad \text{for} \quad i_{L1} \succ 0 \\ &= 0 \quad \text{for} \quad i_{L1} \succ 0 \end{aligned}\right| \tag{5.15}$$

Using Equations 5.14 and 5.15 in Equation 5.13, we have the following:

$$i_{L1\_dot} = \frac{(\text{SF} * V_S - \text{SF\_IL1} * V_O)}{L_1} \tag{5.16}$$

The inductor current flows through the load resistor during switch ON and OFF in CCM and in DCM until it falls to zero. The output voltage equation is formulated by observation of equivalent circuits for CCM and DCM (Figures 5.2 and 5.4), as follows:

$$I_{CF} = I_{L1} - I_O \tag{5.17}$$

$$v_{O\_dot} = \left( \frac{\text{SF\_IL1} * I_{L1}}{C_F} - \frac{V_O}{R_L * C_F} \right) \tag{5.18}$$

$$I_O = \frac{V_O}{R_L} \tag{5.19}$$

In Equations 5.16 and 5.18, $i_{L1\_dot}$ and $v_{O\_dot}$ represent $di_{L1}/dt$ and $dv_O/dt$, respectively. In Equation 5.17, $I_{CF}$ is the average filter current and $I_O$ is the load current.

The interactive model of the buck converter suitable for CCM and DCM operation is shown in Figure 5.6 with a dialogue box. The model subsystem is shown in Figure 5.7. The data in the dialogue box in Figure 5.6 corresponds to the CCM operation given in Table 5.1. The appropriate data for DCM operation given in Table 5.1 are entered in the dialogue box if DCM operation is required.

The switch function SF for the switch defined in Equation 5.14 is generated using the Pulse Generator block, whose amplitude is 1, pulse width 'd*100' (% of period) and switching period '1/(fsw)', where 'd' is the duty ratio and 'fsw' is the frequency of switching. The switch function for the inductor current SF_IL1 defined in Equation 5.15 is generated using the embedded MATLAB® function, whose input is IL1 and output is SF_IL1 as shown in Figure 5.7. Equations 5.16, 5.18 and 5.19 are solved using another embedded MATLAB function and integrators, as shown in Figure 5.7. The source code for the two embedded MATLAB functions are given here:

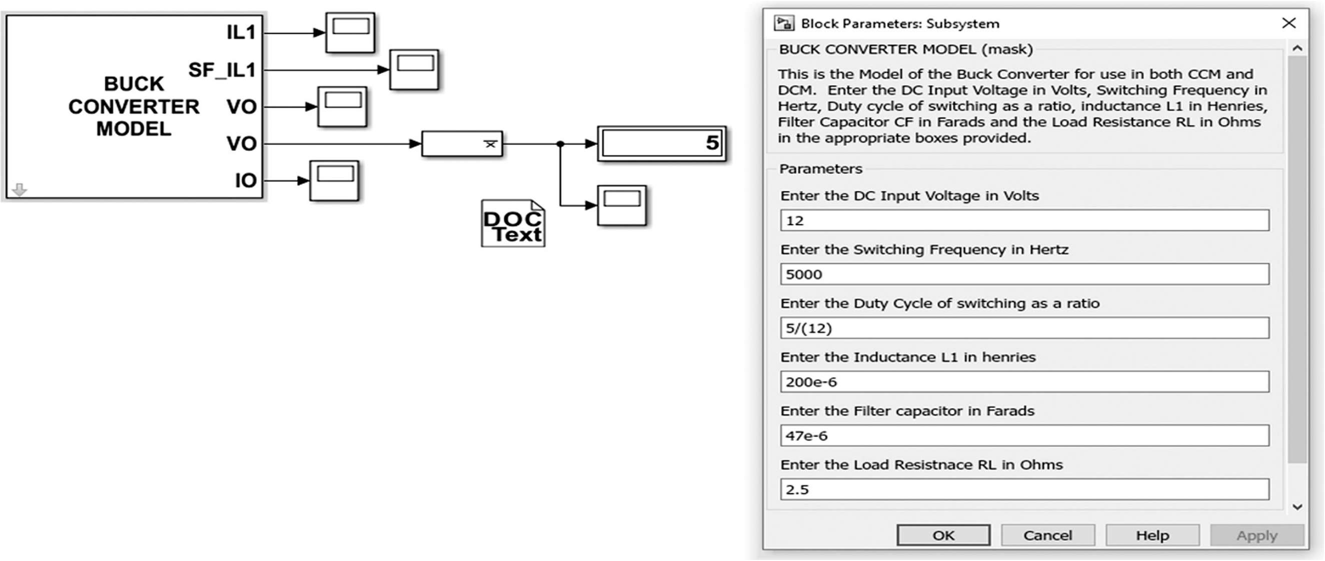
```
function [IL1_dot, VO_dot, IO] = fcn(SF,IL1,VO,VS,L1,CF,RL,SF_IL1)
IL1_dot = -SF_IL1*VO/(L1) + SF*VS/(L1);
VO_dot = SF_IL1*IL1/(CF) - VO/(RL*CF);
IO = VO/(RL);

function SF_IL1 = fcn(IL1)
if IL1 <= 0
    SF_IL1 = 0;
else
    SF_IL1 = 1;
End
```

The embedded MATLAB outputs $v_{o\_dot}$, $i_{L1\_dot}$ are integrated using Integrator blocks to obtain the required outputs and are used as feedback inputs along with SF_IL1 to solve Equations 5.16, 5.18 and 5.19.

### 5.4.1 Simulation Results

Simulation of the buck converter for CCM and DCM operations was carried out using Simulink® [14]. The ode23t (mod. stiff/trapezoidal) solver was used. The data shown in Table 5.1 were used for simulation. The simulation results for the buck converter in CCM are shown in Figure 5.8 and those for DCM are shown in Figure 5.9. Simulation results and calculated values are tabulated in Tables 5.2 and 5.3.



Block Parameters: Subsystem

BUCK CONVERTER MODEL (mask)

This is the Model of the Buck Converter for use in both CCM and DCM. Enter the DC Input Voltage in Volts, Switching Frequency in Hertz, Duty cycle of switching as a ratio, inductance L1 in Henries, Filter Capacitor CF in Farads and the Load Resistance RL in Ohms in the appropriate boxes provided.

Parameters

Enter the DC Input Voltage in Volts: 12

Enter the Switching Frequency in Hertz: 5000

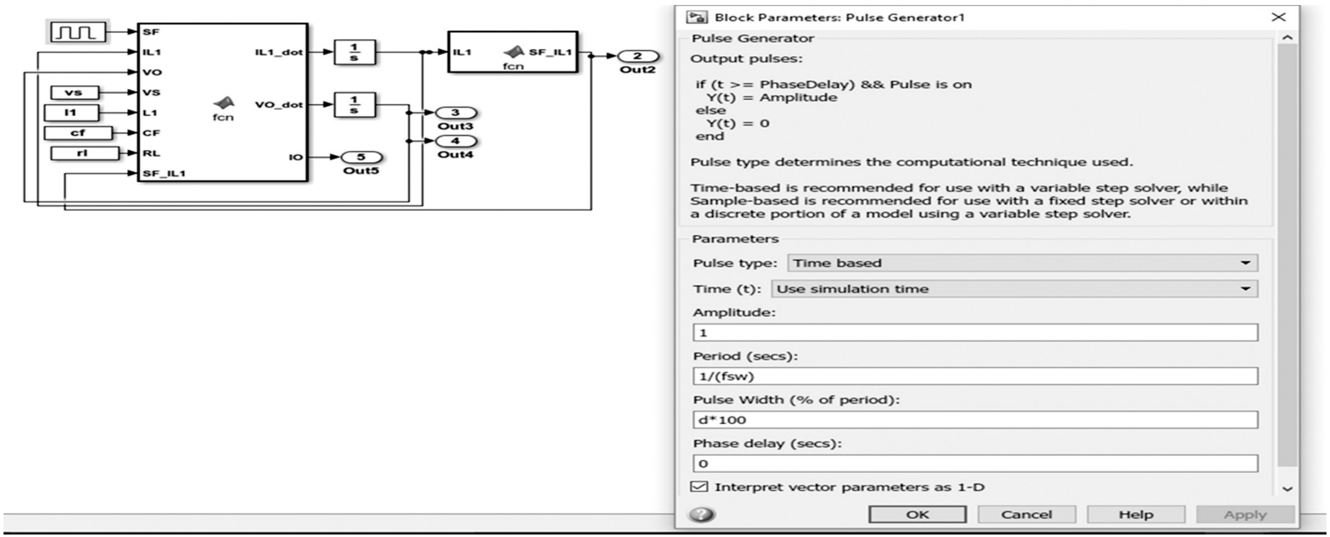
Enter the Duty Cycle of switching as a ratio: 5/(12)

Enter the Inductance L1 in henries: 200e-6

Enter the Filter capacitor in Farads: 47e-6

Enter the Load Resistnace RL in Ohms: 2.5

**FIGURE 5.6**
Model of buck converter in CCM and DCM.


SF
IL1
VO
VS
L1
CF
RL
SF_IL1
vs
l1
cf
rl
fcn
IL1_dot
VO_dot
IO
1/s
1/s
5 Out5
3 Out3
4 Out4
IL1
SF_IL1
fcn
2 Out2

Block Parameters: Pulse Generator1

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): 1/(fsw)

Pulse Width (% of period): d*100

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

OK
Cancel
Help
Apply

**FIGURE 5.7**
Buck converter model subsystem.

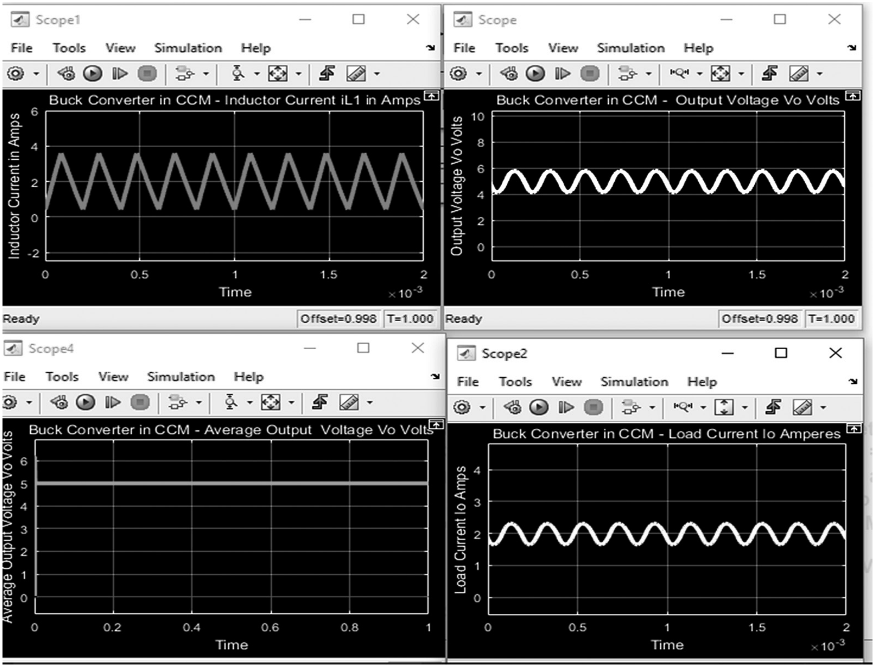

Scope1
File Tools View Simulation Help
Buck Converter in CCM - Inductor Current iL1 in Amps
Inductor Current in Amps
6
4
2
0
-2
0
0.5
1
1.5
2
Time
×10⁻³
Ready
Offset=0.998
T=1.000
Scope
File Tools View Simulation Help
Buck Converter in CCM - Output Voltage Vo Volts
Output Voltage Vo Volts
10
8
6
4
2
0
0
0.5
1
1.5
2
Time
×10⁻³
Ready
Offset=0.998
T=1.000
Scope4
File Tools View Simulation Help
Buck Converter in CCM - Average Output Voltage Vo Volts
Average Output Voltage Vo Volts
6
5
4
3
2
1
0
0
0.2
0.4
0.6
0.8
1
Time
Scope2
File Tools View Simulation Help
Buck Converter in CCM - Load Current Io Amperes
Load Current Io Amps
4
3
2
1
0
0
0.5
1
1.5
2
Time
×10⁻³

**FIGURE 5.8**
Buck converter in CCM: simulation results.

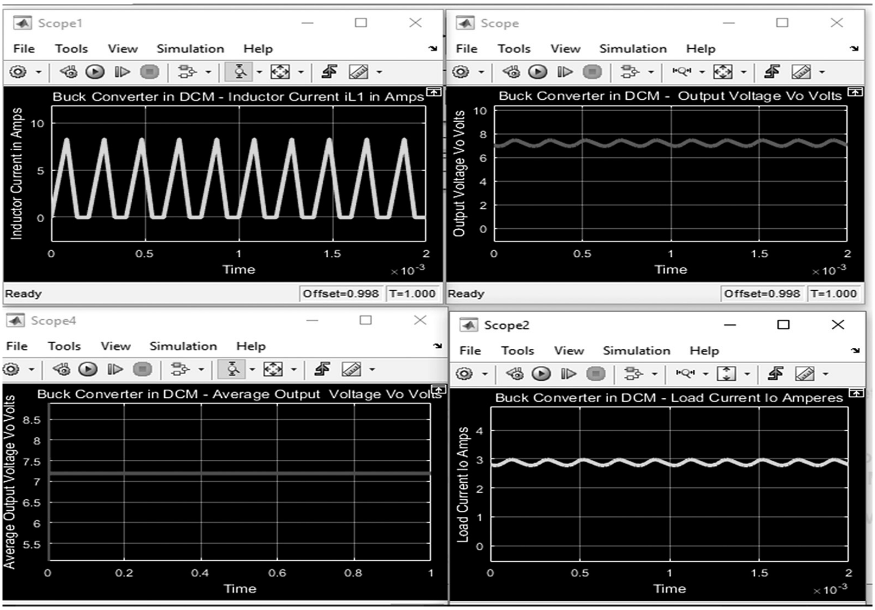

Scope1
File Tools View Simulation Help
Buck Converter in DCM - Inductor Current iL1 in Amps
Inductor Current in Amps
10
5
0
0
0.5
1
1.5
2
Time
×10⁻³
Ready
Offset=0.998
T=1.000
Scope
File Tools View Simulation Help
Buck Converter in DCM - Output Voltage Vo Volts
Output Voltage Vo Volts
10
8
6
4
2
0
0
0.5
1
1.5
2
Time
×10⁻³
Ready
Offset=0.998
T=1.000
Scope4
File Tools View Simulation Help
Buck Converter in DCM - Average Output Voltage Vo Volts
Average Output Voltage Vo Volts
8.5
8
7.5
7
6.5
6
5.5
0
0.2
0.4
0.6
0.8
1
Time
Scope2
File Tools View Simulation Help
Buck Converter in DCM - Load Current Io Amperes
Load Current Io Amps
4
3
2
1
0
0
0.5
1
1.5
2
Time
×10⁻³

**FIGURE 5.9**
Buck converter in DCM: simulation results.

**TABLE 5.2**

Buck Converter: Simulation Results

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | 5 | 0.425 | 3.594 | 2 | CCM |
| 2 | 7.2 | 0 | 8.1 | 2.88 | DCM |

**TABLE 5.3**

Buck Converter: Calculated Values

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | 5 | 0.54 | 3.46 | 2 | CCM |
| 2 | 7.44 | 0 | 7.6 | 2.976 | DCM |

## 5.5 Boost Converter Analysis in Continuous Conduction Mode

The boost converter topology using a semiconductor switch is shown in Figure 5.10 [1–6]. The switch is driven by an external PWM drive whose period is *T* and duty cycle is *D*. Figure 5.11a,b shows the equivalent circuit of Figure 5.10 in the CCM when the switch is ON from 0 to *DT* s and OFF from *DT* to *T* s respectively. The inductor current is always greater than zero in the CCM analysis. Noting that the change in inductor current during the ON period and OFF period are equal or the average inductor current over one switching cycle is zero, the following equations can be derived:

$$\left(\frac{V_S}{L_1}\right) * D.T + \left[\frac{(V_S - V_O)}{L_1}\right] * (1-D).T = 0 \tag{5.20}$$

$$\frac{V_O}{V_S} = \frac{1}{(1-D)} \tag{5.21}$$

During the switch ON period, the inductor current grows linearly and reaches a maximum value $I_{L1\max}$, and during the switch OFF period, the inductor current decays and reaches a minimum value $I_{L1\min}$. The relevant waveforms for CCM operation of the boost converter are shown in Figure 5.12. Neglecting switching losses, input and output power are equal. The inductor current is derived as follows:

$$V_S * I_{L1} = \frac{V_O^2}{R_L} \tag{5.22}$$

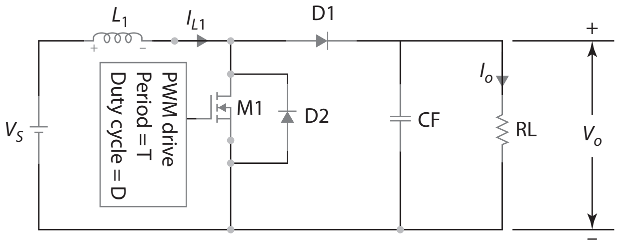

L1
IL1
D1
+
Io
VS
PWM drive
Period = T
Duty cycle = D
M1
D2
CF
RL
Vo
−

**FIGURE 5.10**
Boost converter.

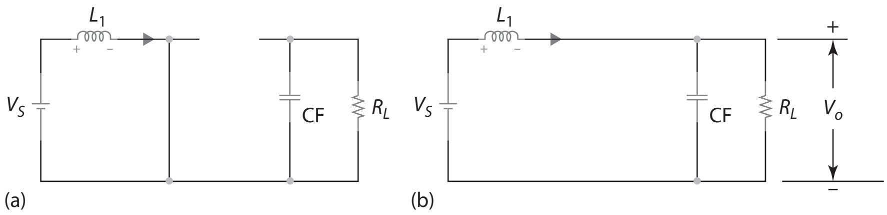

L1
VS
CF
RL
(a)
L1
VS
CF
RL
+
Vo
−
(b)

**FIGURE 5.11**
Boost converter equivalent circuits. (a) Switch ON for $0 < t \leq D.T$. (b) Switch OFF for $D.T < t \leq T$.

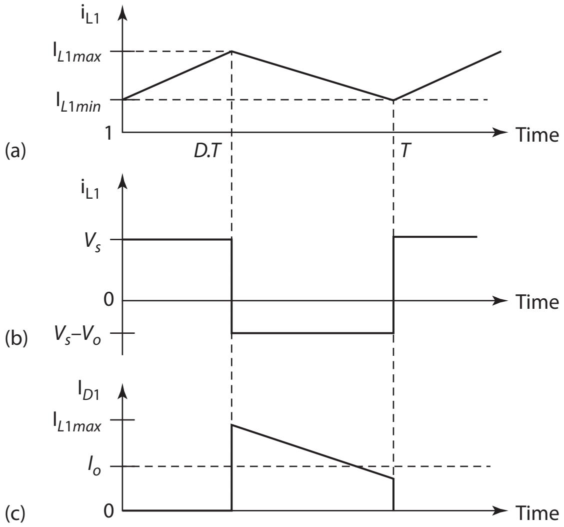


**FIGURE 5.12**
Boost converter waveforms in CCM: (a) inductor current; (b) inductor voltage; and (c) input current.

Using Equations 5.21 and 5.22, the average inductor current $I_{L1}$ is given as follows:

$$I_{L1} = \frac{V_S}{(1-D)^2 * R_L} \tag{5.23}$$

The maximum and minimum inductor current are derived as follows:

$$I_{L1\max} = \left[ \frac{V_S}{(1-D)^2 * R_L} + \frac{V_S * D.T}{2.L_1} \right] \tag{5.24}$$

$$I_{L1\min} = \left[ \frac{V_S}{(1-D)^2 * R_L} - \frac{V_S * D.T}{2.L_1} \right] \tag{5.25}$$

The critical inductance $L_{1\text{crit}}$ required to maintain CCM is obtained by equating $I_{L1\min}$ to zero. This gives the following value for $L_{1\text{crit}}$:

$$L_{1\text{crit}} = \frac{R_L * T}{2} * (1-D)^2 * D \tag{5.26}$$

If the inductor value of $L_1$ is below $L_{1\text{crit}}$, then the converter operates in DCM.

## 5.6 Boost Converter Analysis in Discontinuous Conduction Mode

In DCM, there exists a short interval of time during which the inductor current is zero. The equivalent circuit for DCM operation of the buck converter is shown in Figure 5.13. Figure 5.13c corresponds to DCM operation. The relevant voltage and current waveforms for DCM operation are shown in Figure 5.14. The average inductor current over one switching cycle is zero. This can be expressed as shown here:

$$\left( \frac{V_S}{L_1} \right) * D.T + \left[ \frac{(V_S - V_O)}{L_1} \right] * (D_1 - D).T = 0 \tag{5.27}$$

$$\frac{V_O}{V_S} = M = \frac{D_1}{(D_1 - D)} \tag{5.28}$$

Referring to Figure 5.14c, the average diode current is equal to the load current. Thus, $I_O$ is expressed as follows:

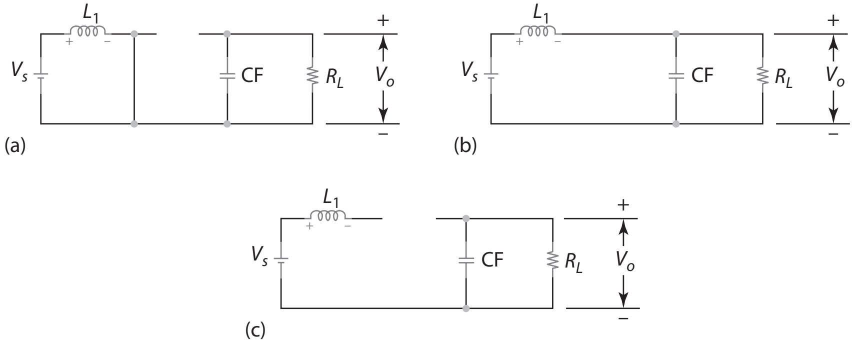


**FIGURE 5.13**
Boost converter equivalent circuits in DCM. (a) Switch ON. (b) Switch OFF. (c) Inductor and diode current are zero.

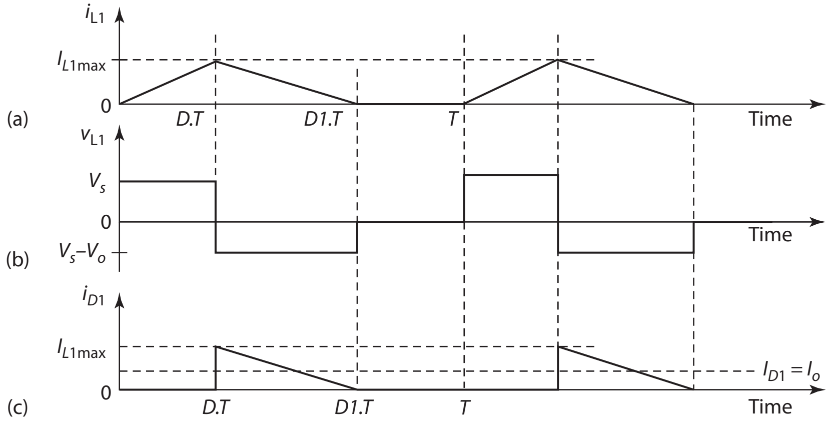


**FIGURE 5.14**
Boost converter waveforms in DCM. (a) Inductor current. (b) Inductor voltage. (c) Diode current.

$$I_O = \frac{V_O}{R_L} = \frac{(D_1 - D) * I_{L1\max}}{2} = \frac{V_S * (D_1 - D) * D * T}{2.L_1} \tag{5.29}$$

$$\frac{V_O}{V_S} = M = \frac{(D_1 - D) * D * T * R_L}{2.L_1} \tag{5.30}$$

Using Equations 5.28 and 5.30 and solving for *M*, we have the following:

$$\frac{V_O}{V_S} = M = \frac{1}{2} \pm \sqrt{\frac{1}{4} + \frac{D^2 * T * R_L}{2.L_1}} \tag{5.31}$$

$$D_1 = \frac{M*D}{(M-1)} \tag{5.32}$$

Equation 5.31 gives two values for $M$, of which one is valid.

## 5.7 Model of Boost Converter in CCM and DCM

Models of the boost converter are available in references [7–13]. The switching function concept is used to model the boost converter [7–13]. Boost converter model parameters are shown in Table 5.4. The development of the model is given here:

Referring to Figures 5.11 and 5.13, the following equations can be derived for CCM and DCM operation of boost converters.

$$\left. \begin{aligned} i_{L1\_dot} &= \frac{(V_S)}{L_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(V_S - V_O)}{L_1} \quad \text{for} \quad D.T \le t \le T \end{aligned} \right| \tag{5.33}$$

Now, for the switch $S$, switching function SF has already been defined in Equation 5.14 for CCM operation. The inverse switch function SF_BAR is defined as follows:

$$\left. \begin{aligned} \text{SF\_BAR} &= 0 \quad \text{for} \quad 0 \le t \le D.T \\ &= 1 \quad \text{for} \quad D.T \le t \le T \end{aligned} \right| \tag{5.34}$$

$$\text{SF\_BAR} = (1 - \text{SF}) \tag{5.35}$$

For the inductor current $i_{L1}$, another switch function SF_IL1 has already been defined in Equation 5.15.

Using Equations 5.14, 5.15 and 5.35 in Equation 5.33, we have the following:

**TABLE 5.4**

Boost Converter Model Parameters

| Sl. No. | Input Voltage $V_S$ (V) | Switching Frequency fsw (Hz) | Duty Cycle $D$ | Inductor $L_1$ (H) | Filter Capacitor $C_F$ (F) | Load Resistor $R_L$ (Ω) | Remarks |
|---|---|---|---|---|---|---|---|
| 1 | 12 | 25E3 | 0.6 | 960E−6 | 90E−6 | 50 | CCM |
| 2 | 12 | 25E3 | 0.6 | 20E−6 | 90E−6 | 50 | DCM |

$$i_{L1\_dot} = \frac{\left[V_S - \mathrm{SF\_IL1} * (1 - \mathrm{SF}) * V_O\right]}{L_1} \tag{5.36}$$

The inductor current flows through the load resistor during the switch OFF period in CCM and in DCM until it falls to zero. The output voltage equation is formulated by observation of equivalent circuits for CCM and DCM (Figures 5.11 and 5.13), as follows:

$$I_{CF} = (1 - \mathrm{SF}) * I_{L1} - I_O \tag{5.37}$$

$$v_{O\_dot} = \left(\frac{\mathrm{SF\_IL1} * (1 - \mathrm{SF}) * I_{L1}}{C_F} - \frac{V_O}{R_L * C_F}\right) \tag{5.38}$$

In Equations 5.36, 5.37 and 5.38, $i_{L1\_dot}$, $I_{CF}$, $I_O$ and $v_{O\_dot}$ are as defined in Section 5.4. $I_O$ is defined in Equation 5.19.

The interactive model of the boost converter suitable for CCM and DCM operation is given in Figure 5.15 with a dialogue box. The model subsystem with a dialogue box is shown in Figure 5.16. The data shown in the dialogue box is for CCM operation of the boost converter, given in Table 5.4. For DCM operation, the relevant data from Table 5.4 have to be re-entered in the dialogue box.

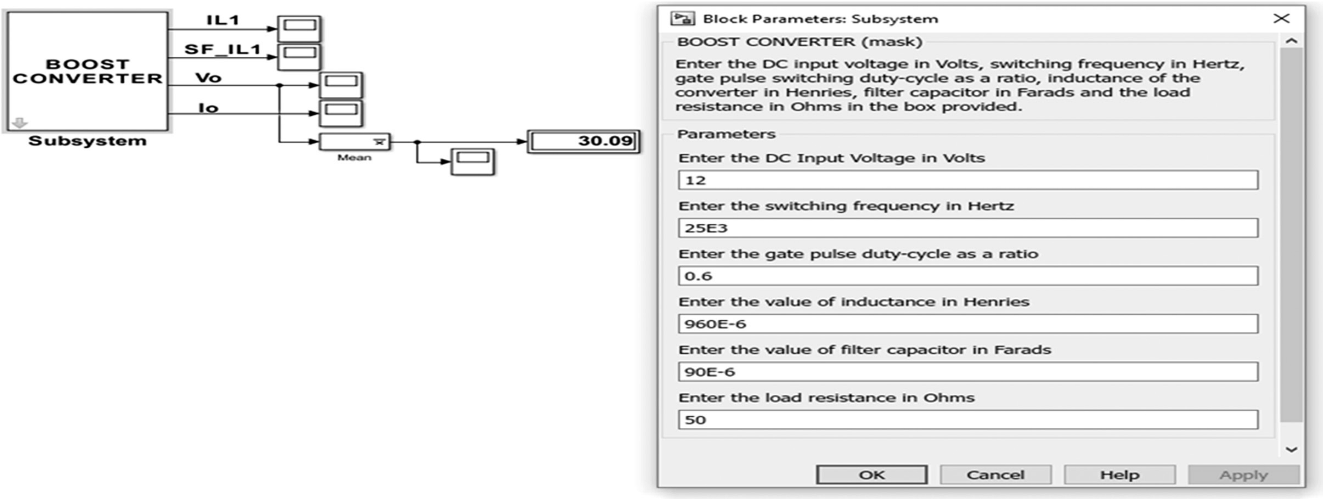
The switch function for the switch SF defined in Equation 5.14 and that for inductor current SF_IL1 defined in Equation 5.15 are generated as explained in Section 5.4. Equations 5.36, 5.38 and 5.19 are solved using the embedded MATLAB function and the source code is written as explained in Section 5.4. The embedded MATLAB outputs $v_{o\_dot}$, $i_{L1\_\mathrm{dot}}$ are integrated using Integrator blocks to obtain the required outputs and are used as feedback inputs along with SF_IL1 to solve Equations 5.36, 5.38 and 5.19.

### 5.7.1 Simulation Results

Simulation of the boost converter for CCM and DCM operations were carried out using Simulink [14]. The ode23t (mod. stiff/trapezoidal) solver was used. The data shown in Table 5.4 were used for the simulation. The simulation results for the boost converter in CCM are shown in Figure 5.17 and those for DCM are shown in Figure 5.18. Simulation results and calculated values are tabulated in Tables 5.5 and 5.6.

## 5.8 Buck–Boost Converter Analysis in Continuous Conduction Mode

The buck–boost converter topology using a semiconductor switch is shown in Figure 5.19 [1–6]. The switch is driven by an external PWM drive whose period is $T$ and duty cycle is $D$. Figure 5.20a,b shows the equivalent



BOOST CONVERTER
Subsystem
IL1
SF_IL1
Vo
Io
Mean
30.09

Block Parameters: Subsystem

BOOST CONVERTER (mask)

Enter the DC input voltage in Volts, switching frequency in Hertz, gate pulse switching duty-cycle as a ratio, inductance of the converter in Henries, filter capacitor in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the DC Input Voltage in Volts: 12

Enter the switching frequency in Hertz: 25E3

Enter the gate pulse duty-cycle as a ratio: 0.6

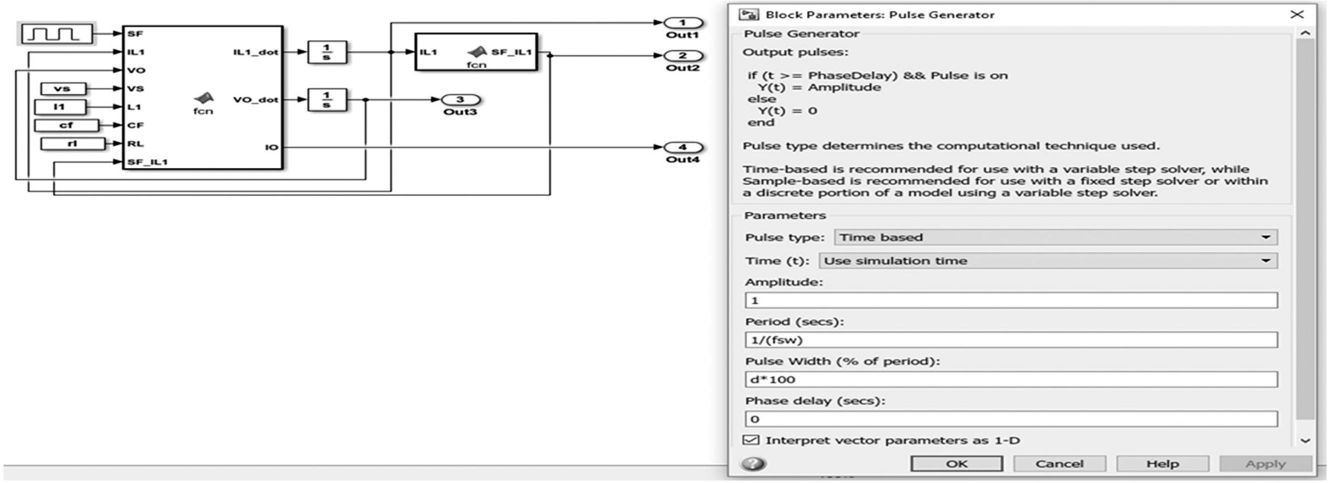
Enter the value of inductance in Henries: 960E-6

Enter the value of filter capacitor in Farads: 90E-6

Enter the load resistance in Ohms: 50

OK
Cancel
Help
Apply

**FIGURE 5.15**
Boost converter in CCM and DCM.


SF
IL1
VO
VS
L1
CF
RL
SF_IL1
vs
l1
cf
rl
fcn
IL1_dot
VO_dot
IO
1/s
1/s
IL1
SF_IL1
fcn
1 Out1
2 Out2
3 Out3
4 Out4

Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): 1/(fsw)

Pulse Width (% of period): d*100

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

OK
Cancel
Help
Apply

**FIGURE 5.16**
Boost converter model subsystem.

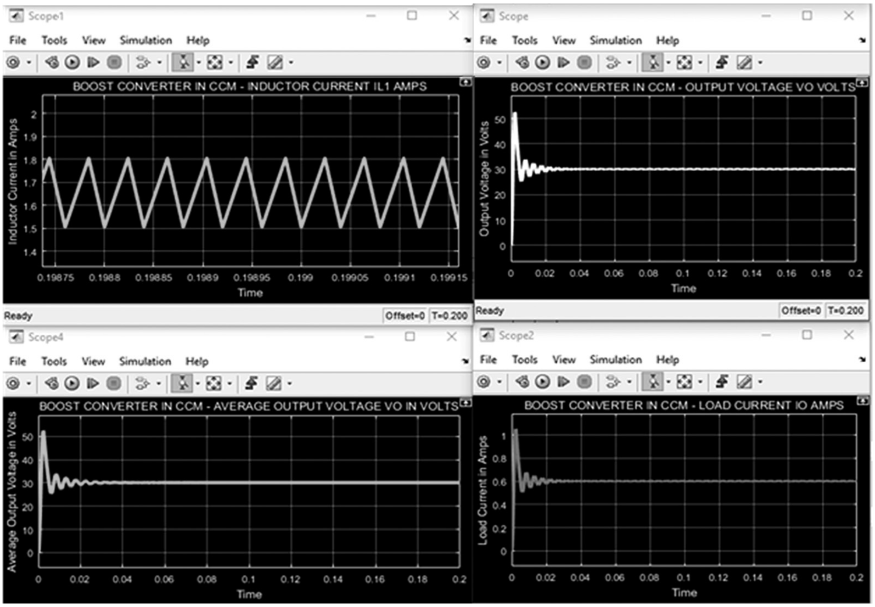


**FIGURE 5.17**
Boost converter in CCM: simulation results.

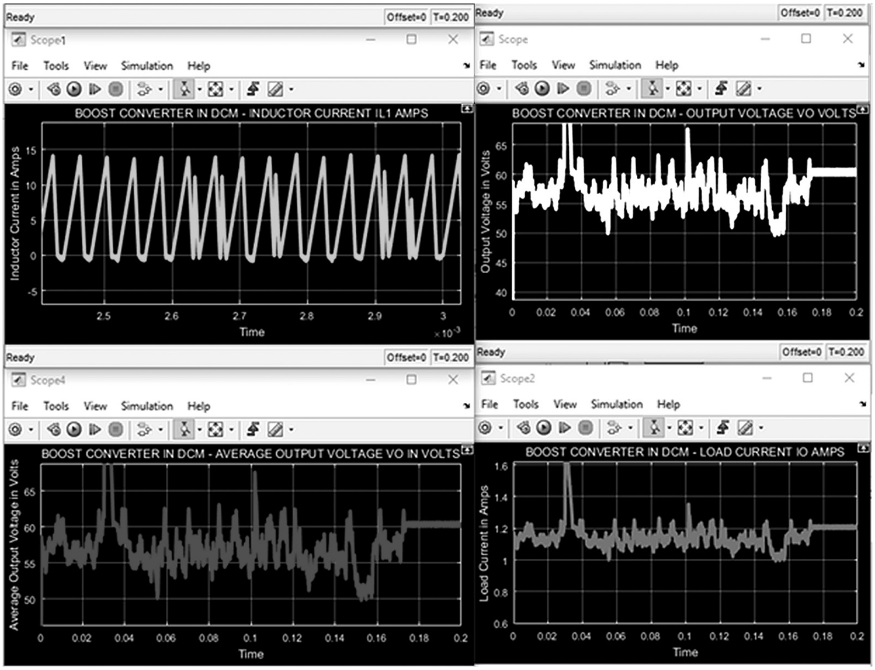


**FIGURE 5.18**
Boost converter in DCM: simulation results.

**TABLE 5.5**

Boost Converter: Simulation Results

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | 30.09 | 1.5 | 1.8 | 0.6 | CCM |
| 2 | 60 | 0 | 14 | 1.2 | DCM |

**TABLE 5.6**

Boost Converter: Calculated Values

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | 30 | 1.35 | 1.65 | 0.6 | CCM |
| 2 | 57.26 | 0 | 14.4 | 1.145 | DCM |

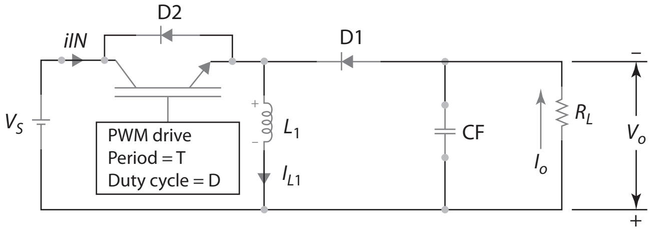


**FIGURE 5.19**
Buck–boost converter.

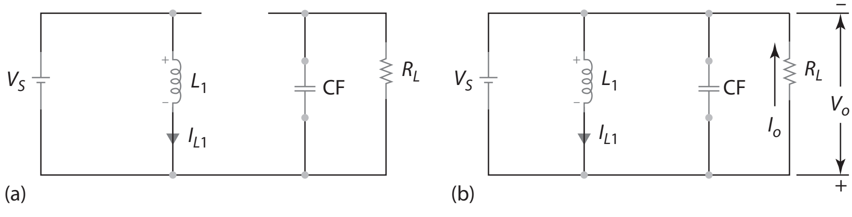


**FIGURE 5.20**
Buck–boost converter equivalent circuits in CCM. (a) Switch ON for $0 < t \leq D.T$. (b) Switch OFF for $D.T < t \leq T$.

circuit of Figure 5.19 in the CCM when the switch is ON from 0 to $DT$ s and OFF from $DT$ to $T$ s respectively. The inductor current is always greater than zero in the CCM analysis. Noting that the change in inductor current during the ON period and OFF period are equal or the average inductor current over one switching cycle is zero, the following equations can be derived:

$$\left(\frac{V_S}{L_1}\right) * D * T + \left(\frac{V_O}{L_1}\right) * (1 - D) * T = 0 \tag{5.39}$$

$$\frac{V_O}{V_S} = \frac{-D}{(1 - D)} \tag{5.40}$$

The minus sign in Equation 5.40 indicates that the polarity of $V_O$ is negative at the top and positive at the bottom terminal. During the switch ON period, the inductor current grows linearly and reaches a maximum value $I_{L1\max}$, and during the switch OFF period, the inductor current decays and reaches a minimum value $I_{L1\min}$. The relevant waveforms for CCM operation of the buck–boost converter are shown in Figure 5.21. Neglecting switching losses, input and output power are equal. The inductor current is derived as follows:

$$V_S * I_{IN} = \frac{V_O^2}{R_L} \tag{5.41}$$

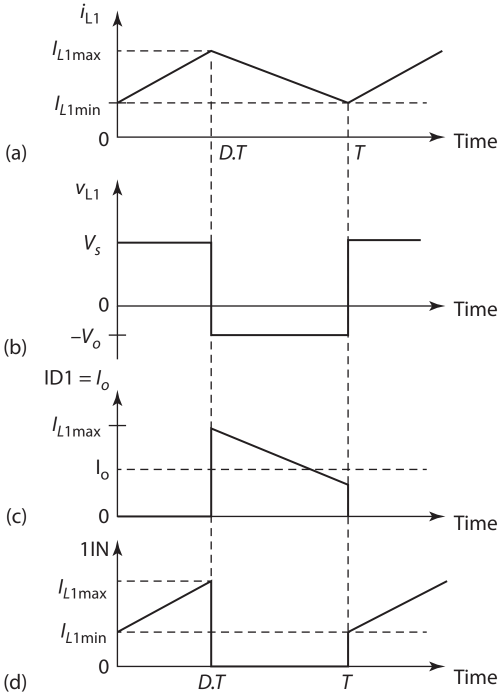


**FIGURE 5.21**
Buck–boost converter waveforms in CCM. (a) Inductor current. (b) Inductor voltage. (c) Diode current. (d) Input current.

$$I_{IN} = D * I_{L1} \tag{5.42}$$

$$I_{L1} = \frac{V_O^2}{V_S * D * R_L} \tag{5.43}$$

Using Equations 5.40 and 5.43, the average inductor current $I_{L1}$ and the maximum and minimum values of the inductor current can be expressed as follows:

$$I_{L1} = \frac{V_S * D}{(1-D)^2 * R_L} \tag{5.44}$$

$$I_{L1\max} = \left[ \frac{V_S * D}{(1-D)^2 * R_L} + \frac{V_S * D * T}{2.L_1} \right] \tag{5.45}$$

$$I_{L1\min} = \left[ \frac{V_S * D}{(1-D)^2 * R_L} - \frac{V_S * D * T}{2.L_1} \right] \tag{5.46}$$

The critical inductance, or minimum value of inductance of the buck–boost converter to maintain CCM operation, is obtained by setting Equation 5.46 to zero, which results in the following expression:

$$L_{1crit} = \frac{(1-D)^2 * T * R_L}{2} \tag{5.47}$$

## 5.9 Buck–Boost Converter Analysis in the Discontinuous Conduction Mode

In the DCM, there exists a short interval of time during which the inductor current is zero. The equivalent circuit for DCM operation of the buck–boost converter is shown in Figure 5.22. Figure 5.22c corresponds to DCM operation. The relevant voltage and current waveforms for DCM operation are shown in Figure 5.23. The average inductor current over one switching cycle is zero. This can be expressed as follows:

$$\left( \frac{V_S}{L_1} \right) * D.T + \left( \frac{-V_O}{L_1} \right) * (D_1 - D).T = 0 \tag{5.48}$$

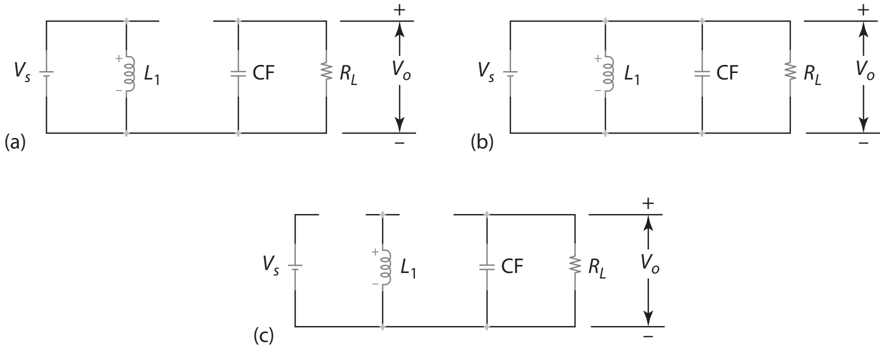


**FIGURE 5.22**
Buck–boost converter equivalent circuits in DCM. (a) Switch ON; (b) Switch OFF. (c) Inductor and diode current are zero.

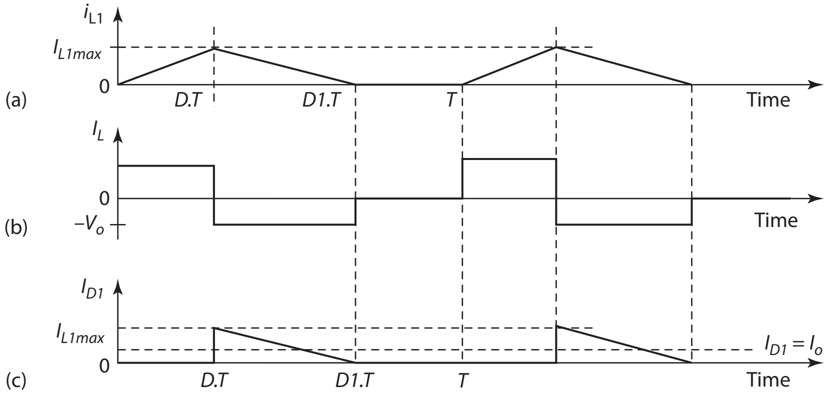


**FIGURE 5.23**
Buck–boost converter waveforms in DCM. (a) Inductor current. (b) Inductor voltage. (c) Diode current.

$$\frac{V_O}{V_S} = M = \frac{D}{(D_1 - D)} \tag{5.49}$$

Referring to Figure 5.23c, the average diode current is equal to the load current. Thus, $I_O$ is expressed as follows.

$$I_O = \frac{V_O}{R_L} = \frac{(D_1 - D) * I_{L1\max}}{2} = \frac{V_S * (D_1 - D) * D * T}{2.L_1} \tag{5.50}$$

$$\frac{V_O}{V_S} = M = \frac{(D_1 - D) * D * T * R_L}{2.L_1} \tag{5.51}$$

Using Equations 5.49 and 5.51 and solving for *M*, we have the following:

$$\frac{V_O}{V_S} = M = D * \sqrt{\frac{T * R_L}{2.L_1}} \tag{5.52}$$

$$D_1 = \left( D + \frac{D}{M} \right) \tag{5.53}$$

## 5.10 Models of Buck–Boost Converter in CCM and DCM

Models of the buck–boost converter are available in the literature [13]. The switching function concept is used to model the buck–boost converter [7–13]. The buck–boost converter model parameters are shown in Table 5.7. The development of the model is given here.

Referring to Figures 5.20 and 5.22, the following equations can be derived for CCM and DCM operation of the buck–boost converter:

$$\left. \begin{aligned} i_{L1\_dot} &= \frac{(V_S)}{L_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(-V_O)}{L_1} \quad \text{for} \quad D.T \le t \le T \end{aligned} \right| \tag{5.54}$$

Now, for the switch *S*, the switching function SF has already been defined in Equation 5.14 for CCM operation. The inverse switch function SF_BAR has been defined in Equations 5.34 and 5.35.

For the inductor current $i_{L1}$, another switch function SF_IL1 has already been defined in Equation 5.15.

Using Equations 5.14, 5.15 and 5.35 in Equation 5.54, we have the following:

$$i_{L1\_dot} = \frac{\left[ \mathrm{SF} * V_S - \mathrm{SF\_IL1} * (1 - \mathrm{SF}) * V_O \right]}{L_1} \tag{5.55}$$

**TABLE 5.7**

Buck–Boost Converter Model Parameters

| Sl. No. | Input Voltage $V_S$(V) | Switching Period *T* (s) | Duty Cycle *D* | Inductor $L_1$ (H) | Filter Capacitor $C_F$ (F) | Load Resistor $R_L$ (Ω) | Remarks |
|---|---|---|---|---|---|---|---|
| 1 | 24 | 5.00E−05 | 0.4 | 1.00E−04 | 4.00E−04 | 5 | CCM |
| 2 | 24 | 5.00E−05 | 0.6 | 1.00E−04 | 4.00E−04 | 5 | CCM |
| 3 | 24 | 5.00E−05 | 0.4 | 2.30E−05 | 4.00E−04 | 5 | DCM |

The inductor current flows through the load resistor during the switch OFF period in CCM and in DCM until it falls to zero. The output voltage equation is formulated by observation of equivalent circuits for CCM and DCM (Figures 5.20 and 5.22), as follows:

$$I_{CF} = (1 - \text{SF}) * I_{L1} - I_O \tag{5.56}$$

$$v_{O\_dot} = \left( \frac{\text{SF\_IL1} * (1 - \text{SF}) * I_{L1}}{C_F} - \frac{V_O}{R_L * C_F} \right) \tag{5.57}$$

In Equations 5.55, 5.56 and 5.57, $i_{L1\_dot}$, $I_{CF}$, $I_O$ and $v_{O\_dot}$ are as defined in Section 5.4. $I_O$ is defined in Equation 5.19.

The interactive model of the buck–boost converter suitable for CCM and DCM operation is given in Figure 5.24 with a dialogue box. The model subsystem with a dialogue box is shown in Figure 5.25.

The data shown in the dialogue box is for CCM operation of the boost converter given in Table 5.7. For DCM operation, the relevant data from Table 5.7 have to be re-entered in the dialogue box.

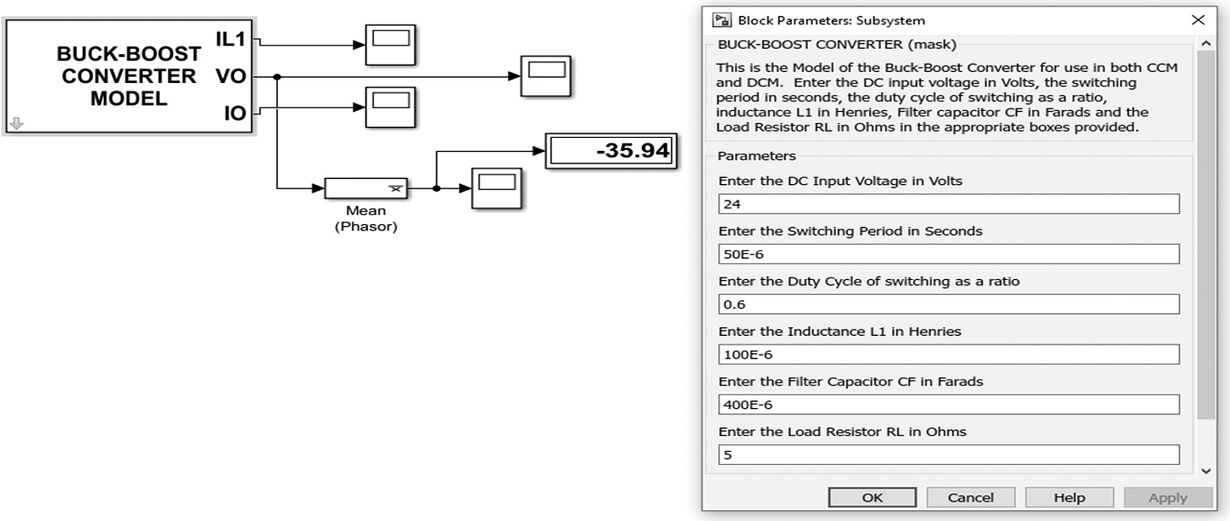
The switch function for the switch SF defined in Equation 5.14 and that for the inductor current SF_IL1 defined in Equation 5.15 are generated as explained in Section 5.4. Equations 5.55, 5.57 and 5.19 are solved using the embedded MATLAB function and the source code is written as explained in Section 5.4. The embedded MATLAB outputs $v_{o\_dot}$, $i_{L1\_dot}$ are integrated using Integrator blocks to obtain the required outputs and are used as feedback inputs along with SF_IL1 to solve Equations 5.55, 5.57 and 5.19.

### 5.10.1 Simulation Results

Simulation of the buck–boost converter for CCM and DCM operations was carried out via Simulink [14]. The ode23t (mod. stiff/trapezoidal) solver was used. The data shown in Table 5.7 are used for the simulation. The simulation results for the buck–boost converter in CCM are shown in Figures 5.26 and 5.27 and those for DCM are shown in Figure 5.28. Simulation results and calculated values are tabulated in Tables 5.8 and 5.9, respectively.

## 5.11 Conclusions

Interactive models are developed for the second-order DC to DC converters such as the buck, boost and the buck–boost topology. One model is suitable to analyse both CCM and DCM operation. The models developed are system models. The embedded MATLAB function is used to develop system models


BUCK-BOOST
CONVERTER
MODEL
IL1
VO
IO
Mean
(Phasor)
-35.94
Block Parameters: Subsystem
OK
Cancel
Help
Apply

BUCK-BOOST CONVERTER (mask)

This is the Model of the Buck-Boost Converter for use in both CCM and DCM. Enter the DC input voltage in Volts, the switching period in seconds, the duty cycle of switching as a ratio, inductance L1 in Henries, Filter capacitor CF in Farads and the Load Resistor RL in Ohms in the appropriate boxes provided.

Parameters

Enter the DC Input Voltage in Volts
24

Enter the Switching Period in Seconds
50E-6

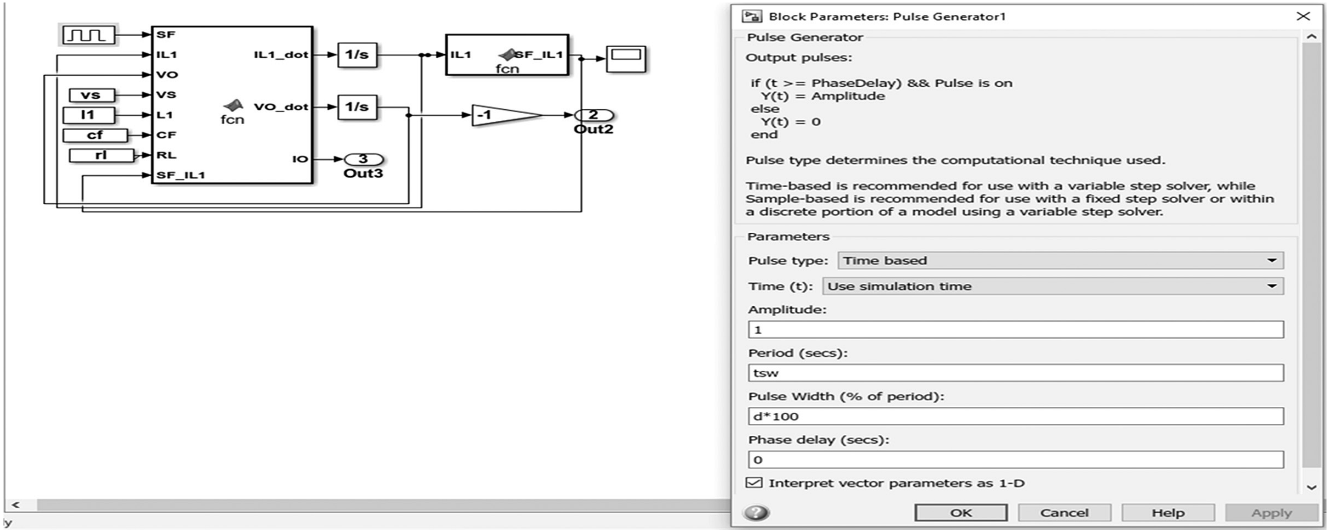
Enter the Duty Cycle of switching as a ratio
0.6

Enter the Inductance L1 in Henries
100E-6

Enter the Filter Capacitor CF in Farads
400E-6

Enter the Load Resistor RL in Ohms
5

**FIGURE 5.24**
Buck–boost converter model in CCM and DCM.


SF
IL1
VO
VS
L1
CF
RL
SF_IL1
vs
l1
cf
rl
fcn
IL1_dot
VO_dot
IO
1/s
1/s
3
Out3
IL1
SF_IL1
fcn
-1
2
Out2
OK
Cancel
Help
Apply

Block Parameters: Pulse Generator1

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): tsw

Pulse Width (% of period): d*100

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

**FIGURE 5.25**
Buck–boost converter model subsystem.

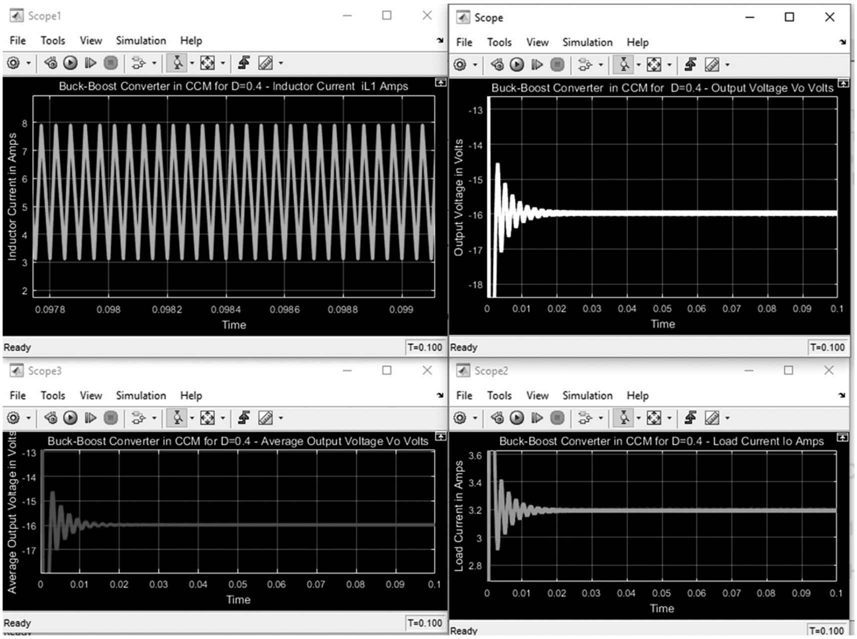

Scope1
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.4 - Inductor Current iL1 Amps
Inductor Current in Amps
2 3 4 5 6 7 8
0.0978 0.098 0.0982 0.0984 0.0986 0.0988 0.099
Time
Ready
T=0.100
Scope
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.4 - Output Voltage Vo Volts
Output Voltage in Volts
-13 -14 -15 -16 -17 -18
0 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0.09 0.1
Time
Ready
T=0.100
Scope3
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.4 - Average Output Voltage Vo Volts
Average Output Voltage in Volts
-13 -14 -15 -16 -17
0 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0.09 0.1
Time
Ready
T=0.100
Scope2
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.4 - Load Current Io Amps
Load Current in Amps
3.6 3.4 3.2 3 2.8
0 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0.09 0.1
Time
Ready
T=0.100

**FIGURE 5.26**
Buck–boost converter in CCM: simulation results for $D = 0.4$.

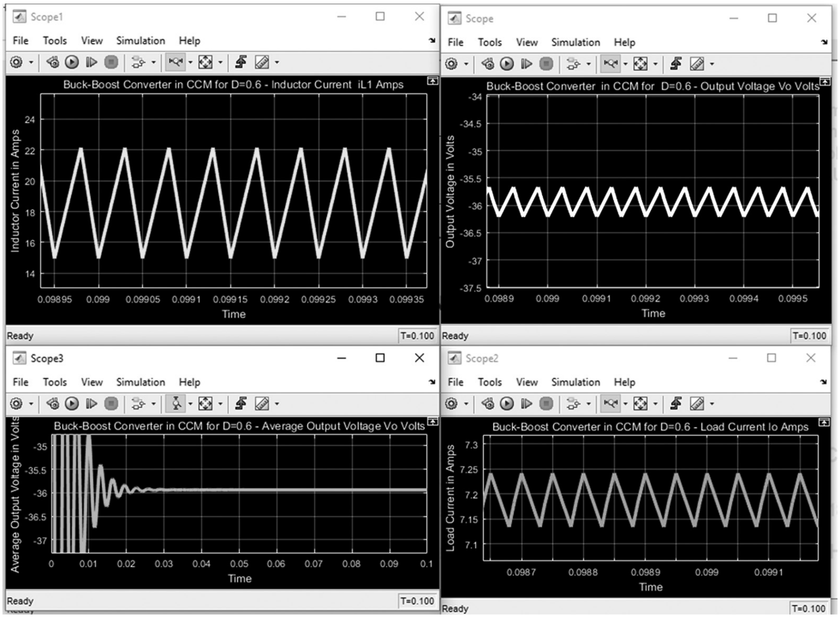

Scope1
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.6 - Inductor Current iL1 Amps
Inductor Current in Amps
14 16 18 20 22 24
0.09895 0.099 0.09905 0.0991 0.09915 0.0992 0.09925 0.0993 0.09935
Time
Ready
T=0.100
Scope
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.6 - Output Voltage Vo Volts
Output Voltage in Volts
-34 -34.5 -35 -35.5 -36 -36.5 -37 -37.5
0.0989 0.099 0.0991 0.0992 0.0993 0.0994 0.0995
Time
Ready
T=0.100
Scope3
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.6 - Average Output Voltage Vo Volts
Average Output Voltage in Volts
-35 -35.5 -36 -36.5 -37
0 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0.09 0.1
Time
Ready
T=0.100
Scope2
File Tools View Simulation Help
Buck-Boost Converter in CCM for D=0.6 - Load Current Io Amps
Load Current in Amps
7.3 7.25 7.2 7.15 7.1
0.0987 0.0988 0.0989 0.099 0.0991
Time
Ready
T=0.100

**FIGURE 5.27**
Buck–boost converter in CCM: simulation results for $D = 0.6$.

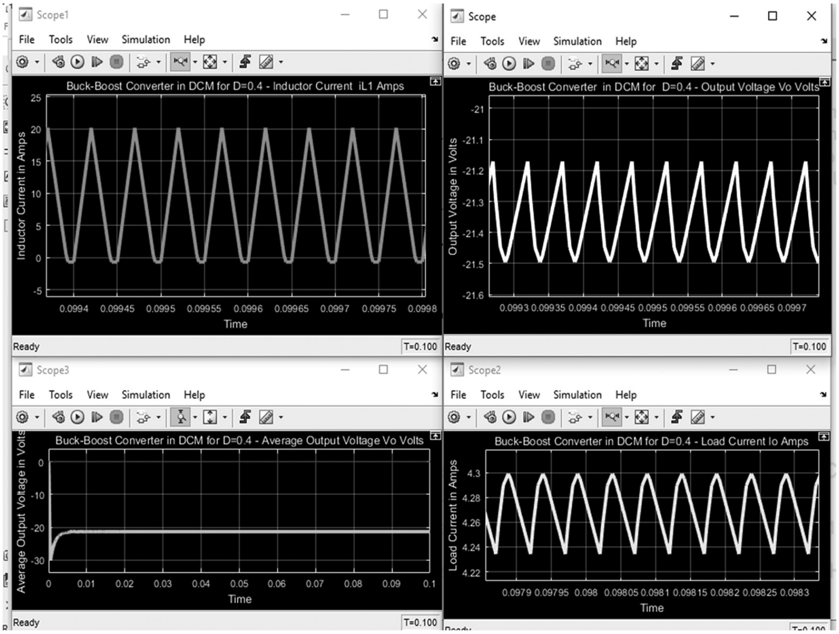

Scope1
File Tools View Simulation Help
Buck-Boost Converter in DCM for D=0.4 - Inductor Current iL1 Amps
Inductor Current in Amps
25
20
15
10
5
0
-5
0.0994 0.09945 0.0995 0.09955 0.0996 0.09965 0.0997 0.09975 0.0998
Time
Ready
T=0.100
Scope
File Tools View Simulation Help
Buck-Boost Converter in DCM for D=0.4 - Output Voltage Vo Volts
Output Voltage in Volts
-21
-21.1
-21.2
-21.3
-21.4
-21.5
-21.6
0.0993 0.09935 0.0994 0.09945 0.0995 0.09955 0.0996 0.09965 0.0997
Time
Ready
T=0.100
Scope3
File Tools View Simulation Help
Buck-Boost Converter in DCM for D=0.4 - Average Output Voltage Vo Volts
Average Output Voltage in Volts
0
-10
-20
-30
0 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0.09 0.1
Time
Ready
T=0.100
Scope2
File Tools View Simulation Help
Buck-Boost Converter in DCM for D=0.4 - Load Current Io Amps
Load Current in Amps
4.3
4.28
4.26
4.24
4.22
0.0979 0.09795 0.098 0.09805 0.0981 0.09815 0.0982 0.09825 0.0983
Time

**FIGURE 5.28**
Buck–boost converter in DCM: simulation results for $D = 0.4$.

**TABLE 5.8**
Buck–Boost Converter: Simulation Results

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Duty Cycle | Remarks |
|---|---|---|---|---|---|---|
| 1 | −16 | 3.05 | 7.99 | 3.2 | 0.4 | CCM |
| 2 | −35.94 | 15 | 22 | 7.19 | 0.6 | CCM |
| 3 | −21.35 | 0 | 20 | 4.27 | 0.4 | DCM |

**TABLE 5.9**
Buck–Boost Converter: Calculated Values

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Duty Cycle | Remarks |
|---|---|---|---|---|---|---|
| 1 | −16 | 2.933 | 7.733 | 3.2 | 0.4 | CCM |
| 2 | −36 | 14.4 | 21.6 | 7.2 | 0.6 | CCM |
| 3 | −22.38 | 0 | 20.869 | 4.476 | 0.4 | DCM |

for all these DC to DC converters. The simulation results indicate that the deviation from theoretically calculated values using formulae are negligible for all three DC to DC converters.

## References

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# 6

# *Interactive Models for AC to AC Converters*

## 6.1 Introduction

There are two categories of AC to AC converters. One is the cycloconverter, which converts the AC input voltage with a given frequency and peak value to a variable amplitude AC output voltage at a desired frequency, different from the frequency of the AC input voltage. The modelling of cycloconverters is not discussed in this chapter. The AC to AC converters used to vary the root mean square (RMS) value of the load voltage at a constant frequency that is the same as the frequency of the AC input voltage are known as *AC voltage controllers* or *AC regulators*. The voltage control is accomplished by phase control or on–off control. A single-phase AC controller uses a pair of silicon-controlled rectifiers (SCRs) connected back-to-back or antiparallel between the supply and the load. Several configurations for three-phase AC controllers are available employing three single-phase AC controllers. This chapter describes the system modelling of two predominant three-phase AC controller configurations, namely, three-phase AC controllers with back-to-back SCRs in series with the AC lines with star-connected resistive load and isolated neutral; and the other, the three-phase AC controllers with back-to-back SCRs in series with resistive load connected in delta to the AC lines.

## 6.2 Analysis of a Fully Controlled Three-Phase Three-Wire AC Voltage Controller with Star-Connected Resistive Load and Isolated Neutral

The three-phase three-wire AC voltage controller with back-to-back antiparallel SCRs and star-connected resistive load with isolated neutral is shown in Figure 6.1 [1–4].

By varying the firing angle α, the RMS voltage across the load can be varied. The firing sequence is T1, T2, T3, T4, T5 and T6. This is derived as follows:

The three-phase line-to-neutral input voltages $v_{AN}$, $v_{BN}$ and $v_{CN}$ are defined in Equation 6.1:

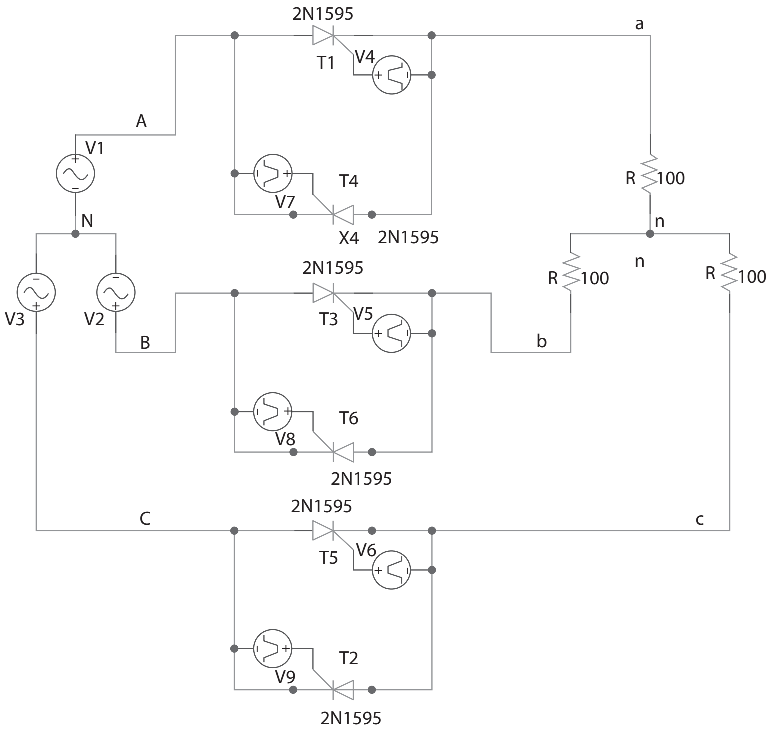

2N1595
a
T1
V4
A
V1
N
T4
V7
X4
2N1595
R
100
n
n
R
100
R
100
2N1595
T3
V5
V3
V2
B
b
T6
V8
2N1595
2N1595
C
c
T5
V6
T2
V9
2N1595

**FIGURE 6.1**
Three-phase AC back-to-back connected thyristor controller.

$$\left.\begin{aligned} vAN &= \sqrt{2} * V_S * \sin(\omega.t) \\ vBN &= \sqrt{2} * V_S * \sin\left(\omega.t - \frac{2\pi}{3}\right) \\ vCN &= \sqrt{2} * V_S * \sin\left(\omega.t + \frac{2\pi}{3}\right) \end{aligned}\right] \quad (6.1)$$

The three-phase instantaneous line-to-line input voltages are given here:

$$\left.\begin{aligned} v_{AB} &= \sqrt{6} * V_S * \sin\left(\omega.t + \frac{\pi}{6}\right) \\ v_{BC} &= \sqrt{6} * V_S * \sin\left(\omega.t - \frac{\pi}{2}\right) \\ v_{CA} &= \sqrt{6} * V_S * \sin\left(\omega.t - \frac{7\pi}{6}\right) \end{aligned}\right] \quad (6.2)$$

The RMS line-to-neutral voltage across the star-connected resistive load for various ranges of firing angle α are given here [1]:

For $0 \le \alpha < 60°$

$$V_O = V_{an\_rms} = \sqrt{6} * V_S * \sqrt{\left[\frac{1}{6} - \frac{\alpha}{4\pi} + \frac{\sin(2\alpha)}{8\pi}\right]} \tag{6.3}$$

For $60° \le \alpha < 90°$

$$V_O = V_{an\_rms} = \sqrt{6} * V_S * \sqrt{\left[\frac{1}{12} - \frac{3 * \sin(2\alpha)}{16\pi} + \frac{\sqrt{3} * \cos(2\alpha)}{16\pi}\right]} \tag{6.4}$$

For $90° \le \alpha < 150°$

$$V_O = V_{an\_rms} = \sqrt{6} * V_S * \sqrt{\left[\frac{5}{24} - \frac{\alpha}{4\pi} - \frac{\sin(2\alpha)}{16\pi} + \frac{\sqrt{3} * \cos(2\alpha)}{16\pi}\right]} \tag{6.5}$$

For $0 \le \alpha < 60°$, immediately before firing of T1, two thyristors conduct. When T1 is fired, three thyristors conduct. When the thyristor current reverses, the particular thyristor turns OFF. For $60° \le \alpha < 90°$, only two thyristors conduct at any time. For $90° \le \alpha < 150°$, although two thyristors conduct at any time, there are periods when *no* thyristors are ON. The output voltage becomes zero for α of 150°.

A PSIM [5] circuit model of this three-phase AC controller with star-connected resistive load and isolated neutral is shown in Figure 6.2 and the simulation result for a firing angle α of π/6 rad is shown in Figure 6.3.

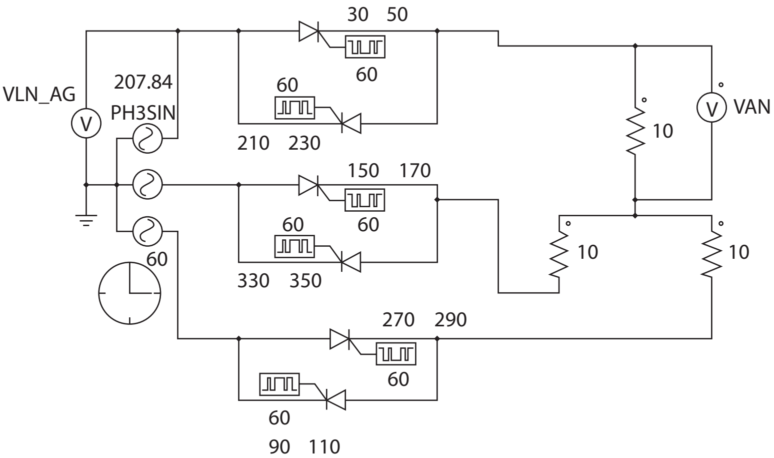
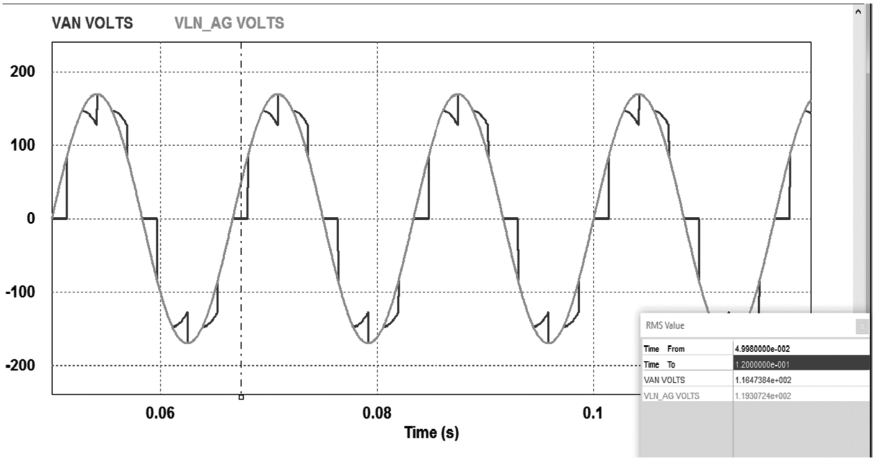


**FIGURE 6.2**
Three-phase AC controller with star-connected resistive load.



| RMS Value | |
|---|---|
| Time From | 4.9980000e-002 |
| Time To | 1.2000000e-001 |
| VAN VOLTS | 1.1647384e+002 |
| VLN_AG VOLTS | 1.1930724e+002 |

**FIGURE 6.3**
Simulation results for SCR three-phase AC controller with star-connected resistive load for a firing angle α of 30°.

The line-to-neutral RMS input voltage is 120 V, with a frequency of 60 Hz. The line-to-neutral RMS output voltage $V_{an}$ is 116.47 V by simulation, which closely agrees with the result obtained by using Equation 6.3.

### 6.2.1 Modelling of a Fully Controlled Three-Phase Three-Wire AC Voltage Controller with Star-Connected Resistive Load and Isolated Neutral

This section describes the modelling of the three-phase AC controller shown in Figure 6.1 [6]. The model for a firing angle α of π/6 rad is shown in Figure 6.4. The various dialogue boxes are shown in Figure 6.5 and the various subsystems in Figure 6.6a–d. The various subsystems are explained here:

Figure 6.6a corresponds to the dialogue box ‘Three-Phase AC Data’ in Figure 6.5. In this dialogue box, the RMS line-to-neutral voltage in volts and the frequency in hertz are entered. The peak voltage $V_m$ and angular frequency ω are internally calculated. Figure 6.6b corresponds to the dialogue box ‘Firing Angle’ in Figure 6.5. The firing angle α in radians is entered in this dialogue box. Figure 6.6b has three constant blocks that generate α, $[(2\pi/3)+\alpha]$, $[(4\pi/3)+\alpha]$ for the three phases. Figure 6.6c generates the switch function SF for the three phases. The switch function corresponds to the firing pulses for the back-to-back connected thyristors in the three phases. These switch functions SF_A, SF_B and SF_C are generated by Relay, Relay1 and Relay2 in Figure 6.6c connected to input phases A, B and C, as defined in Equation 6.6:

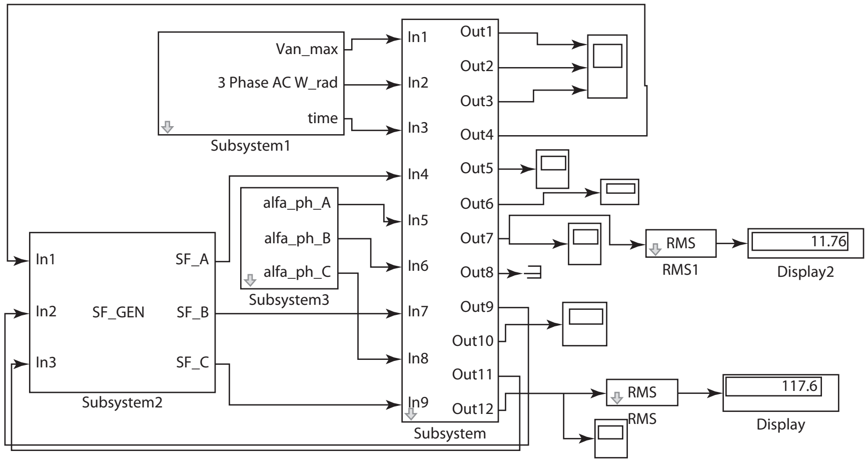
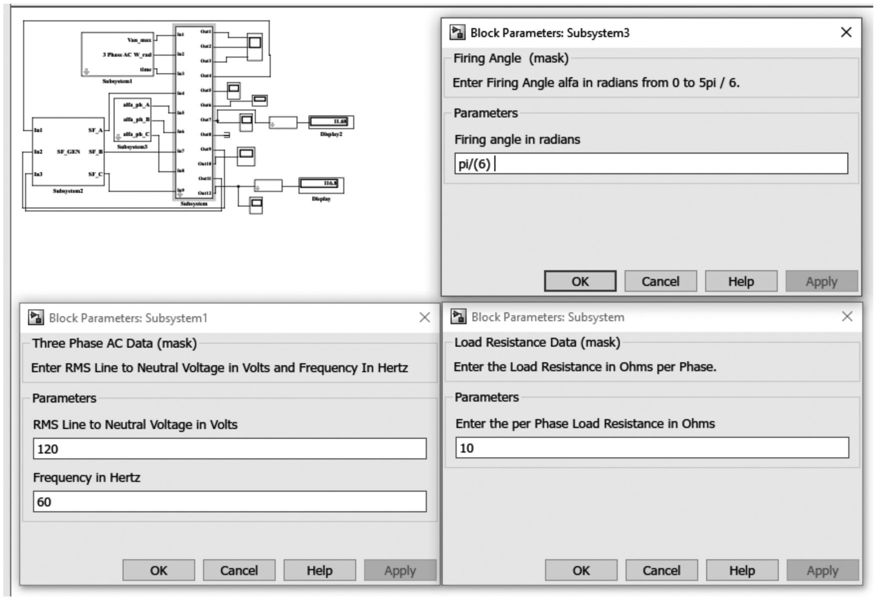

Van_max
3 Phase AC W_rad
time
Subsystem1
In1
In2
In3
In4
In5
In6
In7
In8
In9
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
Subsystem
alfa_ph_A
alfa_ph_B
alfa_ph_C
Subsystem3
In1
In2
In3
SF_GEN
SF_A
SF_B
SF_C
Subsystem2
RMS
RMS1
11.76
Display2
RMS
RMS
117.6
Display

**FIGURE 6.4**
Model of three-phase fully controlled SCR controller with star-connected resistive load and isolated neutral for α = 30°.



Block Parameters: Subsystem3

Firing Angle (mask)

Enter Firing Angle alfa in radians from 0 to 5pi / 6.

Parameters

Firing angle in radians

pi/(6)

Block Parameters: Subsystem1

Three Phase AC Data (mask)

Enter RMS Line to Neutral Voltage in Volts and Frequency In Hertz

Parameters

RMS Line to Neutral Voltage in Volts

120

Frequency in Hertz

60

Block Parameters: Subsystem

Load Resistance Data (mask)

Enter the Load Resistance in Ohms per Phase.

Parameters

Enter the per Phase Load Resistance in Ohms

10

OK
Cancel
Help
Apply

**FIGURE 6.5**
Model of three-phase fully controlled SCR controller with star-connected resistive load and isolated neutral for α = 30° with interactive blocks.

$$\left.\begin{aligned}
\text{SF\_A} &= +1 \quad \text{for} \quad \alpha \le \omega.t \le (\pi+\alpha)\\
&= -1 \quad \text{for} \quad (\pi+\alpha) \le \omega.t \le (2\pi+\alpha)\\
\text{SF\_B} &= +1 \quad \text{for} \quad \left(\frac{2\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{5\pi}{3}+\alpha\right)\\
&= -1 \quad \text{for} \quad \left(\frac{5\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{8\pi}{3}+\alpha\right)\\
\text{SF\_C} &= +1 \quad \text{for} \quad \left(\frac{4\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{7\pi}{3}+\alpha\right)\\
&= -1 \quad \text{for} \quad \left(\frac{7\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{10\pi}{3}+\alpha\right)
\end{aligned}\right] \tag{6.6}$$

The model of the back-to-back connected thyristors in the three phases and the star-connected resistive load is shown in Figure 6.6d. The development of this model in Figure 6.6d is given as follows:

Referring to the topmost four-input mux corresponding to Phase A, the inputs $u(1)$ to $u(4)$ are, respectively, peak line-to-neutral voltage $V_m$ ($\sqrt{2}.V_S$), supply angular frequency ω, time $t$ and SCR firing angle α. The Fcn block at the top marked 'VAN' generates $v_{AN}$ given by Equation 6.1, while the bottom Fcn block generates an attenuated value of $v_{AN}$ lagging by the firing angle α. The two Fcn blocks corresponding to Phase B and C, respectively, generate

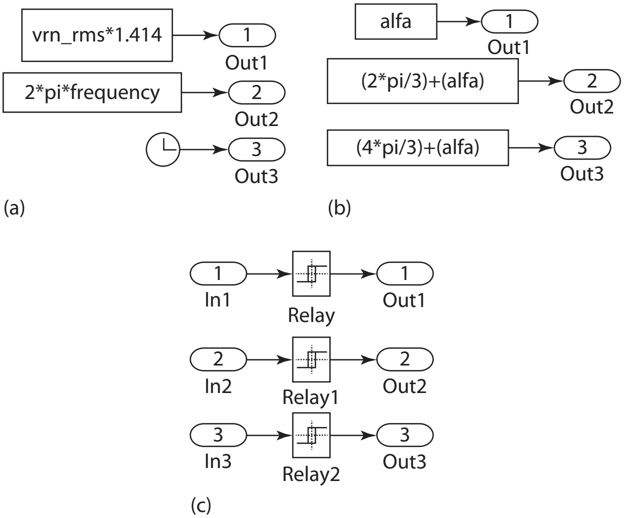

vrn_rms*1.414
1
Out1
2*pi*frequency
2
Out2
3
Out3
(a)
alfa
1
Out1
(2*pi/3)+(alfa)
2
Out2
(4*pi/3)+(alfa)
3
Out3
(b)
1
In1
Relay
1
Out1
2
In2
Relay1
2
Out2
3
In3
Relay2
3
Out3
(c)

**FIGURE 6.6**
(a–d) Three-phase SCR controller with star-connected resistive load and isolated neutral–model subsystems.

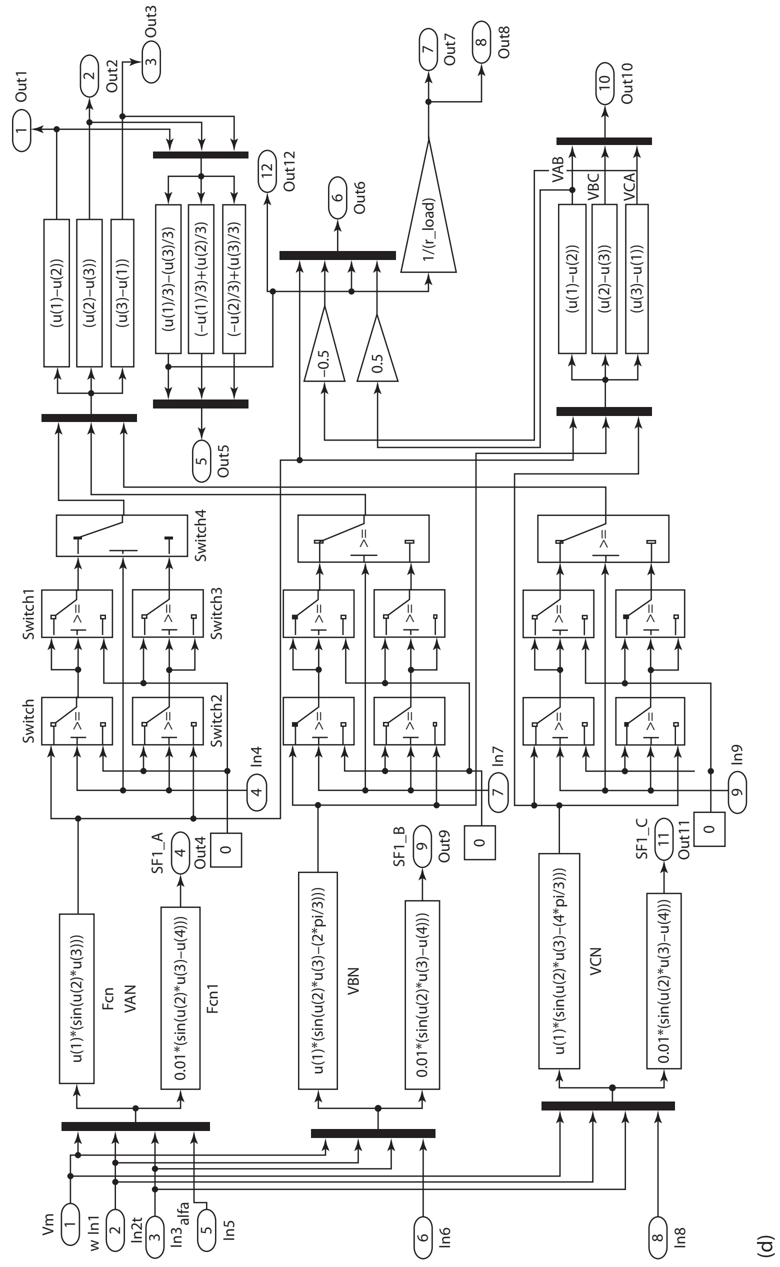

Vm
1
w In1
2
In2t
3
In3alfa
5
In5
6
In6
8
In8
u(1)*(sin(u(2)*u(3)))
Fcn
VAN
0.01*(sin(u(2)*u(3)−u(4)))
Fcn1
SF1_A
4
Out4
u(1)*(sin(u(2)*u(3)−(2*pi/3)))
VBN
0.01*(sin(u(2)*u(3)−u(4)))
SF1_B
9
Out9
u(1)*(sin(u(2)*u(3)−(4*pi/3)))
VCN
0.01*(sin(u(2)*u(3)−u(4)))
SF1_C
11
Out11
0
4
In4
7
In7
9
In9
Switch
Switch1
Switch2
Switch3
Switch4
>=
(u(1)−u(2))
(u(2)−u(3))
(u(3)−u(1))
1
Out1
2
Out2
3
Out3
(u(1)/3)−(u(3)/3)
(−u(1)/3)+(u(2)/3)
(−u(2)/3)+(u(3)/3)
5
Out5
12
Out12
−0.5
0.5
6
Out6
1/(r_load)
7
Out7
8
Out8
VAB
VBC
VCA
10
Out10
(d)

**FIGURE 6.6**
Continued

$v_{BN}$ given by Equation 6.1 and attenuated $v_{BN}$ lagging by $[(2.\pi/3)+\alpha]$, $v_{CN}$ given by Equation 6.1 and attenuated $v_{CN}$ lagging by $[(4.\pi/3)+\alpha]$. The bottom mux output of each phase marked SF1_A, SF1_B and SF1_C in Figure 6.6d are given as input In1, In2 and In3 to the three relays in Figure 6.6c. All three relays output 1 when the respective input crosses zero and becomes positive and output −1 when the respective input crosses zero and becomes negative.

Considering Phase A for clarity, SF1_A is passed as the $u(2)$ input to the threshold switches marked Switch and Switch2 in Figure 6.6d. The VAN output of the Fcn block is passed as the $u(1)$ input to Switch and the $u(3)$ input to Switch2. Zero is passed to the $u(3)$ input of Switch and the $u(1)$ input to Switch2. The output of Switch is passed to the $u(1)$ and $u(2)$ input of Switch1 and its $u(3)$ input is zero. The output of Switch2 is passed to the $u(2)$ and $u(3)$ input of Switch3 and its $u(1)$ input is zero. The output of Switch1 and Switch3 are passed as the $u(1)$ and $u(3)$ input to Switch4 and its $u(2)$ input is *SF_A*. Switch, Switch1, Switch2, Switch3 and Switch4 all have a threshold value of zero and all these switches' output correspond to $u(1)$ when $u(2)$ is greater than or equal to zero, else all these switches' output correspond to the $u(3)$ input. The threshold switches corresponding to Phase B and Phase C operate on the same principle as for Phase A.

Referring to the threshold switches in Phase A shown in Figure 6.6d and noting the definition of SF_A in Equation 6.6, the output of various threshold switches can be explained as follows.

Switch and Switch2 have the following output given by Equations 6.7 and 6.8, respectively:

$$\begin{aligned}\text{Switch output} &= +V_m.\sin(\omega t) \quad \text{for} \quad \alpha \le \omega t \le (\pi+\alpha)\\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.7}$$

$$\begin{aligned}\text{Switch2 output} &= -V_m.\sin(\omega t) \quad \text{for} \quad (\pi+\alpha) \le \omega t \le (2\pi+\alpha)\\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.8}$$

Switch1 and Switch3 have the following output given by Equations 6.9 and 6.10, respectively:

$$\begin{aligned}\text{Switch1 output} &= +V_m.\sin(\omega t) \quad \text{for} \quad \alpha \le \omega t \le \pi\\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.9}$$

$$\begin{aligned}\text{Switch3 output} &= -V_m.\sin(\omega t) \quad \text{for} \quad (\pi+\alpha) \le \omega t \le 2\pi\\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.10}$$

Switch4 has the following output given by Equation 6.11:

$$
\begin{aligned}
\text{Switch4 output} &= +V_m.\sin(\omega t) \quad \text{for} \quad \alpha \le \omega t \le \pi \\
&= -V_m.\sin(\omega t) \quad \text{for} \quad (\pi+\alpha) \le \omega t \le 2\pi \\
&= 0 \quad \text{for} \quad \text{other time intervals}
\end{aligned}
\tag{6.11}
$$

The Switch4 output of Phase A and the corresponding Switch output of Phase B and Phase C are connected to a three-input mux as shown in Figure 6.6d. The three Fcn blocks calculate the three-phase line-to-line voltage across the star-connected resistive load using the following formula:

$$
\begin{bmatrix} v_{L1L2} \\ v_{L2L3} \\ v_{L3L1} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} v_{L1N} \\ v_{L2N} \\ v_{L3N} \end{bmatrix} = \begin{bmatrix} u(1)-u(2) \\ u(2)-u(3) \\ u(3)-u(1) \end{bmatrix} \tag{6.12}
$$

In Equation 6.12, $L1$, $L2$, $L3$ and $N$ correspond to the terminals A, B, C and N as marked in Figure 6.1. In Figure 6.6d, Out1, Out2 and Out3 correspond to these line-to-line voltages across the star-connected load. These three voltages are given to another set of three-input mux as shown in Figure 6.6d. The three Fcn blocks connected to this mux calculates the line-to-neutral voltages across the star-connected resistive load using the following formula:

$$
\begin{bmatrix} v_{L1n} \\ v_{L2n} \\ v_{L3n} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & 0 & \frac{-1}{3} \\ \frac{-1}{3} & \frac{1}{3} & 0 \\ 0 & \frac{-1}{3} & \frac{1}{3} \end{bmatrix} * \begin{bmatrix} v_{L1L2} \\ v_{L2L3} \\ v_{L3L1} \end{bmatrix} = \begin{bmatrix} \frac{u(1)}{3} - \frac{u(3)}{3} \\ \frac{-u(1)}{3} + \frac{u(2)}{3} \\ \frac{-u(2)}{3} + \frac{u(3)}{3} \end{bmatrix} \tag{6.13}
$$

In Equation 6.13, $n$ is the load neutral point as shown in Figure 6.1. The line-to-neutral voltage $v_{L1n}$ is multiplied by 1/(r_load) to obtain the load current through each of the resistors.

### 6.2.2 Simulation Results

The simulation of the fully controlled three-phase AC controller with star-connected load and neutral isolated was carried out using the ode23t (mod. stiff/trapezoidal) solver for various firing angles α of π/6, π/4, π/3, π/2 and 2.π/3 rad [7]. The data used for this controller is given in Table 6.1 [1]. The simulation results for firing angles α of π/6, π/4, π/3, π/2 and 2.π/3 rad are shown from Figures 6.7a–f to Figure 6.11a–f. The names of the various waveforms are given at the top of each simulation result. The simulation results for various firing angles α are tabulated in Table 6.2. The RMS line-to-neutral voltage

**TABLE 6.1**

Data for Three-Phase AC Controller with Star-Connected Resistive Load

| Sl. No. | RMS Line-to-Neutral Voltage (V) | Frequency (Hz) | Firing Angle $\alpha$ (rad) | Per Phase Load Resistance ($\Omega$) |
|---|---|---|---|---|
| 1 | 120 | 60 | $\pi/6$ | 10 |
| 2 | 120 | 60 | $\pi/4$ | 10 |
| 3 | 120 | 60 | $\pi/3$ | 10 |
| 4 | 120 | 60 | $\pi/2$ | 10 |
| 5 | 120 | 60 | $2.\pi/3$ | 10 |

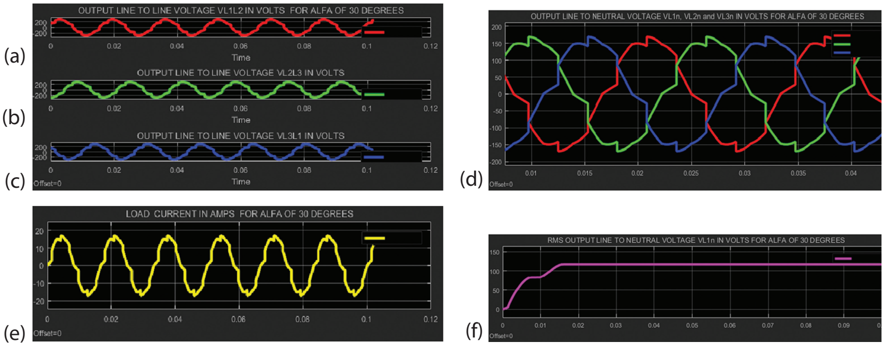


**FIGURE 6.7**
(a–f) Three-phase AC to AC controller with star-connected resistive load: simulation results for $\alpha = \pi/6$ rad.

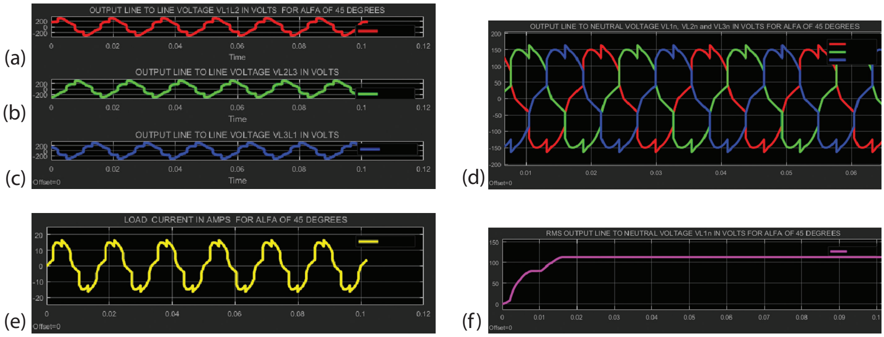


**FIGURE 6.8**
(a–f) Three-phase AC to AC controller with star-connected resistive load: simulation results for $\alpha = \pi/4$ rad.

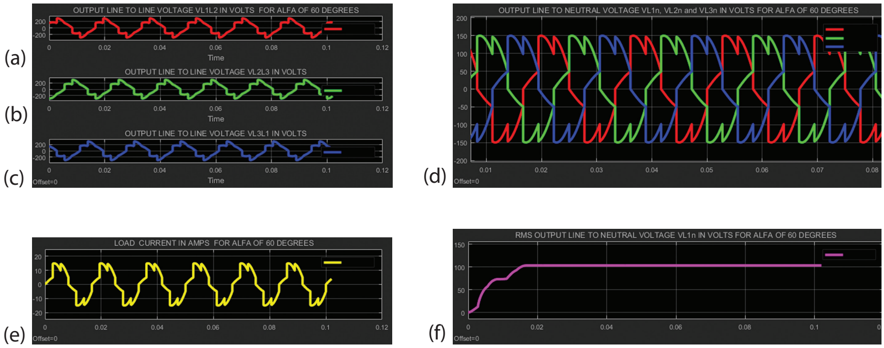


**FIGURE 6.9**
(a–f) Three-phase AC to AC controller with star-connected resistive load: simulation results for $\alpha = \pi/3$ rad.

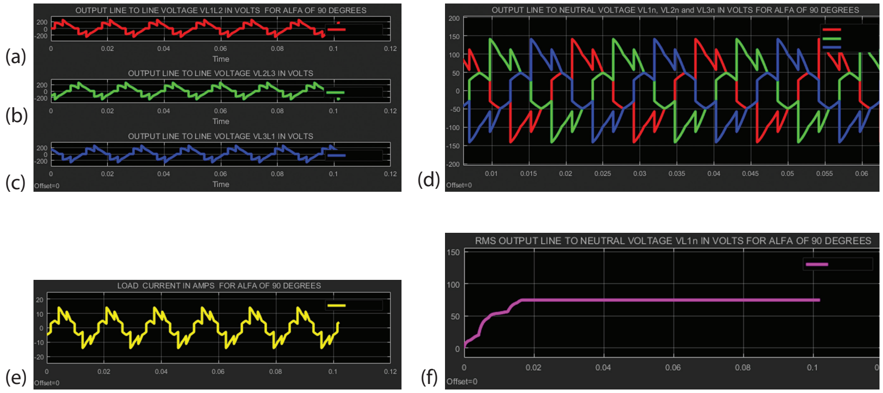


**FIGURE 6.10**
(a–f) Three-phase AC to AC controller with star-connected resistive load: simulation results for $\alpha = \pi/2$ rad.

across resistive load, calculated by using Equations 6.3 through 6.5, and also the RMS load current by calculation are given in Table 6.3.

Comparison of the values given in Tables 6.2 and 6.3 reveals that the percentage error for load current and RMS line-to-neutral output voltage is very small for $\alpha = \pi/6$, $\pi/4$ and $\pi/3$ rad and this value is in the range of 15.16% for $\alpha = \pi/2$ rad and −27.8% for $\alpha = 2\pi/3$ rad.

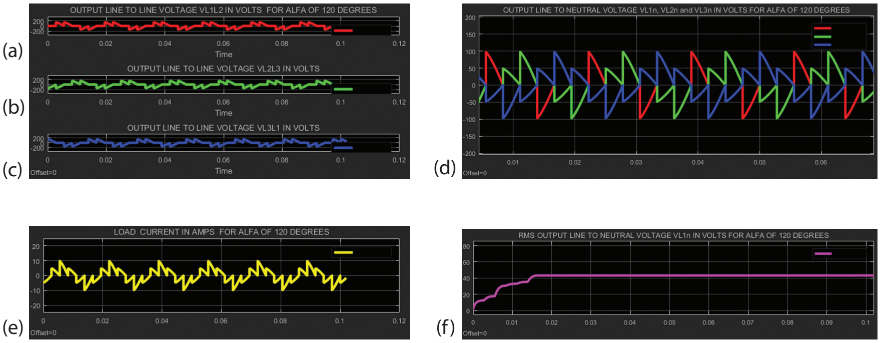


**FIGURE 6.11**
(a–f) Three-phase AC to AC controller with star-connected resistive load: simulation results for $\alpha = 2.\pi/3$ rad.

**TABLE 6.2**
Simulation Results for Three-Phase AC Controller with Star-Connected Resistive Load

| Sl. No. | Line-to-Neutral Voltage (V) | Frequency (Hz) | Firing Angle α (rad) | Per Phase Load Resistance (Ω) | RMS Line-to-Neutral Load Voltage (V) | RMS Load Current (A) |
|---|---|---|---|---|---|---|
| 1 | 120 | 60 | π/6 | 10 | 117.6 | 11.76 |
| 2 | 120 | 60 | π/4 | 10 | 112.5 | 11.25 |
| 3 | 120 | 60 | π/3 | 10 | 103.2 | 10.32 |
| 4 | 120 | 60 | π/2 | 10 | 74.82 | 7.482 |
| 5 | 120 | 60 | 2.π/3 | 10 | 43.32 | 4.332 |

**TABLE 6.3**
Calculated Values for Three-Phase AC Controller with Star-Connected Resistive Load

| Sl. No. | Line-to-Neutral Voltage (V) | Frequency (Hz) | Firing Angle α (rad) | Per Phase Load Resistance (Ω) | RMS Line-to-Neutral Load Voltage (V) | RMS Load Current (A) |
|---|---|---|---|---|---|---|
| 1 | 120 | 60 | π/6 | 10 | 117.38 | 11.738 |
| 2 | 120 | 60 | π/4 | 10 | 111.53 | 11.153 |
| 3 | 120 | 60 | π/3 | 10 | 100.88 | 10.088 |
| 4 | 120 | 60 | π/2 | 10 | 64.97 | 6.497 |
| 5 | 120 | 60 | 2.π/3 | 10 | 60 | 6.00 |

## 6.3 Analysis of a Fully Controlled Three-Phase AC Voltage Controller in Series with Resistive Load Connected in Delta

The three-phase three-wire AC voltage controller with back-to-back SCRs in series with resistive load connected in delta is shown in Figure 6.12 [1–4]. By varying the firing angle α, the RMS current through the load can be varied.

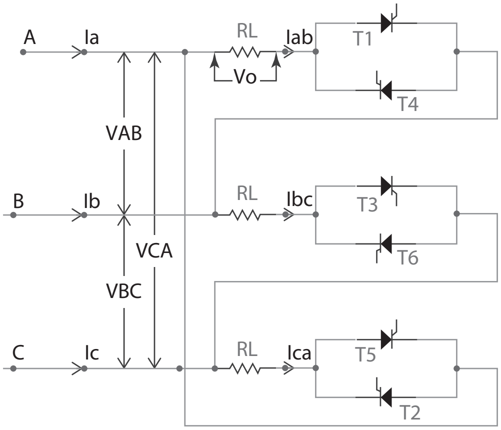

A
Ia
RL
Iab
T1
Vo
T4
VAB
B
Ib
RL
Ibc
T3
T6
VCA
VBC
C
Ic
RL
Ica
T5
T2

**FIGURE 6.12**
Three-phase thyristor AC controller in series with resistive load in delta.

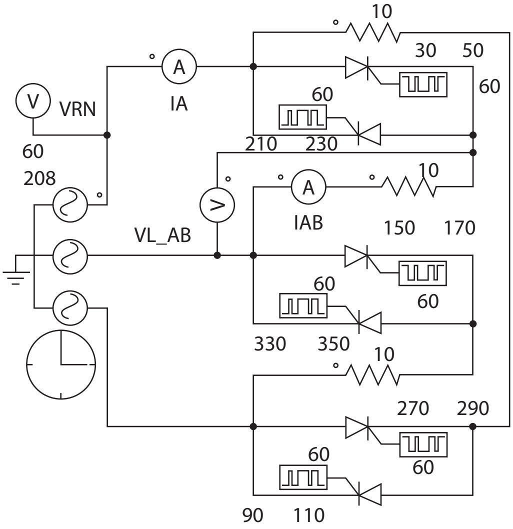

10
30
50
60
A
IA
V
VRN
60
60
208
210
230
10
A
IAB
150
170
VL_AB
60
60
330
350
10
270
290
60
60
90
110

**FIGURE 6.13**
Three-phase AC controller in series with resistive load in delta.

The firing sequence is T1, T2, T3, T4, T5 and T6. The RMS output voltage is derived in Equation 6.15. The three-phase line-to-line AC voltage is defined in Equation 6.14.

$$\left.\begin{aligned} v_{AB} &= \sqrt{2} * V_S * \sin(\omega.t) \\ v_{BC} &= \sqrt{2} * V_S * \sin\left(\omega.t - \frac{2\pi}{3}\right) \\ v_{CA} &= \sqrt{2} * V_S * \sin\left(\omega.t + \frac{2\pi}{3}\right) \end{aligned}\right] \tag{6.14}$$

In Equation 6.14, $v_{AB}$, $v_{BC}$, $v_{CA}$ are the instantaneous voltages and $V_S$ is the RMS line-to-line voltage. As the load resistance is in series with the back-to-back connected SCRs forming a delta configuration, the RMS phase voltage $V_O$ can be derived as follows, for any firing angle α.

$$\begin{aligned} V_{O\_RMS} &= \sqrt{\left[\frac{1}{\pi} * \int_{\alpha}^{\pi} 2V_S^2 * \sin^2(\omega.t).d(\omega.t)\right]} \\ &= V_S * \sqrt{\left[1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}\right]} \end{aligned} \tag{6.15}$$

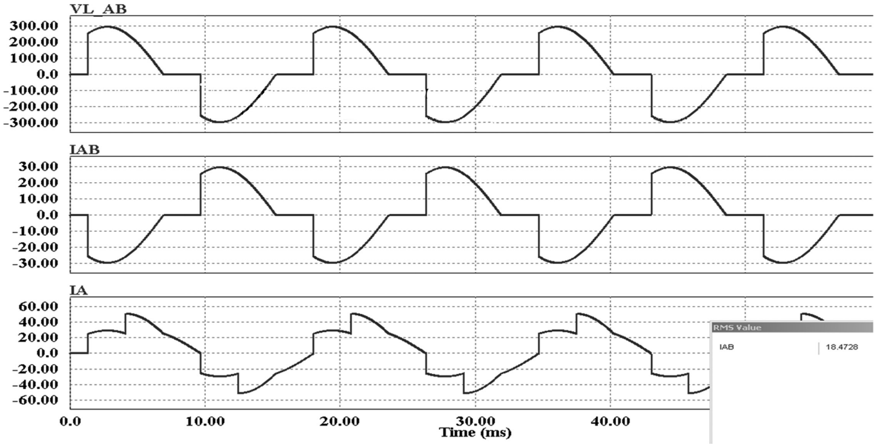


**FIGURE 6.14**
Three-phase AC controller in series with resistive load in delta: output waveforms for $\alpha = \pi/6$ rad.

The range of firing angles is $0 \leq \alpha \leq \pi$. In Figure 6.12, $i_{ab}$, $i_{bc}$ and $i_{ca}$ are the phase currents through the load. Also, $i_a = i_{ab} - i_{ca}$, $i_b = i_{bc} - i_{ab}$ and $i_c = i_{ca} - i_{bc}$ are the line currents.

A PSIM [5] circuit model of the three-phase AC to three-phase AC thyristor controller in series with resistive load connected in delta, for a firing angle of $\pi/6$ rad, is shown in Figure 6.13. The RMS line-to-line input voltage is 208 V and frequency is 60 Hz. The simulation results are shown in Figure 6.14. From simulation results, it is seen that the load current is 18.47 A for a firing angle of $\pi/6$ rad and the load voltage $V_{AB}$ is 184.7 V with a load resistance of 10 Ω.

### 6.3.1 Modelling of a Fully Controlled Three-Phase AC Voltage Controller in Series with Resistive Load Connected in Delta

This section describes the modelling of the three-phase delta-connected AC controller shown in Figure 6.12 [6]. The model for a firing angle $\alpha$ of $\pi/6$ rad is shown in Figure 6.15. The various dialogue boxes are shown in Figure 6.16 and the various subsystems in Figure 6.17a–d. The various subsystems are explained here:

Figure 6.17a corresponds to the dialogue box 'Three-Phase AC Supply Data' in Figure 6.16. In this dialogue box, the RMS line-to-line voltage in volts and the frequency in hertz are entered. The peak voltage $V_m$ and angular frequency $\omega$ are internally calculated. Figure 6.17b corresponds to the dialogue box 'Firing Pulse Generator' in Figure 6.16. The firing angle $\alpha$ in radians is entered in this dialogue box. Figure 6.17b has three constant blocks that generate $\alpha$, $[(2\pi/3)+\alpha]$ and $[(4\pi/3)+\alpha]$ for the three phases. Figure 6.17c generates the switch function SF for the three phases. The switch function corresponds to the firing pulses for the back-to-back connected thyristors in the three phases. These switch functions SF_A, SF_B and SF_C are defined as follows:

The dialogue box 'Load Resistance' in Figure 6.16 corresponds to Figure 6.17d. The load resistance value in ohms per phase is entered in this dialogue box. Figure 6.17d corresponds to the model of the back-to-back connected thyristors in the three phases in series with load resistors connected in delta. The development of this model in Figure 6.17d is given here:

Referring to the topmost four-input mux corresponding to Phase A, the inputs $u(1)$ to $u(4)$ are, respectively, peak line-to-line voltage $V_m$ $(\sqrt{2}.V_S)$, supply angular frequency $\omega$, time $t$ and firing angle $\alpha$. The function block at the top marked Fcn generates $v_{AB}$ given by Equation 6.14, while the bottom Fcn1 block generates attenuated $v_{AB}$ lagging $v_{AB}$ by the firing angle $\alpha$. The two Fcn blocks corresponding to Phase B and C, respectively, generate $v_{BC}$ given by Equation 6.14 and attenuated $v_{BC}$ lagging $v_{AB}$ by $[(2.\pi/3)+\alpha]$, $v_{CA}$ given by Equation 6.14 and attenuated $v_{CA}$ lagging $v_{AB}$ by $[(4.\pi/3)+\alpha]$.

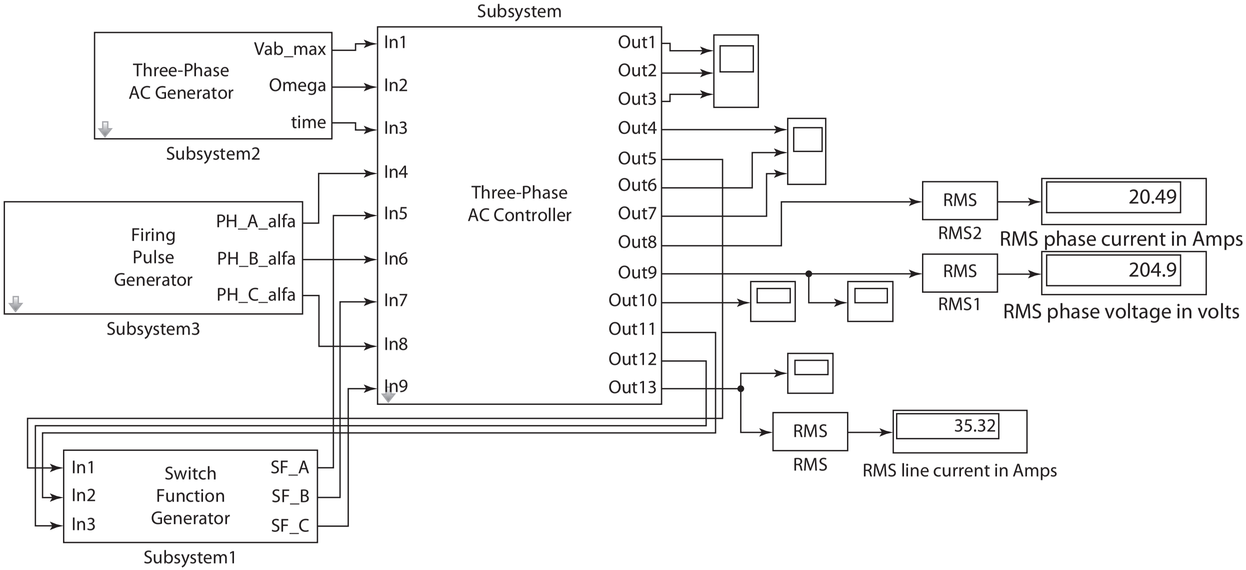
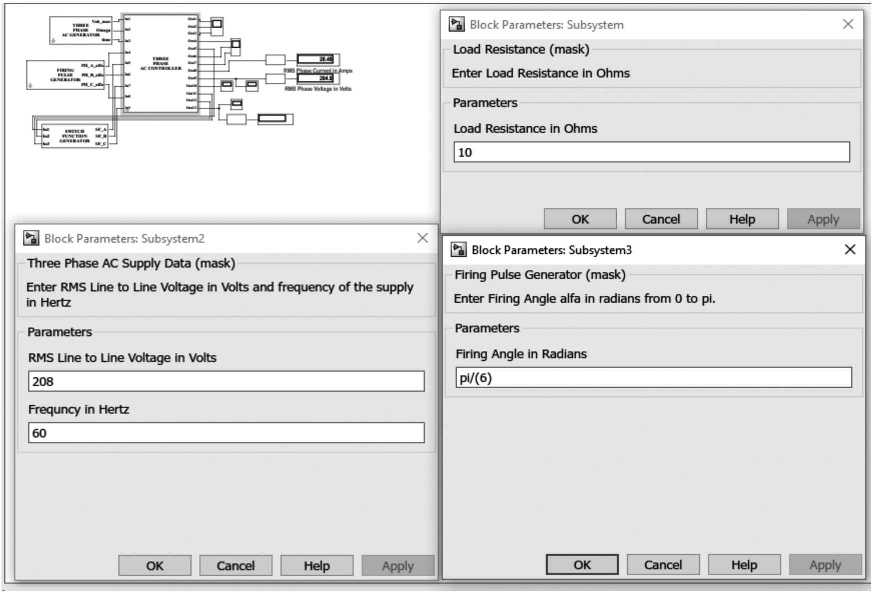

Subsystem
Three-Phase
AC Controller
In1
In2
In3
In4
In5
In6
In7
In8
In9
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
Out13
Three-Phase
AC Generator
Vab_max
Omega
time
Subsystem2
Firing
Pulse
Generator
PH_A_alfa
PH_B_alfa
PH_C_alfa
Subsystem3
Switch
Function
Generator
In1
In2
In3
SF_A
SF_B
SF_C
Subsystem1
RMS
RMS2
20.49
RMS phase current in Amps
RMS
RMS1
204.9
RMS phase voltage in volts
RMS
RMS
35.32
RMS line current in Amps

**FIGURE 6.15**
Three-phase AC controller: back-to-back thyristor in series with resistive load connected in delta.



Block Parameters: Subsystem

Load Resistance (mask)

Enter Load Resistance in Ohms

Parameters

Load Resistance in Ohms: 10

Block Parameters: Subsystem2

Three Phase AC Supply Data (mask)

Enter RMS Line to Line Voltage in Volts and frequency of the supply in Hertz

Parameters

RMS Line to Line Voltage in Volts: 208

Frequncy in Hertz: 60

Block Parameters: Subsystem3

Firing Pulse Generator (mask)

Enter Firing Angle alfa in radians from 0 to pi.

Parameters

Firing Angle in Radians: pi/(6)

OK
Cancel
Help
Apply

**FIGURE 6.16**
Three-phase AC controller: back-to-back thyristor in series with resistive load connected in delta with interactive blocks.

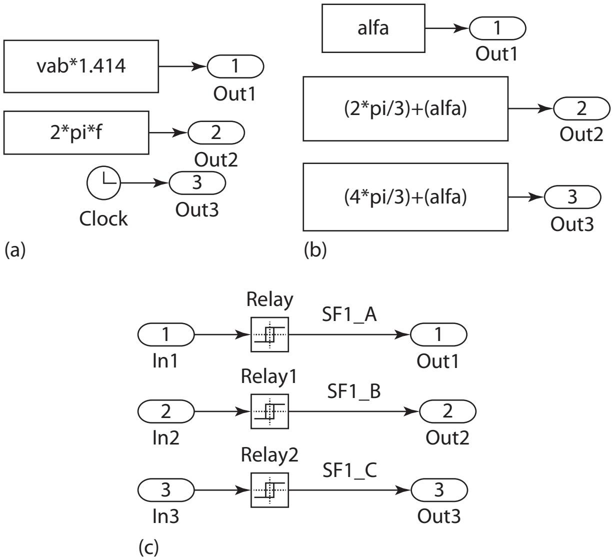

vab*1.414
1
Out1
2*pi*f
2
Out2
Clock
3
Out3
(a)
alfa
1
Out1
(2*pi/3)+(alfa)
2
Out2
(4*pi/3)+(alfa)
3
Out3
(b)
1
In1
Relay
SF1_A
1
Out1
2
In2
Relay1
SF1_B
2
Out2
3
In3
Relay2
SF1_C
3
Out3
(c)

**FIGURE 6.17**
(a–d) Three-phase AC controller: back-to-back thyristor in series with resistive load connected in delta–model subsystems.

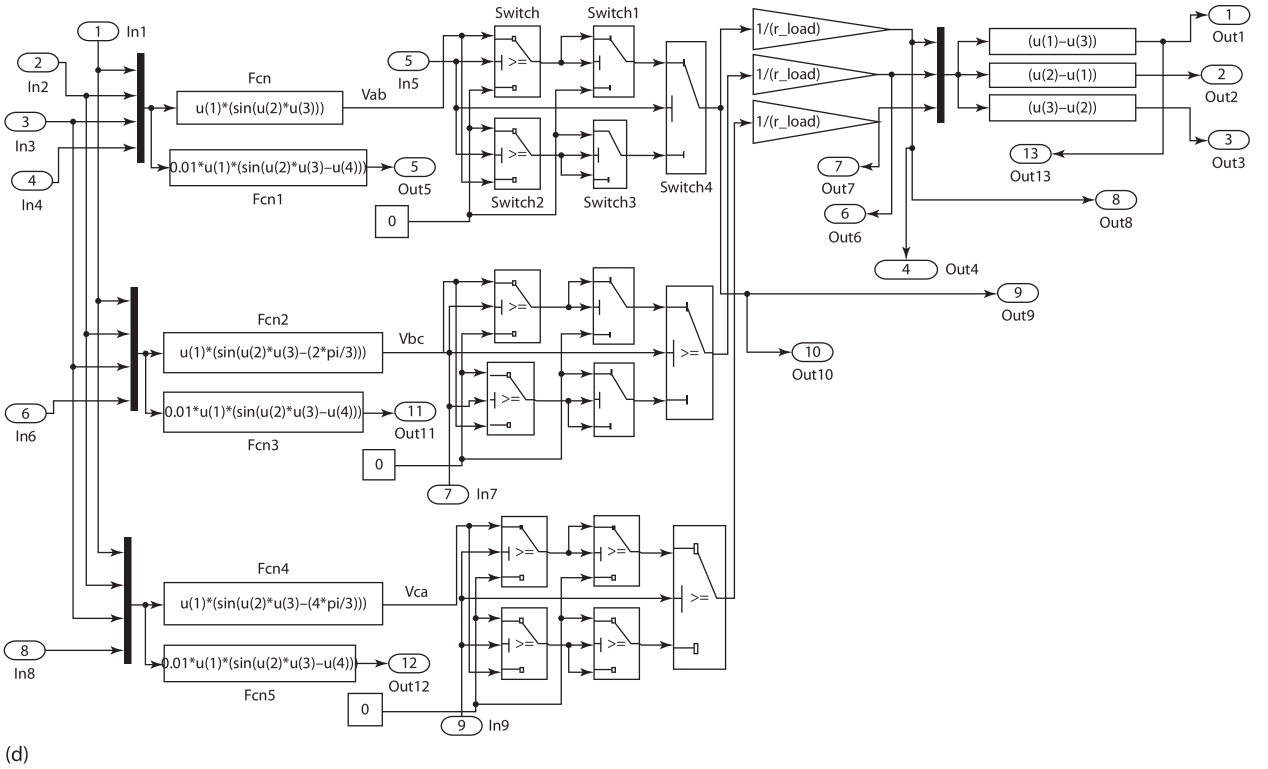

1 In1
2 In2
3 In3
4 In4
Fcn
u(1)*(sin(u(2)*u(3)))
Vab
0.01*u(1)*(sin(u(2)*u(3)−u(4)))
Fcn1
5 Out5
5 In5
0
Switch
Switch1
Switch2
Switch3
Switch4
>=
1/(r_load)
1/(r_load)
1/(r_load)
(u(1)−u(3))
(u(2)−u(1))
(u(3)−u(2))
1 Out1
2 Out2
3 Out3
13 Out13
7 Out7
6 Out6
8 Out8
4 Out4
9 Out9
10 Out10
Fcn2
u(1)*(sin(u(2)*u(3)−(2*pi/3)))
Vbc
0.01*u(1)*(sin(u(2)*u(3)−u(4)))
Fcn3
11 Out11
0
7 In7
6 In6
Fcn4
u(1)*(sin(u(2)*u(3)−(4*pi/3)))
Vca
0.01*u(1)*(sin(u(2)*u(3)−u(4)))
Fcn5
12 Out12
0
9 In9
8 In8
(d)

**FIGURE 6.17**
Continued

$$\left.\begin{aligned}
\text{SF\_A} &= +1 \quad \text{for} \quad \alpha \le \omega.t \le (\pi+\alpha)\\
&= -1 \quad \text{for} \quad (\pi+\alpha) \le \omega.t \le (2\pi+\alpha)\\
\text{SF\_B} &= +1 \quad \text{for} \quad \left(\frac{2\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{5\pi}{3}+\alpha\right)\\
&= -1 \quad \text{for} \quad \left(\frac{5\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{8\pi}{3}+\alpha\right)\\
\text{SF\_C} &= +1 \quad \text{for} \quad \left(\frac{4\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{7\pi}{3}+\alpha\right)\\
&= -1 \quad \text{for} \quad \left(\frac{7\pi}{3}+\alpha\right) \le \omega.t \le \left(\frac{10\pi}{3}+\alpha\right)
\end{aligned}\right] \tag{6.16}$$

The bottom function block output, that is, the output of Fcn1, Fcn3 and Fcn5 of each phase marked in Figure 6.17d are passed as input In1, In2 and In3 to the three relays in Figure 6.17c. All three relays output 1 when the respective input crosses zero and becomes positive, and output −1 when the respective input crosses zero and becomes negative.

Considering Phase A for clarity, SF_A is passed as the $u(2)$ input to the threshold switches marked Switch and Switch2 in Figure 6.17d. The output of the Fcn block is passed as the $u(1)$ input to Switch and the $u(3)$ input to Switch2. Zero is passed to the $u(3)$ input of Switch and the $u(1)$ input of Switch2. The output of Switch is passed to the $u(1)$ and $u(2)$ input of Switch1 and its $u(3)$ input is zero. The output of Switch2 is passed to the $u(2)$ and $u(3)$ input of Switch3 and its $u(1)$ input is zero. The output of Switch1 and Switch3 are passed as the $u(1)$ and $u(3)$ input to Switch4 and its $u(2)$ input is SF_A. Switch, Switch1, Switch2, Switch3 and Switch4 all have a threshold value of zero and all these switches' output correspond to $u(1)$ when $u(2)$ is greater than or equal to zero, else all these switches' output correspond to the $u(3)$ input. The threshold switches corresponding to Phase B and Phase C operate on the same principle as for Phase A.

Referring to the threshold switches in Phase A shown in Figure 6.17d and noting the definition of SF_A in Equation 6.16, the output of various threshold switches can be explained as follows:

Switch and Switch2 have the following output, given by Equation 6.17 and 6.18, respectively.

$$\begin{aligned}
\text{Switch output} &= +V_m.\sin(\omega t) \quad \text{for} \quad \alpha \le \omega t \le (\pi+\alpha)\\
&= 0 \quad \text{for} \quad \text{other time intervals}
\end{aligned} \tag{6.17}$$

$$\begin{aligned}
\text{Switch2 output} &= -V_m.\sin(\omega t) \quad \text{for} \quad (\pi+\alpha) \le \omega t \le (2\pi+\alpha)\\
&= 0 \quad \text{for} \quad \text{other time intervals}
\end{aligned} \tag{6.18}$$

Switch1 and Switch3 have the following output, given by Equations 6.19 and 6.20, respectively:

$$\begin{aligned}\text{Switch1 output} &= +V_m.\sin(\omega t) \quad \text{for} \quad \alpha \le \omega t \le \pi \\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.19}$$

$$\begin{aligned}\text{Switch3 output} &= -V_m.\sin(\omega t) \quad \text{for} \quad (\pi+\alpha) \le \omega t \le 2\pi \\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.20}$$

Switch4 has the following output, given by Equation 6.21:

$$\begin{aligned}\text{Switch4 output} &= +V_m.\sin(\omega t) \quad \text{for} \quad \alpha \le \omega t \le \pi \\ &= -V_m.\sin(\omega t) \quad \text{for} \quad (\pi+\alpha) \le \omega t \le 2\pi \\ &= 0 \quad \text{for} \quad \text{other time intervals}\end{aligned} \tag{6.21}$$

The Switch4 output in Figure 6.17d corresponds to the phase voltage $V_O$ across the load resistor. This $V_O$ is multiplied by 1/(r_load) using gain multiplier blocks to obtain the phase currents $i_{ab}$, $i_{bc}$ and $i_{ca}$ through the load resistor. These respective phase currents are passed to a three-input mux. The three Fcn blocks performing $(u(1)-u(3))$, $(u(2)-u(1))$ and $(u(3)-u(2))$ output the line currents $i_a$, $i_b$ and $i_c$.

### 6.3.2 Simulation Results

Simulation of the fully controlled three-phase AC controller in series with resistive load connected in delta was carried out using the ode23t (mod. stiff/trapezoidal) solver for various firing angles α of π/6, π/4, π/3, π/2, 2.π/3 and π rad [7]. The data used for this controller are given in Table 6.4 [1]. The simulation results for firing angles α of π/6, π/4, π/3, π/2, 2.π/3 and π rad are shown from Figure 6.18a–h to Figure 6.23a–h, respectively.

**TABLE 6.4**

Data for Three-Phase AC Controller with Delta-Connected Resistive Load

| Sl. No. | RMS Line-to-Line Supply Voltage (V) | Frequency Hz | Firing Angle α (rad) | Per Phase Load Resistance (Ω) |
|---|---|---|---|---|
| 1 | 208 | 60 | π/6 | 10 |
| 2 | 208 | 60 | π/4 | 10 |
| 3 | 208 | 60 | π/3 | 10 |
| 4 | 208 | 60 | π/2 | 10 |
| 5 | 208 | 60 | 2.π/3 | 10 |
| 6 | 208 | 60 | π | 10 |

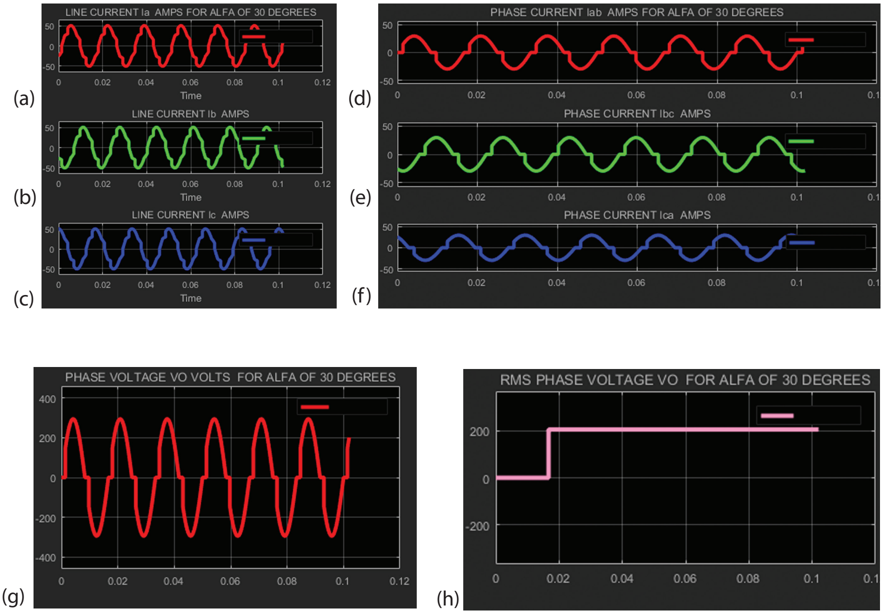


**FIGURE 6.18**
(a–h) Three-phase AC controller with resistive load in delta: simulation results for $\alpha = \pi/6$ rad.

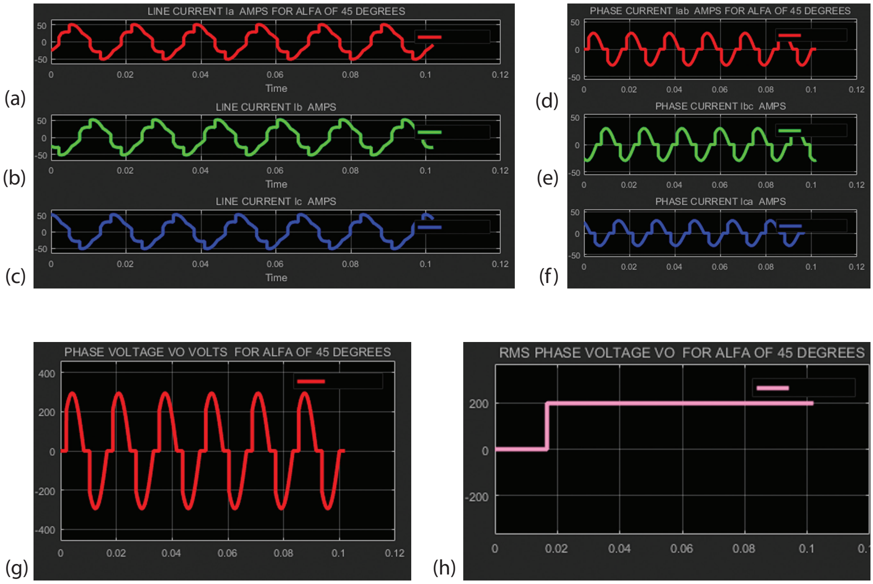


**FIGURE 6.19**
(a–h) Three-phase AC controller with resistive load in delta: simulation results for $\alpha = \pi/4$ rad.

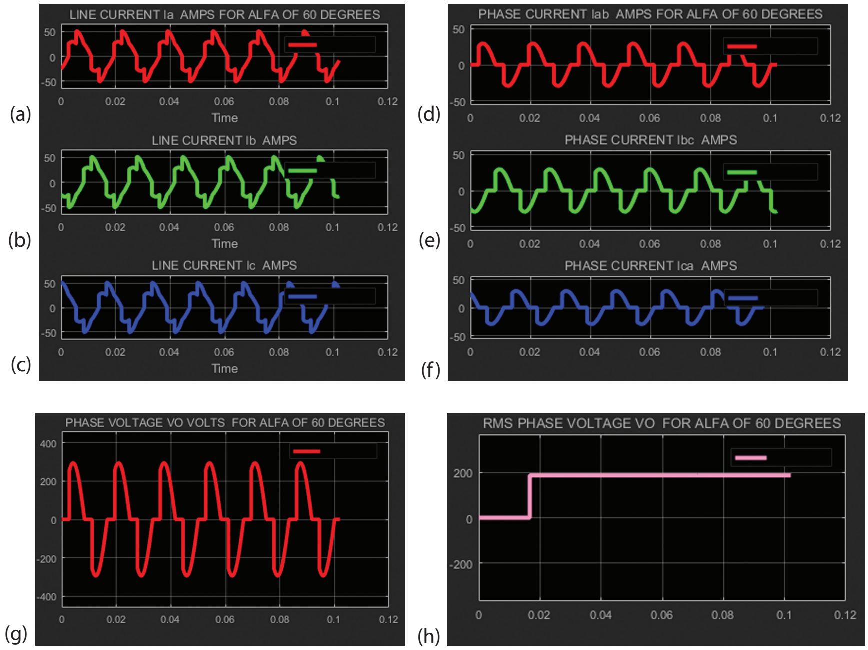


**FIGURE 6.20**
(a–h) Three-phase AC controller with resistive load in delta: simulation results for $\alpha = \pi/3$ rad.

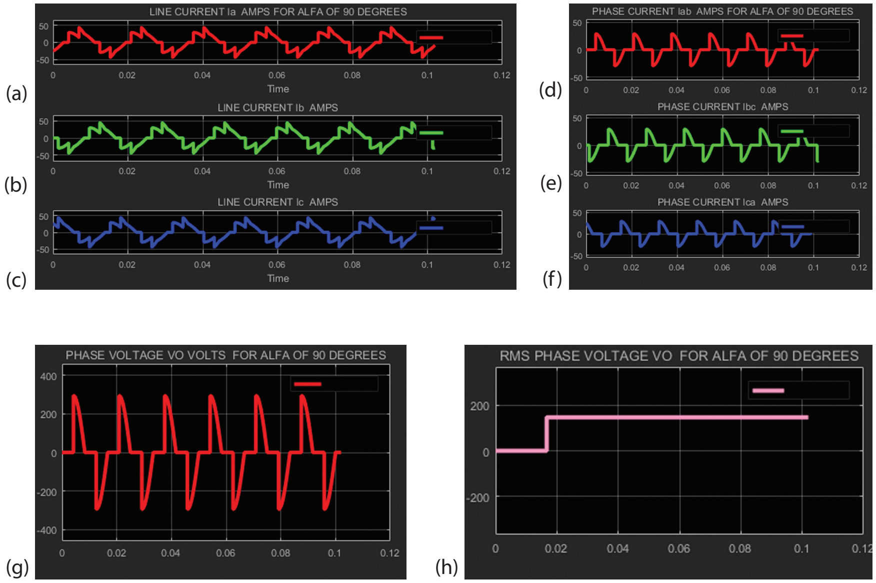


**FIGURE 6.21**
(a–h) Three-phase AC controller with resistive load in delta: simulation results for $\alpha = \pi/2$ rad.

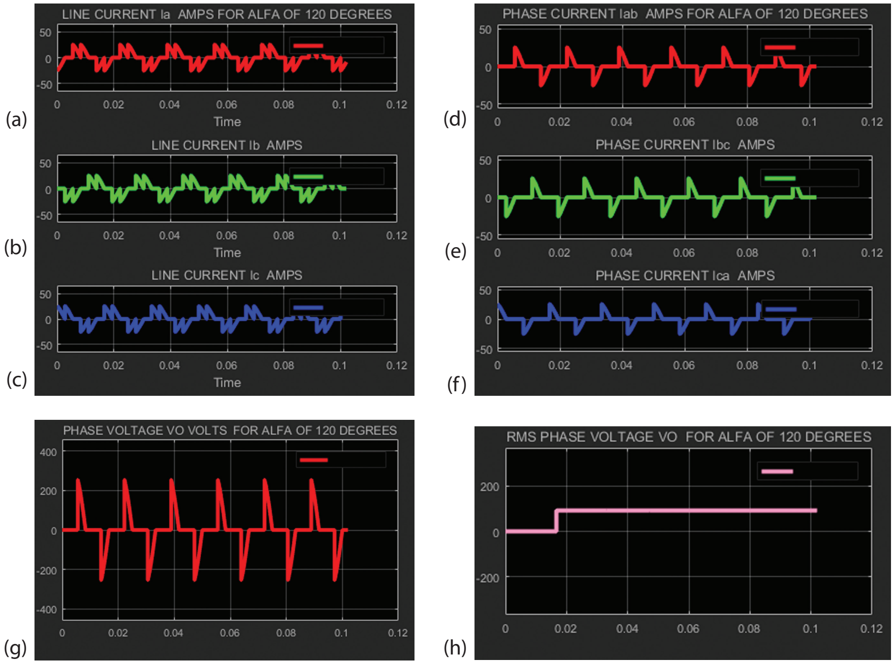


**FIGURE 6.22**
(a–h) Three-phase AC controller with resistive load in delta: simulation results for $\alpha = 2.\pi/3$ rad.

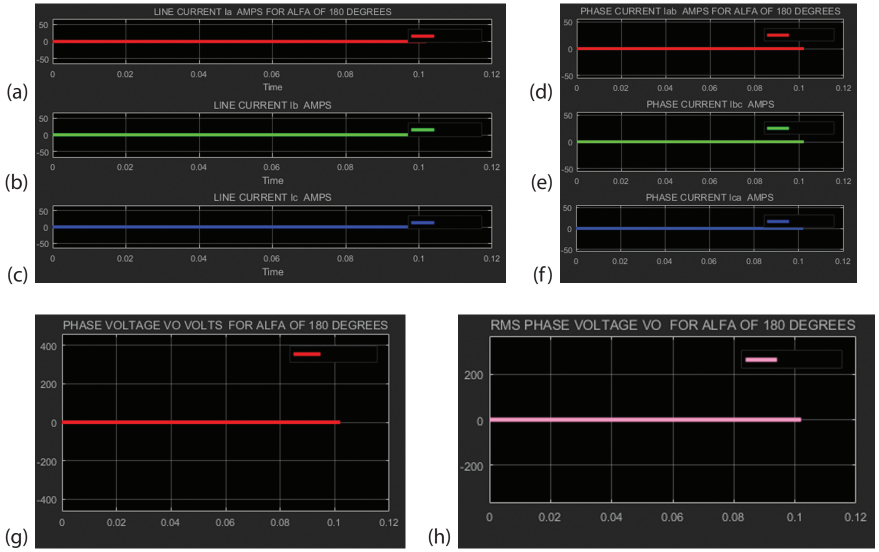


**FIGURE 6.23**
(a–h) Three-phase AC controller with resistive load in delta: simulation results for $\alpha = \pi$ rad.

**TABLE 6.5**

Simulation Results for Three-Phase AC Controller in Series with Resistive Load Connected in Delta

| Sl. No. | RMS Line-to-Line Input Voltage (V) | Frequency (Hz) | Firing Angle α (rad) | Per Phase Load Resistance (Ω) | RMS Load Voltage $V_O$ (V) | RMS Load Current $i_{ab}$ (A) |
|---|---|---|---|---|---|---|
| 1 | 208 | 60 | π/6 | 10 | 204.9 | 20.49 |
| 2 | 208 | 60 | π/4 | 10 | 198.3 | 19.83 |
| 3 | 208 | 60 | π/3 | 10 | 186.5 | 18.65 |
| 4 | 208 | 60 | π/2 | 10 | 147.1 | 14.71 |
| 5 | 208 | 60 | 2.π/3 | 10 | 91.96 | 9.196 |
| 6 | 208 | 60 | π | 10 | 0 | 0 |

**TABLE 6.6**

Calculated Values for Three-Phase AC Controller in Series with Resistive Load Connected in Delta

| Sl. No. | RMS Line-to-Line Input Voltage (V) | Frequency (Hz) | Firing Angle α (rad) | Per Phase Load Resistance (Ω) | RMS Load Voltage $V_O$ (V) | RMS Load Current $i_{ab}$ (A) |
|---|---|---|---|---|---|---|
| 1 | 208 | 60 | π/6 | 10 | 204.978 | 20.497 |
| 2 | 208 | 60 | π/4 | 10 | 198.327 | 19.832 |
| 3 | 208 | 60 | π/3 | 10 | 186.56 | 18.65 |
| 4 | 208 | 60 | π/2 | 10 | 147.078 | 14.7078 |
| 5 | 208 | 60 | 2.π/3 | 10 | 91.968 | 9.1968 |
| 6 | 208 | 60 | π | 10 | 0 | 0 |

The simulation results and the calculated values for various firing angles α for the three-phase back-to-back connected thyristor AC controller with series-connected resistive load in delta are shown in Tables 6.5 and 6.6, respectively [6].

## 6.4 Conclusions

System models for three-phase back-to-back connected thyristor AC controllers in series with lines connected to star-connected resistive load with isolated neutral, and also for three-phase back-to-back connected thyristor AC controller in series with resistive load connected in delta are developed, and their simulation and theoretically calculated results are presented. The switching function concept is used in these two models. It is seen from

Tables 6.2 and 6.3 that as the firing angle α increases, the percentage error between the theoretical and simulated results for line-to-neutral voltage across the load resistor increases [6]. Comparison of the values given in Tables 6.2 and 6.3 reveals that the percentage error for load current and RMS line-to-neutral output voltage is very small for $\alpha = \pi/6$, $\pi/4$ and $\pi/3$ rad and this value is in the range of 15.16% for $\alpha = \pi/2$ rad and −27.8% for $\alpha = 2\pi/3$ rad. It is also seen from Tables 6.5 and 6.6 that for the various firing angles α, the percentage error between the theoretical and simulated values for output voltage across load and load current per phase is negligible [6].

## References

1. M.H. Rashid: *Power Electronics Circuits, Devices and Applications*, Upper Saddle River, NJ: Pearson Education, Pearson Prentice Hall, 2004.
2. M.H. Rashid [Ed.]: *Power Electronics Handbook*, Burlington, MA: Elsevier, 2011.
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4. A.M. Trzynadlowski: *Introduction to Modern Power Electronics*, Hoboken, NJ: John Wiley, 2010; pp. 199–209.
5. Powersim Inc.: “PSIM demo version 10.0”, 2015.
6. N.P.R. Iyer: “MATLAB/SIMULINK modules for modelling and simulation of power electronic converters and electric drives”, M.E. by research thesis, University of Technology Sydney, NSW, Australia, 2006, Chapter 6.
7. The Mathworks Inc.: “MATLAB/Simulink” Release notes, version 8.8, R2016b, 2016.

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# 7

# *Interactive Modelling of an Switched Mode Power Supply Using Buck Converter*

## 7.1 Introduction

Switched mode power supplies (SMPS) are used to obtain a regulated DC output voltage from an unregulated DC input voltage. Here, the output voltage $V_O$ is compared with a reference voltage $V_{REF}$ and the difference voltage, called *error voltage* ($V_{ERR}$), is compared with a high-frequency triangle carrier signal $V_c$ to produce gate pulses to drive the buck converter semiconductor switch. This semiconductor switch may be a BJT, MOSFET or IGBT. Depending on the value of $V_O$, the duty cycle of the pulse width modulation (PWM) switching pulses adjust to maintain $V_O$ almost nearly constant, irrespective of variations in the input DC voltage $V_s$. In this type of SMPS, the buck converter is always operated in the continuous conduction mode (CCM). The switching function concept is used to model the buck converter SMPS.

## 7.2 Principle of Operation of Switched Mode Power Supply

Figure 7.1 gives the general block diagram of the SMPS using a buck converter. Referring to Figure 7.1, the buck converter output $V_O$ is attenuated using a potential divider and the resulting output $V_{POT}$ is subtracted from the reference input $V_{REF}$ using a difference amplifier to obtain the error output $V_{ERR}$. This $V_{ERR}$ output is compared with triangle carrier $V_c$ in an op-amp comparator to obtain the PWM switching pulses $V_g$ to drive the buck converter semiconductor switch. The switch SS1 is used to select the direct mode or PI controller mode. The PI controller in Figure 7.1 is used to reduce the peak value of oscillations and its number of cycles in the output voltage $V_O$. Depending on the value of $V_O$, the duty cycle of the PWM switching pulses adjusts to maintain the output voltage $V_O$ almost nearly constant, irrespective of variations in the input DC voltage $V_S$ within a given range [1–6].

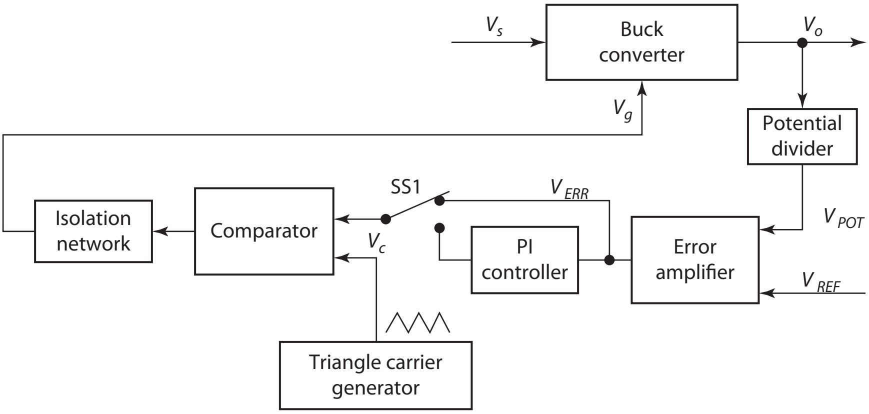


**FIGURE 7.1**
General model of the buck converter SMPS.

Simulation of SMPS using a buck converter was carried out using PSIM [7]. The parameters of the SMPS used for simulation are shown in Table 7.1.

The buck converter circuit simulation schematics using PSIM 6.1, without and with a PI controller, are shown in Figure 7.2a, b, respectively. The Gain block *K* with value −1 shown in Figure 7.2a, b is the inverting op-amp (a 10K resistor between the inverting pin and the PI controller; another 10K resistor between the output and the inverting pin and the non-inverting pin is earthed, as shown in Figure 7.2c). This inverting op-amp configuration is not shown in Figure 7.2a, b due to node limitation in the demo version of PSIM 6.1. The potential divider output $V_{POT}$ is eight-ninths of the output voltage $V_O$. The reference voltage $V_{REF}$ is 9 V. The error amplifier generates $V_{ERR}$, which is ($V_{REF} - V_{POT}$). The PI controller generates the transfer function $(0.1 + (6/s))$. The triangle carrier generator generates triangle carrier signal *V_CARRIER* with a frequency of 100 kHZ. The *V_CARRIER* output and $V_{ERR}$ output are compared in an op-amp comparator. The output *V_DRIVE* is the gate pulse drive to the buck converter switch.

**TABLE 7.1**
Parameters of SMPS

| Sl.No. | Parameter | Value | Units |
|---|---|---|---|
| 1 | Normal input voltage $V_s$ | 15 | Volts |
| 2 | Normal output voltage $V_O$ | 9 | Volts |
| 3 | Variation of input voltage | 12–18 | Volts |
| 4 | Load resistance $R_L$ | 10 | Ohms |
| 5 | Inductance $L_1$ | 300E−6 | Henries |
| 6 | Filter capacitance $C_F$ | 200E−6 | Farads |
| 7 | Switching frequency $F_{sw}$ | 100 | Kilohertz |
| 8 | PI controller – $K_p, K_i$ | 0.1,6 | |

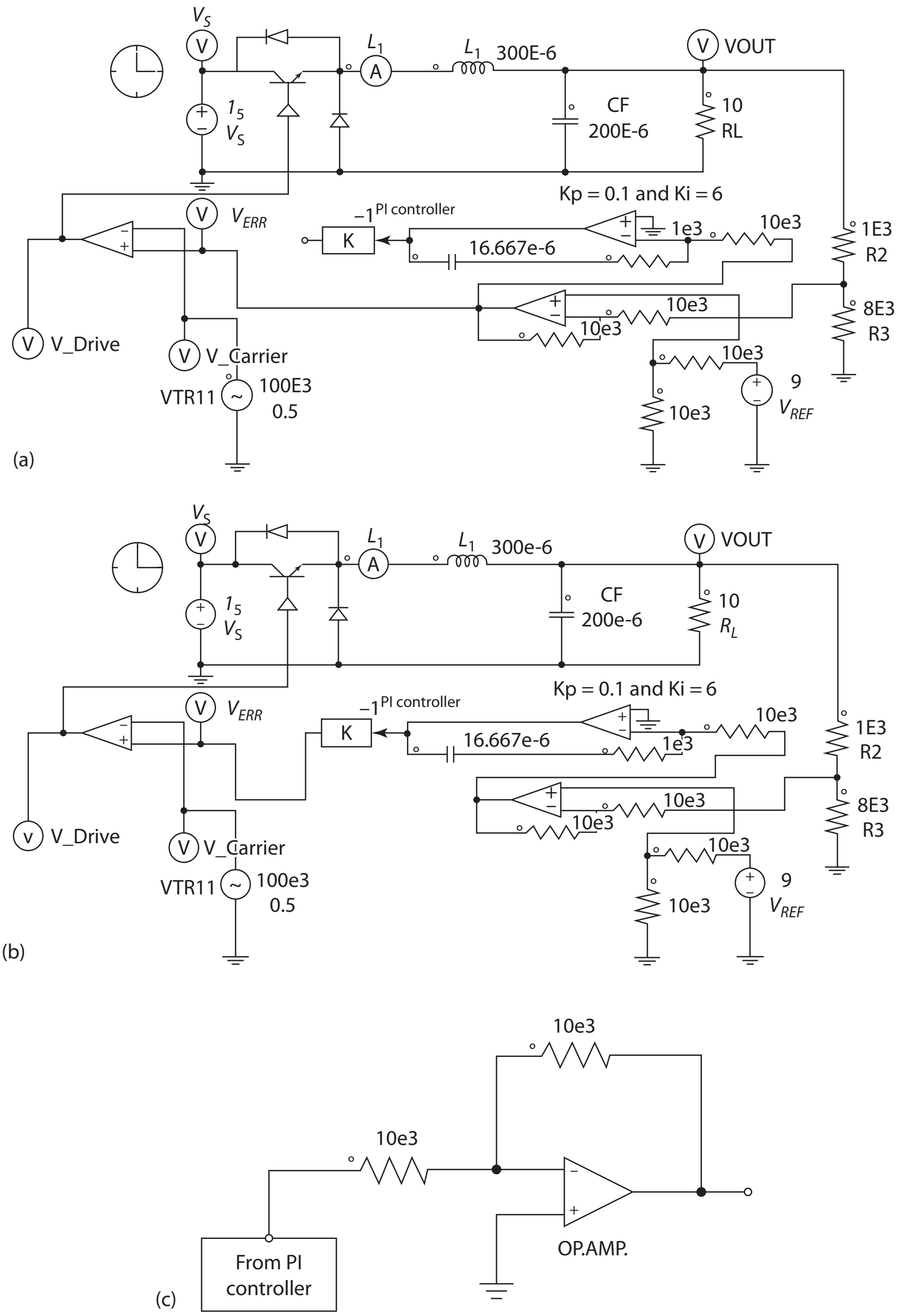

$V_S$
V
$1_5$
$V_S$
$L_1$
A
$L_1$ 300E-6
V VOUT
CF
200E-6
10
RL
Kp = 0.1 and Ki = 6
V
$V_{ERR}$
–1
PI controller
K
16.667e-6
1e3
10e3
1E3
R2
8E3
R3
10e3
10e3
10e3
10e3
9
$V_{REF}$
V V_Drive
V V_Carrier
VTR11
100E3
0.5
(a)
$V_S$
V
$1_5$
$V_S$
$L_1$
A
$L_1$ 300e-6
V VOUT
CF
200e-6
10
$R_L$
Kp = 0.1 and Ki = 6
V
$V_{ERR}$
–1
PI controller
K
16.667e-6
1e3
10e3
1E3
R2
8E3
R3
10e3
10e3
10e3
10e3
9
$V_{REF}$
v V_Drive
V V_Carrier
VTR11
100e3
0.5
(b)
10e3
10e3
OP.AMP.
From PI controller
(c)

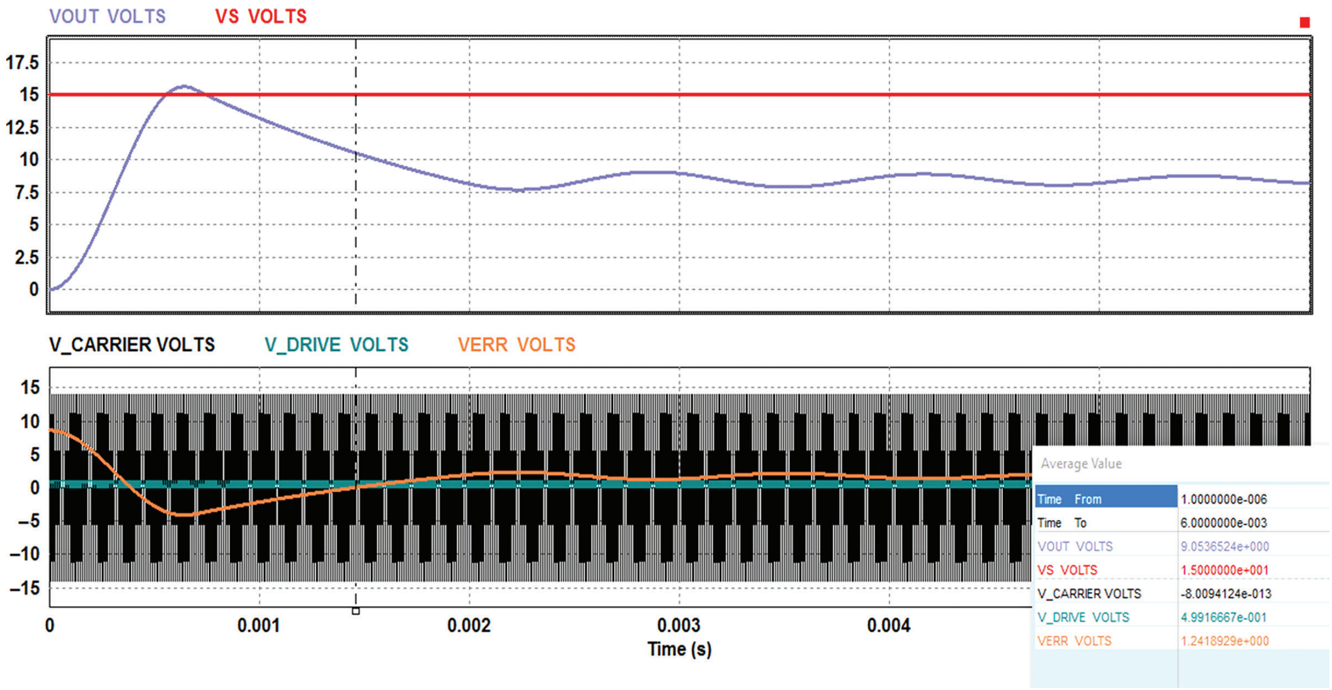
**FIGURE 7.2**
Buck converter: (a) SMPS without PI controller. (b) SMPS with PI controller. (c) Inverting operational amplifier.

The simulation of this buck converter SMPS with and without a PI controller was carried out using the demo version of PSIM 6.1. The simulation results without a PI controller and with a PI controller are shown in Figures 7.3 and 7.4, respectively.

## 7.3 Modelling of the Switched Mode Power Supply

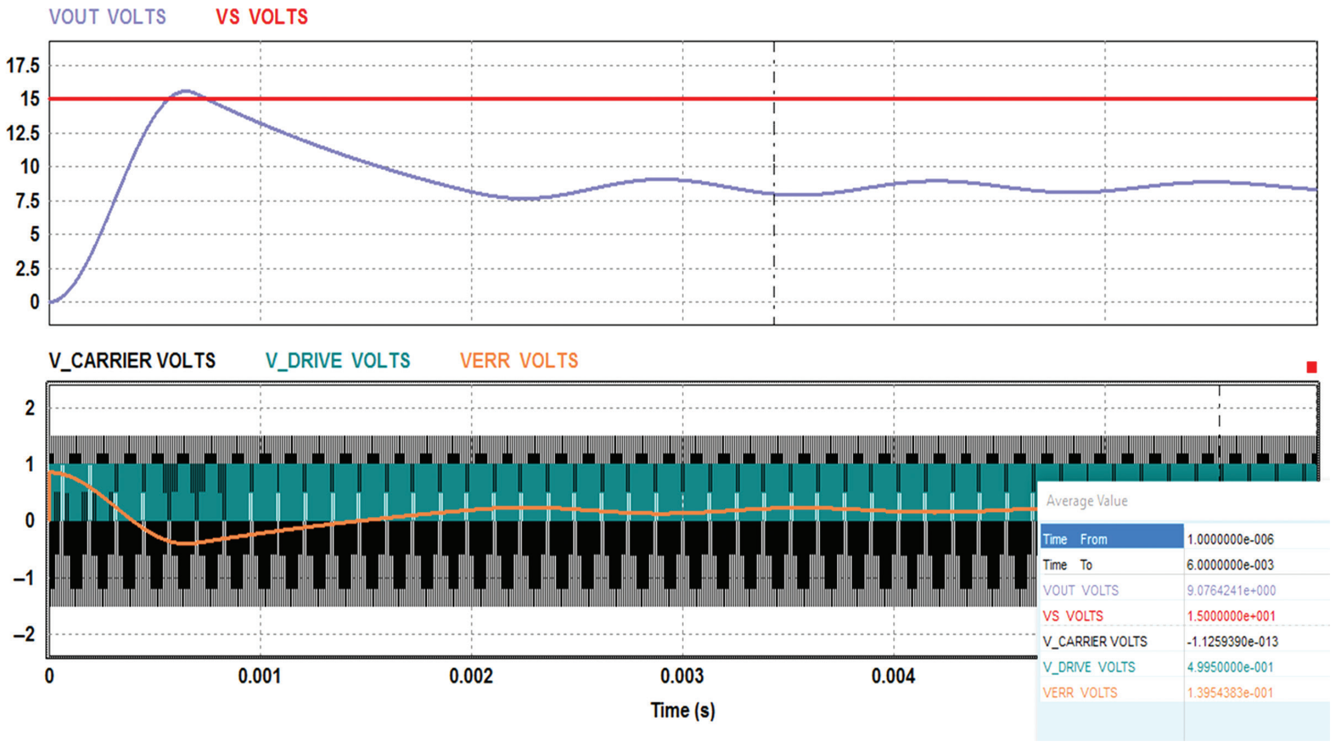
The interactive model of the SMPS is shown in Figure 7.5 [8, 9]. The various dialogue boxes and help file are shown in Figures 7.6 and 7.7. The various subsystems are shown in Figure 7.8a–d. A brief description of the various subsystems is given as follows:

Figure 7.8a, b shows the model of the buck converter used in the SMPS. This corresponds to the dialogue box 'Buck Converter Unit' shown in Figure 7.6. The parameters relating to inductance, load resistance and filter capacitance are entered in the dialogue box. The buck converter circuit is shown in Figure 5.1. The modelling of the buck converter using the switching function concept has already been discussed in Section 5.4. The same modelling Equations (5.13 through 5.16) are used to model the buck converter used in this SMPS. As this SMPS is always operated in CCM, the inductor current switch function *SF_IL*1 has a value of unity in Equation 5.16. Figure 7.8a calculates $\mathrm{d}i_{L1}/\mathrm{d}t$ using Equation 5.16 with *SF_IL*1 replaced with unity and then integrated using the Integrator block to obtain $i_{L1}$. In Figure 7.8b, this inductor current $i_{L1}$ is passed as input to a transfer function block to obtain the output voltage $V_O$. This transfer function block is the parallel combination of load resistor $R_L$ and filter capacitor $C_F$. Figure 7.8c corresponds to the dialogue box 'Error Amplifier and PI Controller Unit' in Figure 7.6. The potential divider constant, reference voltage, proportional constant *Kp* and integral constant *Ki* are entered in the appropriate places in this dialogue box. The output voltage $V_O$ is multiplied by this potential divider constant $k_{pot}$ and compared in the error detector with the reference voltage $V_{REF}$, which produces the error output voltage $V_{ERR}$. A selector switch SS1 selects $V_{ERR}$ directly or through the PI controller. This output from SS1 is passed to the comparator block in Figure 7.8d. Figure 7.8d corresponds to the dialogue box 'Triangle Carrier Generator Unit' in Figure 7.6 and the help file shown in Figure 7.7. Here, the triangle carrier pulse is generated by integration of the square pulse. The amplitude of this square pulse, the switching period of SMPS, the gain constant *k*1, and the two function constants *k*2 and *c* are entered in the appropriate places in the dialogue box. In Figure 7.8d, the Fcn2 block subtracts the amplitude $V_{max}$ of the square pulse from half its value there by generating a square pulse with positive and negative peaks of $+V_{max}/2$ and $-V_{max}/2$, respectively, with a switching period of the SMPS Tsw. This is multiplied by *k*1 using the Gain2 block; then, this value is subtracted from a constant



| | |
|---|---|
| Time From | 1.0000000e-006 |
| Time To | 6.0000000e-003 |
| VOUT VOLTS | 9.0536524e+000 |
| VS VOLTS | 1.5000000e+001 |
| V_CARRIER VOLTS | -8.0094124e-013 |
| V_DRIVE VOLTS | 4.9916667e-001 |
| VERR VOLTS | 1.2418929e+000 |

**FIGURE 7.3**
Buck SMPS: simulation results without PI controller.



| | |
|---|---|
| Time From | 1.0000000e-006 |
| Time To | 6.0000000e-003 |
| VOUT VOLTS | 9.0764241e+000 |
| VS VOLTS | 1.5000000e+001 |
| V_CARRIER VOLTS | -1.1259390e-013 |
| V_DRIVE VOLTS | 4.9950000e-001 |
| VERR VOLTS | 1.3954383e-001 |

**FIGURE 7.4**
Buck SMPS: simulation results with PI controller.

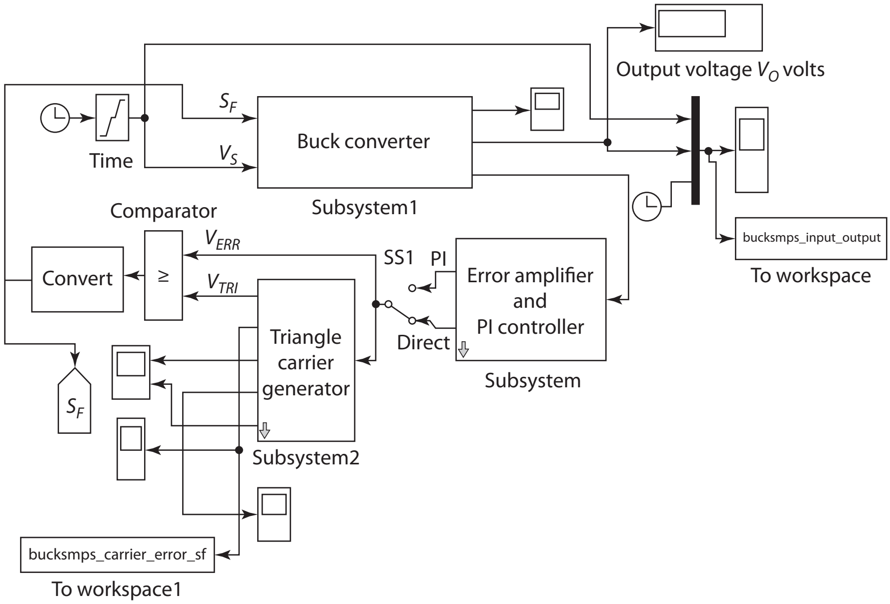
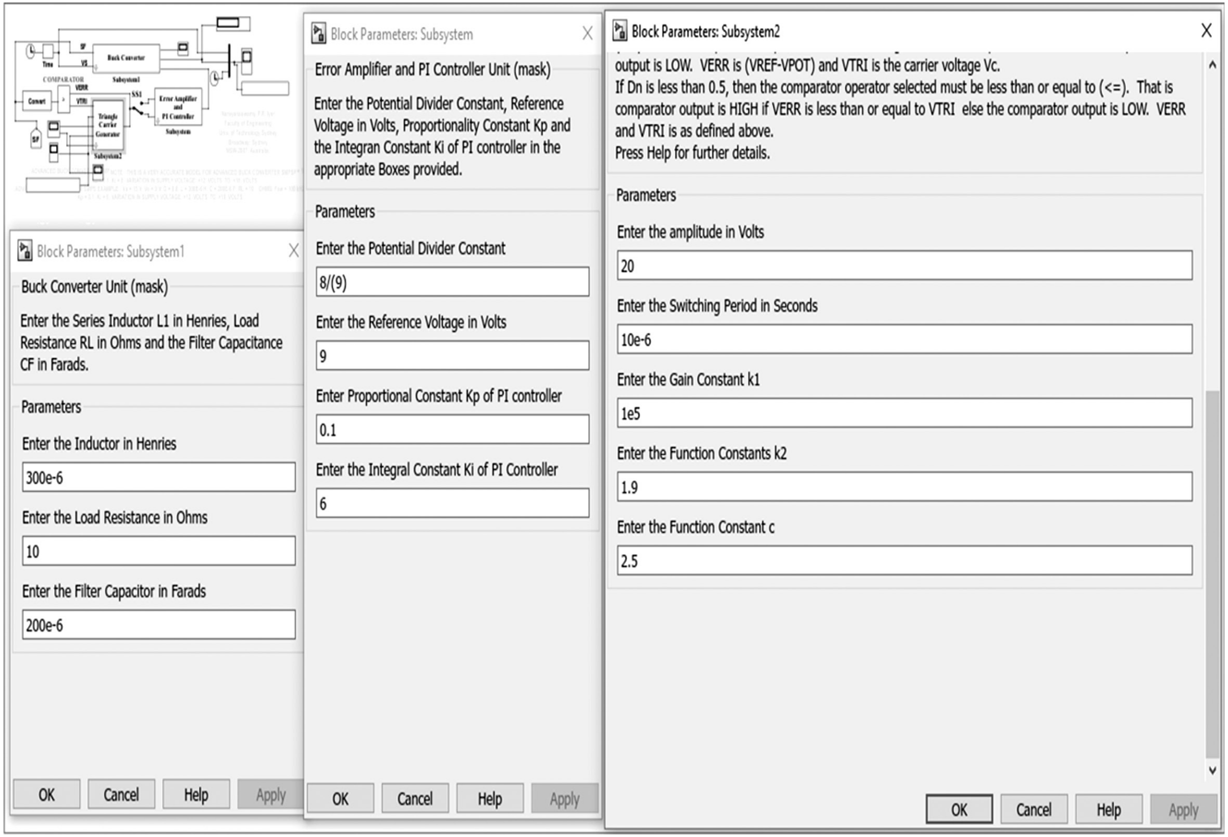

Output voltage $V_O$ volts
$S_F$
$V_S$
Time
Buck converter
Subsystem1
Comparator
$V_{ERR}$
$V_{TRI}$
Convert
≥
SS1
PI
Error amplifier and PI controller
Direct
Subsystem
Triangle carrier generator
Subsystem2
$S_F$
bucksmps_input_output
To workspace
bucksmps_carrier_error_sf
To workspace1

**FIGURE 7.5**
Buck converter SMPS.

*c* and the result is multiplied by another constant *k*2 using the Fcn3 block to obtain the triangle carrier wave with the switching period of the SMPS. The dialogue box 'Triangle Carrier Generator Unit' in Figure 7.7 provides the method to find constants *k*1, *k*2 and *c* and the peak value of the triangle carrier wave for any carrier switching frequency of the SMPS. The triangle carrier output $V_{TRI}$ and the error output $V_{ERR}$ either directly or through the PI controller are compared in the relational operator block, which is the comparator unit. The convert block converts the logical or Boolean output of the comparator to unsigned integer output. The comparator and convert blocks are shown in Figure 7.5. The selection of the relational operator for the comparator is also explained in Figure 7.7. The output of the comparator is the switch function *SF*, which drives the gate of the buck converter switch.

### 7.3.1 Simulation Results

Simulation of the buck converter SMPS was conducted with and without a PI controller using the ode23t(mod. stiff/trapezoidal) solver [10]. The parameters of the SMPS are as shown in Table 7.1. A time-varying input DC voltage source using a look-up table was used in both cases. The simulation results of the input voltage, output voltage, triangular carrier, error voltage output $V_{ERR}$, switch function *SF* and the inductor current *IL* without the PI controller are shown in Figure 7.9a–f. The same results with the PI controller are shown in Figure 7.10a–f, respectively.


Time
SF
VS
Buck Converter
Subsystem1
COMPARATOR
VERR
VTRI
Convert
SS1
Triangle Carrier Generator
Subsystem2
Error Amplifier and PI Controller
Subsystem
Block Parameters: Subsystem1
X
OK
Cancel
Help
Apply
Block Parameters: Subsystem
X
OK
Cancel
Help
Apply
Block Parameters: Subsystem2
X
OK
Cancel
Help
Apply

Buck Converter Unit (mask)

Enter the Series Inductor L1 in Henries, Load Resistance RL in Ohms and the Filter Capacitance CF in Farads.

Parameters

Enter the Inductor in Henries: 300e-6

Enter the Load Resistance in Ohms: 10

Enter the Filter Capacitor in Farads: 200e-6

Error Amplifier and PI Controller Unit (mask)

Enter the Potential Divider Constant, Reference Voltage in Volts, Proportionality Constant Kp and the Integran Constant Ki of PI controller in the appropriate Boxes provided.

Parameters

Enter the Potential Divider Constant: 8/(9)

Enter the Reference Voltage in Volts: 9

Enter Proportional Constant Kp of PI controller: 0.1

Enter the Integral Constant Ki of PI Controller: 6

output is LOW. VERR is (VREF-VPOT) and VTRI is the carrier voltage Vc.
If Dn is less than 0.5, then the comparator operator selected must be less than or equal to (<=). That is comparator output is HIGH if VERR is less than or equal to VTRI else the comparator output is LOW. VERR and VTRI is as defined above.
Press Help for further details.

Parameters

Enter the amplitude in Volts: 20

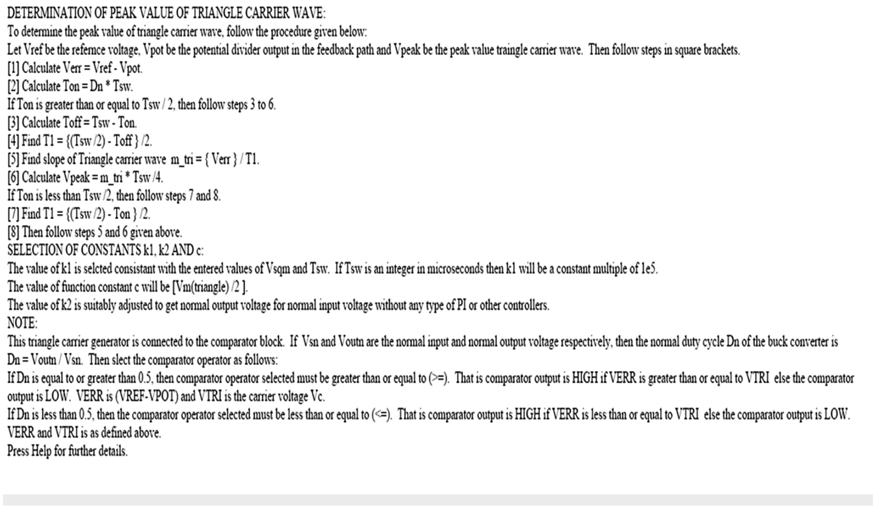
Enter the Switching Period in Seconds: 10e-6

Enter the Gain Constant k1: 1e5

Enter the Function Constants k2: 1.9

Enter the Function Constant c: 2.5

**FIGURE 7.6**
Buck converter SMPS with interactive blocks.



DETERMINATION OF PEAK VALUE OF TRIANGLE CARRIER WAVE:
To determine the peak value of triangle carrier wave, follow the procedure given below:
Let Vref be the refernce voltage, Vpot be the potential divider output in the feedback path and Vpeak be the peak value traingle carrier wave. Then follow steps in square brackets.
[1] Calculate Verr = Vref - Vpot.
[2] Calculate Ton = Dn * Tsw.
If Ton is greater than or equal to Tsw / 2, then follow steps 3 to 6.
[3] Calculate Toff = Tsw - Ton.
[4] Find T1 = {(Tsw /2) - Toff } /2.
[5] Find slope of Triangle carrier wave m_tri = { Verr } / T1.
[6] Calculate Vpeak = m_tri * Tsw /4.
If Ton is less than Tsw /2, then follow steps 7 and 8.
[7] Find T1 = {(Tsw /2) - Ton } /2.
[8] Then follow steps 5 and 6 given above.
SELECTION OF CONSTANTS k1, k2 AND c:
The value of k1 is selcted consistant with the entered values of Vsqm and Tsw. If Tsw is an integer in microseconds then k1 will be a constant multiple of 1e5.
The value of function constant c will be [Vm(triangle) /2 ].
The value of k2 is suitably adjusted to get normal output voltage for normal input voltage without any type of PI or other controllers.
NOTE:
This triangle carrier generator is connected to the comparator block. If Vsn and Voutn are the normal input and normal output voltage respectively, then the normal duty cycle Dn of the buck converter is Dn = Voutn / Vsn. Then slect the comparator operator as follows:
If Dn is equal to or greater than 0.5, then comparator operator selected must be greater than or equal to (>=). That is comparator output is HIGH if VERR is greater than or equal to VTRI else the comparator output is LOW. VERR is (VREF-VPOT) and VTRI is the carrier voltage Vc.
If Dn is less than 0.5, then the comparator operator selected must be less than or equal to (<=). That is comparator output is HIGH if VERR is less than or equal to VTRI else the comparator output is LOW.
VERR and VTRI is as defined above.
Press Help for further details.

**FIGURE 7.7**
Buck SMPS: triangle carrier generator unit.

## 7.4 Conclusions

Examination of the simulation results of the buck SMPS model in Figure 7.9a–f and in Figure 7.10a–f indicates the following points:

- Without the PI controller, the number of initial switching cycles is as high as 11 for the first 0.01 s.
- With the PI controller, the number of initial switching cycles is reduced from 11 to 7 for the first 0.01 s.
- The peak-to-peak voltage output during the initial or first switching cycle is reduced by around 2.4 V with the PI controller as compared with without the PI controller.
- The duty cycle of *SF* adjusts to a suitable value to maintain the output voltage $V_O$ close to 9 V.
- The change in output voltage for a given change in input voltage or regulation of the SMPS is greater with the PI controller as compared with without the PI controller.
- The normal output voltage is close to 9 V for a normal input voltage of 15 V in both cases.
- The triangle carrier peak with the PI controller is less than that without the PI controller to achieve the same DC output voltage of 9 V with a DC input voltage of 15 V in both cases.

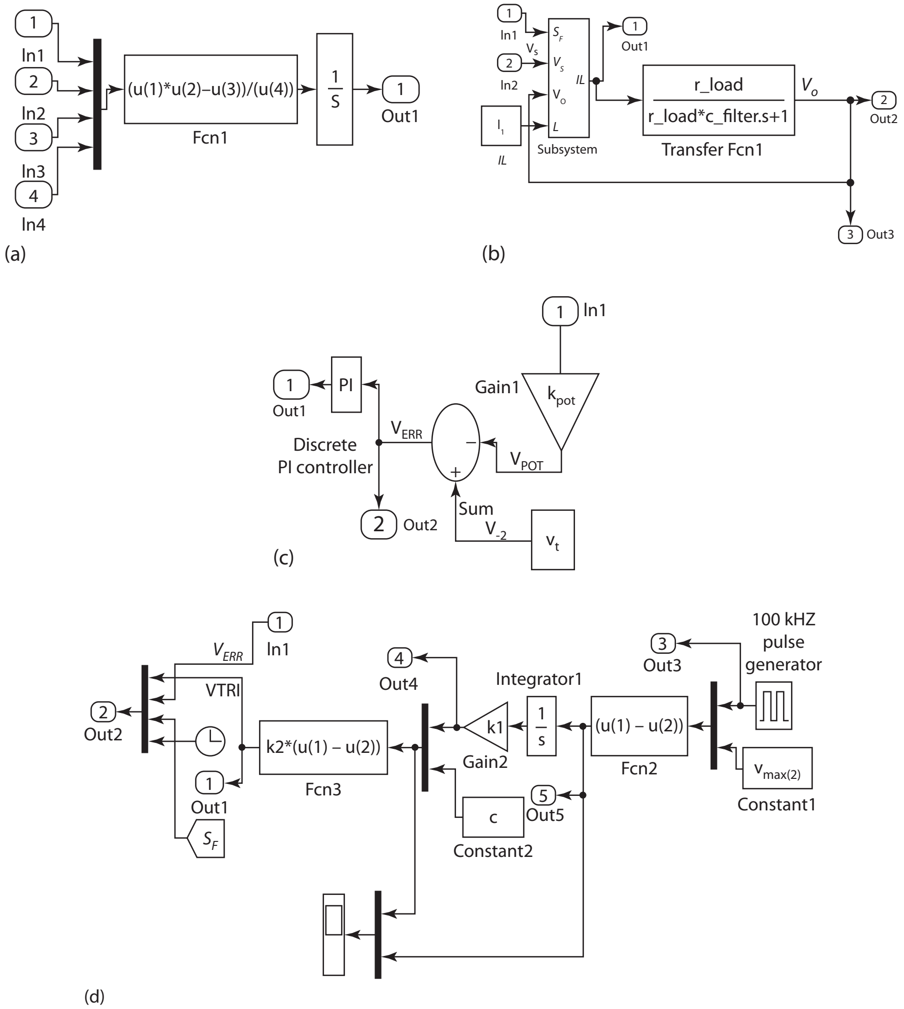

1
In1
2
In2
3
In3
4
In4
(u(1)*u(2)–u(3))/(u(4))
Fcn1
1/S
1
Out1
(a)
1
In1
Vs
2
In2
SF
VS
VO
L
IL
Subsystem
I1
IL
1
Out1
r_load
r_load*c_filter.s+1
Transfer Fcn1
Vo
2
Out2
3
Out3
(b)
1
In1
Gain1
kpot
VPOT
Sum
VERR
V-2
vt
PI
1
Out1
Discrete PI controller
2
Out2
(c)
1
In1
VERR
VTRI
2
Out2
1
Out1
SF
k2*(u(1) – u(2))
Fcn3
4
Out4
k1
Gain2
c
Constant2
Integrator1
1/s
5
Out5
(u(1) – u(2))
Fcn2
3
Out3
100 kHZ pulse generator
vmax(2)
Constant1
(d)

**FIGURE 7.8**
(a–d) Buck converter SMPS model subsystems.

- The inductor current is continuous and the buck converter operates in CCM in both cases.
- Depending on the chosen values of the parameters for the buck converter, the number of oscillation cycles and their peak values will change in both cases.

To conclude, the buck SMPS with PI controller reduces the number and peak-to-peak value of oscillation cycles in the output voltage as compared with the one without PI controller. However, the problem of the buck SMPS with PI controller is that the change in output voltage for a given change in

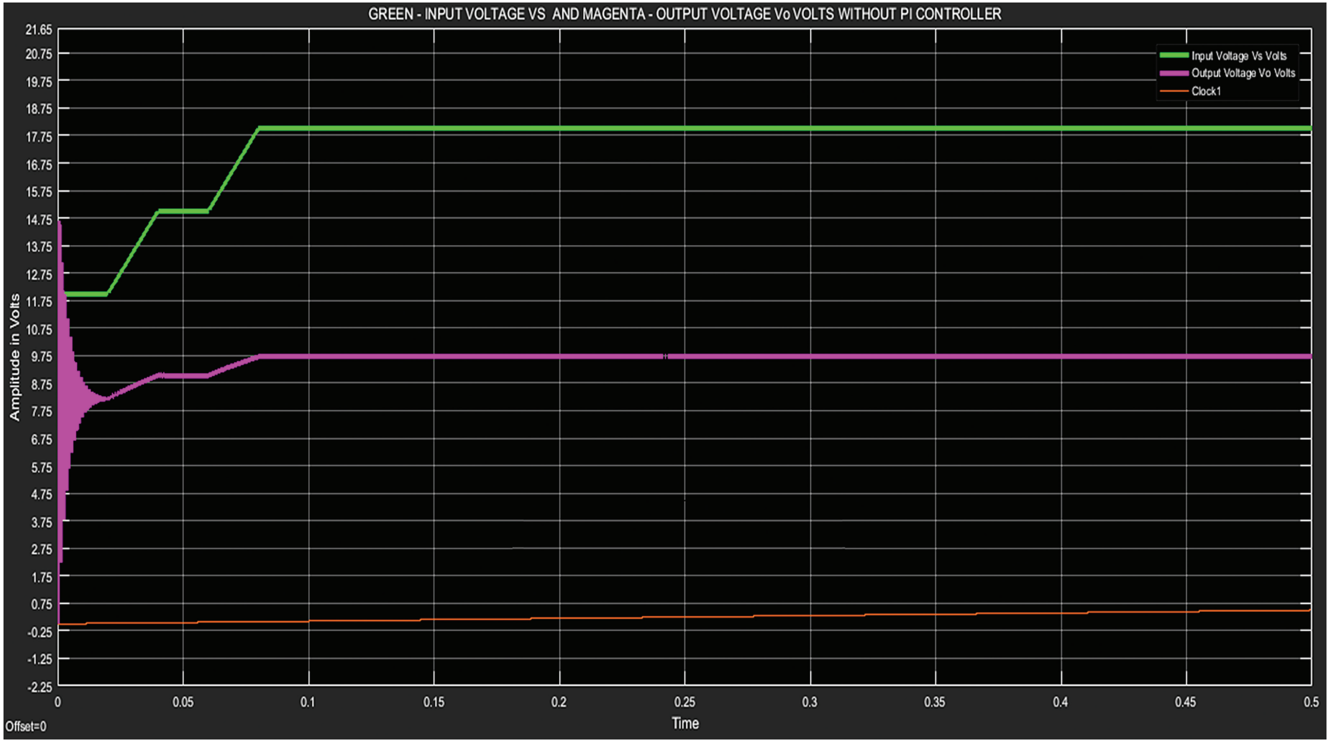


**FIGURE 7.9**
(a, b) Input voltage (green) vs. output voltage (magenta) without pi controller.

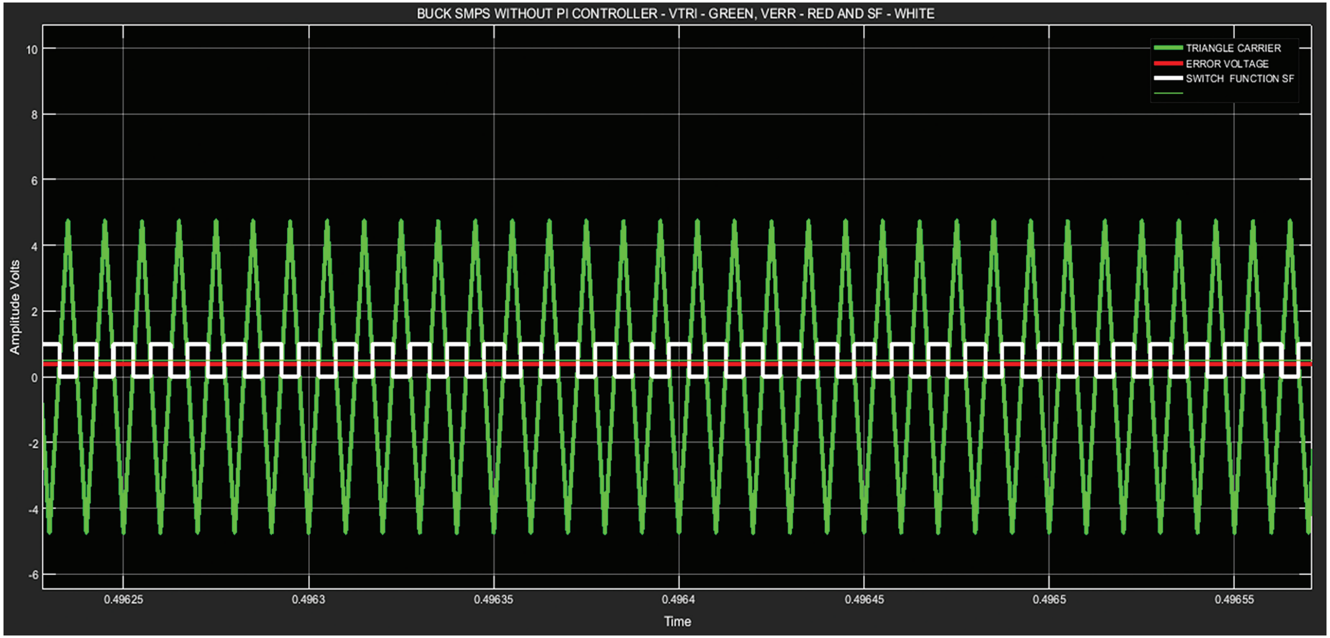


**FIGURE 7.9**
(c–e) Buck SMPS without pi controller. VTRI (green), VERR (red) and SF (white).

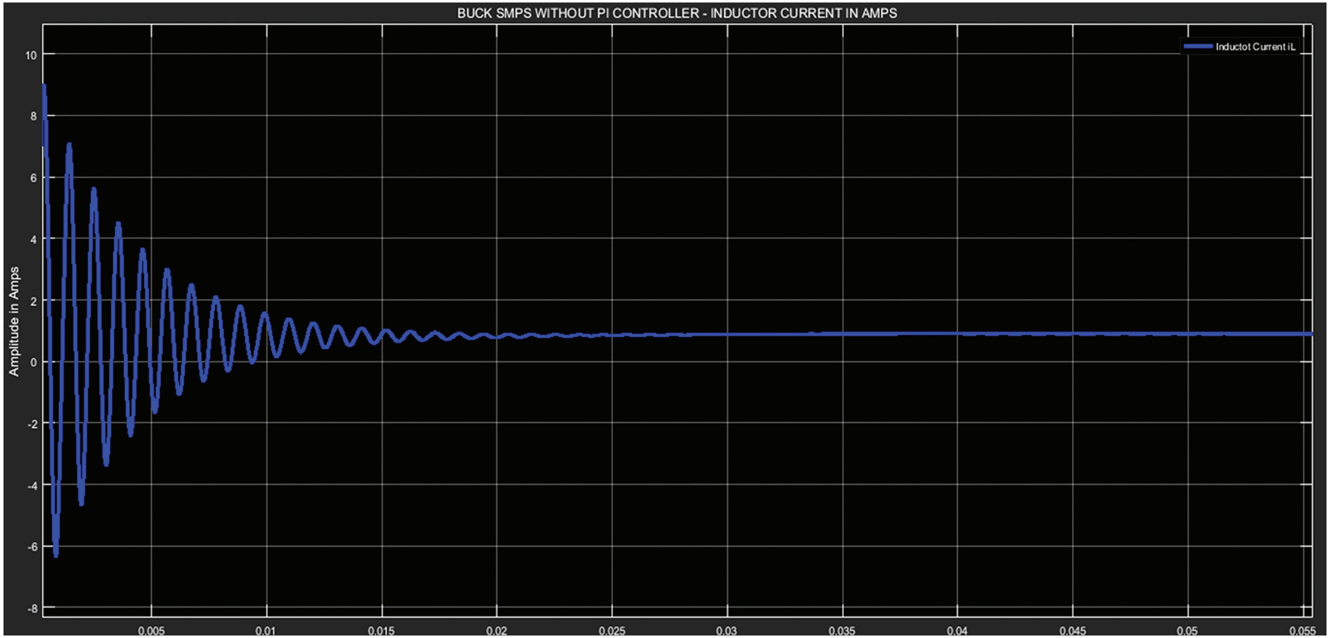


**FIGURE 7.9**
(f) Buck SMPS without pi controller: inductor current in amps.

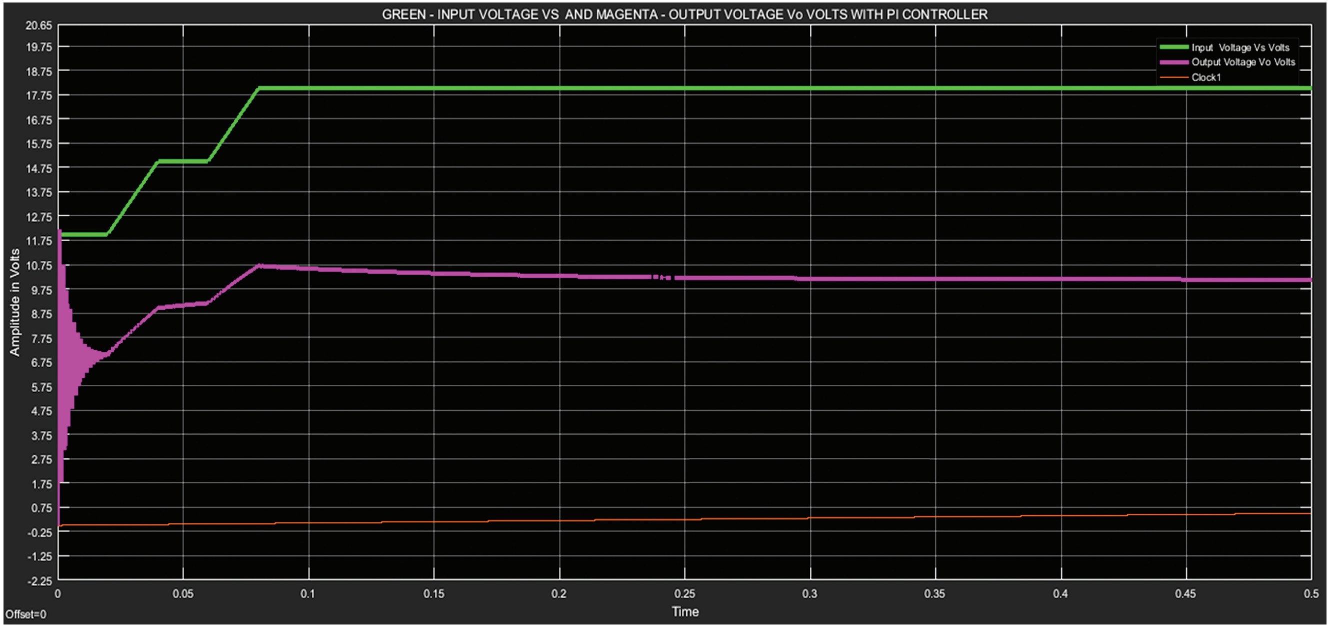


**FIGURE 7.10**
(a, b) Input voltage (green) vs. output voltage (magenta) with pi controller.

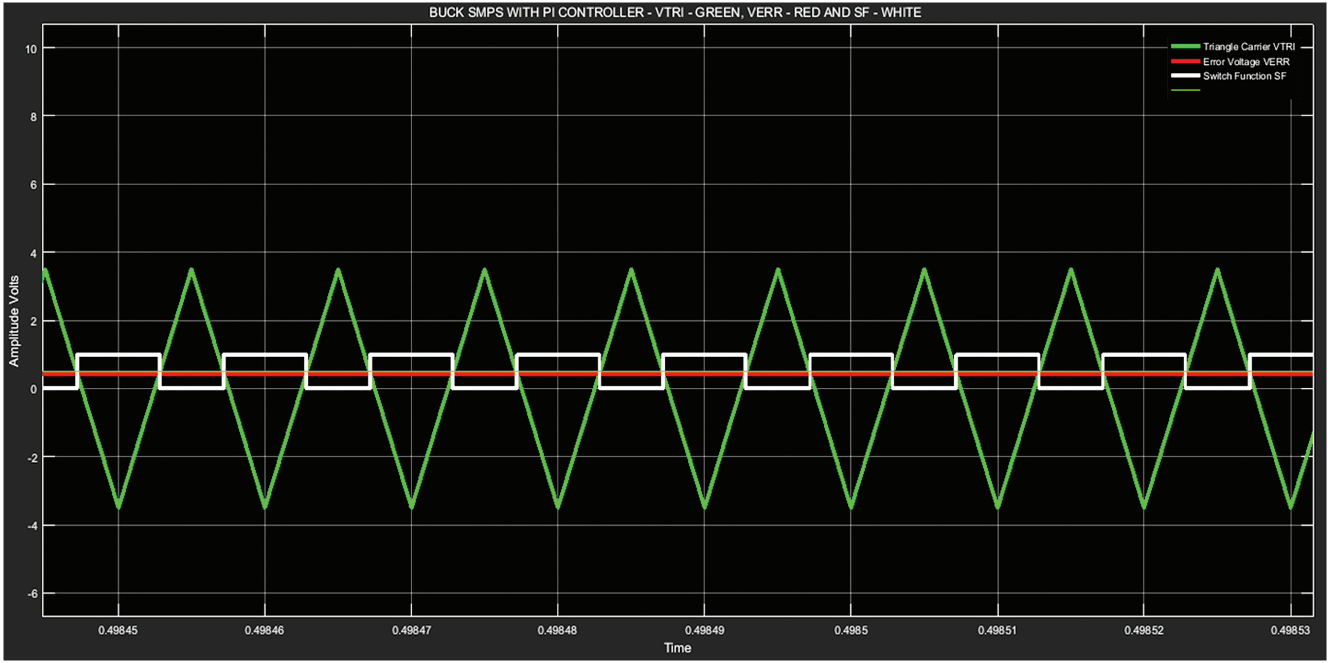


**FIGURE 7.10**
(c–e) Buck SMPS with pi controller. VTRI (green), VERR (red) and SF (white).

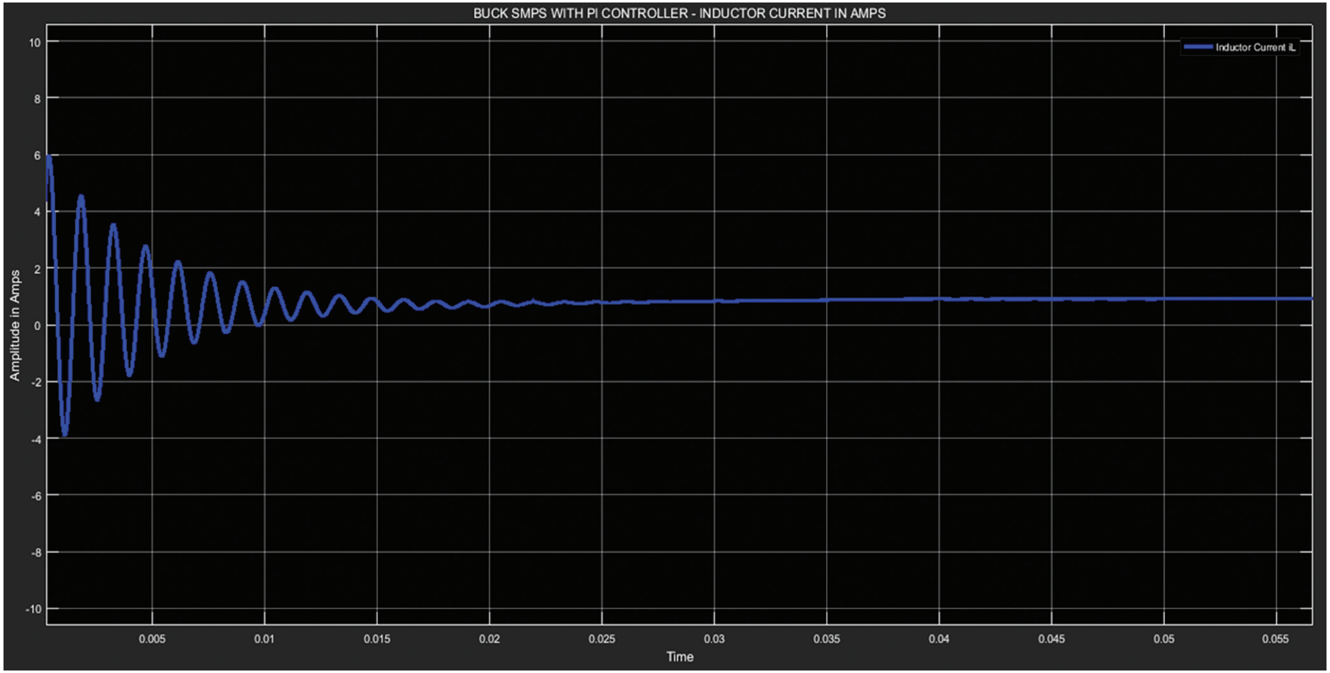


**FIGURE 7.10**
(f) Buck SMPS with pi controller: inductor current in amps.

input voltage is much larger compared with the one without PI controller. Referring to Figure 7.9a,b, it is seen that for the buck SMPS without PI controller, when the input voltage changes from 12 to 18 V, the steady-state output voltage changes from 8.25 to 9.75 V. From Figure 7.10a,b, it is seen that for the buck SMPS with PI controller, this steady-state output voltage variation is 7–10.25 V for the same change in input voltage.

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9. N.P.R. Iyer: "MATLAB/SIMULINK modules for modelling and simulation of power electronic converters and electric drives", M.E. by research thesis, University of Technology Sydney, NSW, Australia, 2006, Chapter 10.
10. The Mathworks Inc.: "MATLAB/Simulink Release Notes", R2016b, 2016.

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# 8

# Interactive Models for Fourth-Order DC to DC Converters

## 8.1 Introduction

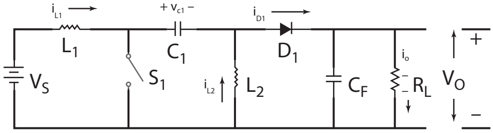
As already mentioned in Chapter 5, fourth-order DC to DC converters have two inductors, one energy transfer capacitor, one filter capacitor, one or more diodes and a load resistor, along with the semiconductor switch, gate drive and DC voltage source. These converters can be operated in the buck or boost mode by proper choice of duty cycle for the gate pulse drive. Interactive system models for selected fourth-order DC to DC converters such as the single-ended primary inductance converter (SEPIC), quadratic boost and ultra-lift Luo converters are presented in this chapter for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

## 8.2 Analysis of SEPIC Converter in CCM

The SEPIC converter is used to obtain a positive output voltage less than, equal to or greater than the input DC voltage. The circuit schematic of the SEPIC converter is shown in Figure 8.1 [1–5].

The switch is driven by a gate pulse whose period is $T$ and duty cycle $D$. When the switch $S_1$ is ON for the interval $0 \le t \le D.T$ s, the diode $D_1$ is reverse biased and is open. When switch $S_1$ is OFF for the interval $D.T \le t \le T$ s, the diode $D_1$ is forward biased and provides a short circuit path. This is shown in Figure 8.2a, b. The average inductor current of $L_1$ and $L_2$ over one switching cycle is zero. This can be expressed as follows:

$$\frac{V_S.D.T}{L_1}+\frac{(V_S-V_{C1}-V_O).(1-D).T}{L_1}=0 \tag{8.1}$$



$i_{L1}$
$+ v_{c1} -$
$i_{D1}$
$L_1$
$C_1$
$D_1$
$V_S$
$S_1$
$i_{L2}$
$L_2$
$C_F$
$i_o$
$R_L$
$V_O$
+
–

**FIGURE 8.1**
SEPIC converter.

$$\frac{(-V_{C1}).D.T}{L_2}+\frac{(V_O).(1-D).T}{L_2}=0 \tag{8.2}$$

From Equation 8.2, $V_{C1}$ can be expressed as follows:

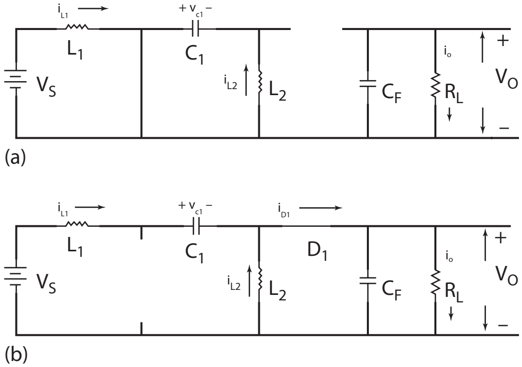
$$V_{C1}=\frac{V_O.(1-D)}{D} \tag{8.3}$$

Using Equation 8.3 in Equation 8.1 and simplifying gives the following result:

$$\frac{V_O}{V_S}=\frac{D}{(1-D)} \tag{8.4}$$

The polarity of $V_O$ is positive at the top and negative at the bottom terminal, as shown in Figure 8.1. The relevant waveforms for the SEPIC converter CCM operation are shown in Figure 8.3. Neglecting switching losses, the input power and output power are equal. This can be expressed as follows:

$$V_S * I_{L1}=\frac{V_O^2}{R_L} \tag{8.5}$$



$i_{L1}$
$+ v_{c1} -$
$L_1$
$C_1$
$V_S$
$i_{L2}$
$L_2$
$C_F$
$i_o$
$R_L$
$V_O$
+
–
(a)
$i_{L1}$
$+ v_{c1} -$
$i_{D1}$
$L_1$
$C_1$
$D_1$
$V_S$
$i_{L2}$
$L_2$
$C_F$
$i_o$
$R_L$
$V_O$
+
–
(b)

**FIGURE 8.2**
SEPIC converter equivalent circuits in CCM. (a) Switch ON for $0 \le t \le D.T$ s. (b) Switch OFF for $D.T \le t \le T$ s.

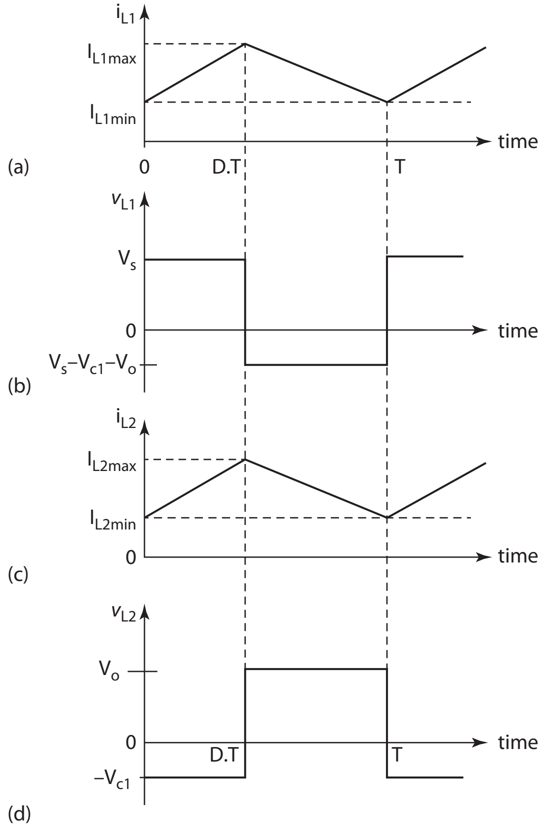


**FIGURE 8.3**
SEPIC converter waveforms in CCM. (a) Inductor $L_1$ current $i_{L1}$. (b) Inductor $L_1$ voltage $vL_1$. (c) Inductor $L_2$ current $i_{L2}$. (d) Inductor $L_2$ voltage $vL_2$.

Using Equations 8.4 and 8.5, we have the following:

$$I_{L1} = \frac{V_S.D^2}{(1-D)^2.R_L} \tag{8.6}$$

The maximum and minimum inductor current for $L_1$ can be expressed as follows:

$$I_{L1\max} = \frac{V_S.D^2}{(1-D)^2.R_L} + \frac{V_S.D.T}{2L_1} \tag{8.7}$$

$$I_{L1\min} = \frac{V_S.D^2}{(1-D)^2.R_L} - \frac{V_S.D.T}{2L_1} \tag{8.8}$$

The minimum value of inductance for $L_1$, known as *critical inductance*, $L_{1\text{crit}}$, to maintain CCM is obtained by setting Equation 8.8 to zero.

$$L_{1\text{crit}} = \frac{(1-D)^2 .T.R_L}{2D} \tag{8.9}$$

Similarly, for the inductor $L_2$, the maximum and minimum values of inductor current $I_{L2\max}$ and $I_{L2\min}$ can be expressed as follows:

$$I_{L2\max} = \frac{V_O}{R_L} + \frac{V_O.(1-D).T}{2L_2} \tag{8.10}$$

$$I_{L2\min} = \frac{V_O}{R_L} - \frac{V_O.(1-D).T}{2L_2} \tag{8.11}$$

The minimum value of inductance for $L_2$, $L_{2\text{crit}}$, to maintain CCM is obtained by setting Equation 8.11 to zero.

$$L_{2\text{crit}} = \frac{(1-D).T.R_L}{2} \tag{8.12}$$

## 8.3 Analysis of SEPIC Converter in DCM

In DCM, the two inductor currents are not continuous. During the switch OFF period, the two inductor currents $i_{L1}$ and $i_{L2}$ decay and reach and maintain zero value for a brief period of time. The equivalent circuit for DCM operation is shown in Figure 8.4.

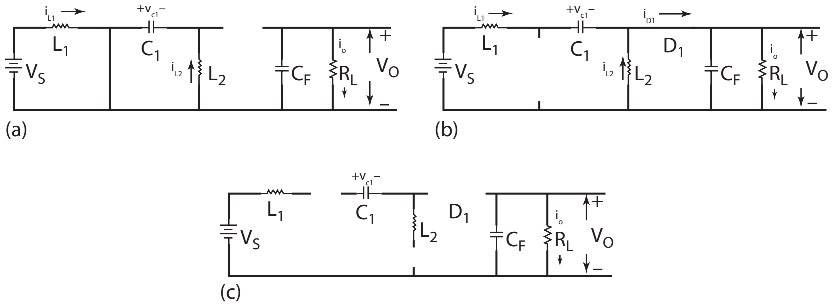


**FIGURE 8.4**
SEPIC converter equivalent circuits in DCM. (a) Switch ON for $0 \leq t \leq D.T$ s. (b) Switch OFF for $D.T \leq t \leq D_1.T$ s. (c) Inductor currents $i_{L1}$ and $i_{L2}$ are zero.

The relevant waveforms for DCM are shown in Figure 8.5 [1–5]. During the switch ON period, the two inductor currents $i_{L1}$ and $i_{L2}$ increase and reach maximum values $I_{L1\max}$ and $I_{L2\max}$ during the interval $0 \leq t \leq D.T$. When the switch is OFF, the two inductor currents decay and reach a value of zero during the interval $D.T \leq t \leq D_1.T$. From $D_1.T$ to $T$ s, the two inductor currents remain zero and the cycle repeats. The diode current $i_{D1}$ flows only during the switch OFF period from $D.T$ to $D_1.T$ s.

The average inductor current over one switching cycle is zero and, referring to Figures 8.4 and 8.5, the following equations are valid for inductor currents $i_{L1}$ and $i_{L2}$:

$$\frac{V_S.D.T}{L_1} + \frac{(V_S - V_{C1} - V_O).(D_1 - D).T}{L_1} = 0 \tag{8.13}$$

$$\frac{(-V_{C1}).D.T}{L_2} + \frac{(V_O).(D_1 - D).T}{L_2} = 0 \tag{8.14}$$

From Equation 8.14,

$$\frac{V_{C1}}{V_O} = \frac{(D_1 - D)}{D} \tag{8.15}$$

From Equations 8.13 and 8.15,

$$\frac{V_O}{V_S} = M = \frac{D}{(D_1 - D)} \tag{8.16}$$

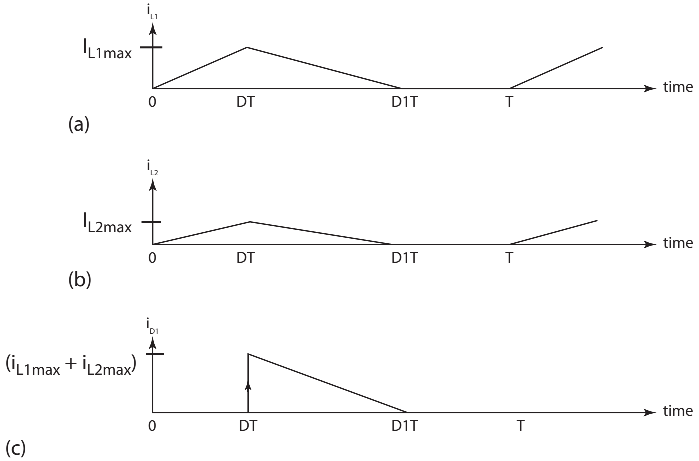


**FIGURE 8.5**
SEPIC converter waveforms in DCM. (a) Inductor $L_1$ current. (b) Inductor $L_2$ current. (c) Diode $D_1$ current.

$V_O$ has a polarity that is positive at the top and negative at the bottom terminal, as shown in Figure 8.4.

From Figure 8.4, it is seen that the load current $I_O$ is the average value of diode $D_1$ current $i_{D1}$, and $i_{D1}$ flows through the load resistance only during the switch OFF period. Referring to Figure 8.5c, $I_O$ can be expressed as follows:

$$I_O = \frac{V_O}{R_L} = \frac{1}{T}.\left[\frac{\left(I_{L1\max} - I_{L2\max}\right).\left(D_1 - D\right).T}{2}\right] \tag{8.17}$$

$$I_O = \frac{V_O}{R_L} = \left[\frac{\left(D_1 - D\right)}{2}\right] * \left(\frac{V_S.D.T}{L_1} + \frac{V_{C1}.D.T}{L_2}\right) \tag{8.18}$$

Using Equations 8.15 and 8.16 in Equation 8.18 and simplifying gives the following result:

$$V_O = \left[\frac{V_S.D.T.R_L.\left(D_1 - D\right)}{2}\right] * \left[\frac{1}{L_1} + \frac{1}{L_2}\right] \tag{8.19}$$

$$\text{Let} \quad \frac{1}{L_{eq}} = \left[\frac{1}{L_1} + \frac{1}{L_2}\right] \tag{8.20}$$

$$\text{Let} \quad K = \frac{2.L_{eq}}{T.R_L} \tag{8.21}$$

Using Equations 8.20 and 8.21 in Equation 8.19 and simplifying gives the following:

$$\frac{V_O}{V_S} = M = \frac{D.\left(D_1 - D\right)}{K} \tag{8.22}$$

Using Equations 8.16 and 8.22, the expression for $V_O/V_S$ can be written as given here:

$$\frac{V_O}{V_S} = M = \frac{D}{\sqrt{K}} \tag{8.23}$$

Also from Equation 8.16, $D_1$ can be expressed as follows:

$$D_1 = \frac{D.\left(1 + M\right)}{M} \tag{8.24}$$

## 8.4 Model of SEPIC Converter in CCM and DCM

Models for fourth-order converters are available in references [6–8]. The switching function concept is used to model the SEPIC converter [6–8]. The SEPIC converter model parameters are shown in Table 5.1. The development of the model is given as follows:

Referring to Figures 8.2 and 8.4, the following equations can be derived for CCM and DCM operation.

$$\left.\begin{aligned} i_{L1\_dot} &= \frac{(V_S)}{L_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(V_S - V_{C1} - V_O)}{L_1} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.25}$$

Now, for the switch $S_1$, the switching function SF has already been defined in Equation 5.14 for CCM operation. For the inductor current $i_{L1}$, another switch function SF_I$_{L1}$ has already been defined in Equation 5.15. For the inductor current $i_{L2}$ through $L_2$, the switch function SF_I$_{L2}$ is defined as follows:

$$\left.\begin{aligned} \text{SF\_I}_{L2} &= 1 \quad \text{for} \quad i_{L2} \succ 0 \\ &= 0 \quad \text{for} \quad i_{L2} \le 0 \end{aligned}\right| \tag{8.26}$$

$$\left.\begin{aligned} i_{L2\_dot} &= \frac{(V_{C1})}{L_2} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(-V_O)}{L_2} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.27}$$

$$\left.\begin{aligned} v_{C1\_dot} &= \frac{-I_{L2}}{C_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{I_{L1}}{C_1} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.28}$$

$$\left.\begin{aligned} v_{O\_dot} &= \frac{-V_O}{(R_L.C_F)} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{\left(I_{L1} + I_{L2} - \dfrac{V_O}{R_L}\right)}{C_F} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.29}$$

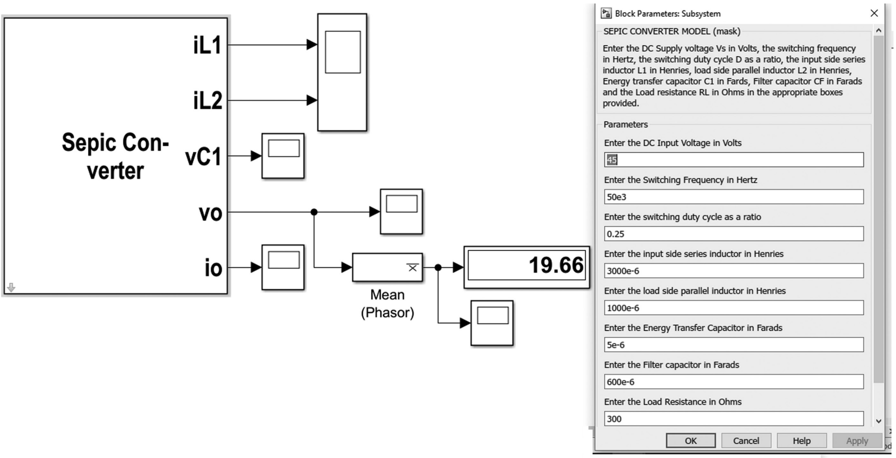
Load current $I_O$ is given by Equation 5.19. In Equations 8.25, 8.27, 8.28 and 8.29, the symbol *_dot* indicates the first derivative with respect to time of the respective variable. These equations are valid for DCM by replacing $D.T <= t <= T$ by $D.T <= t <= D_1.T$. The diode $D_1$ current $i_{D1}$ flows through the load resistor and filter capacitor during the switch OFF period in CCM and in DCM until this diode current falls to zero. This diode current $i_{D1}$ during the switch OFF period is the algebraic sum of the two inductor currents $i_{L1}$ and $i_{L2}$. The output voltage equation is formulated by observation of equivalent circuits for CCM and DCM (Figures 8.2 and 8.4), as shown in Equation 8.29.

The interactive model of the SEPIC converter suitable for CCM and DCM operation with a dialogue box is shown in Figure 8.6 and the model subsystem with a dialogue box is shown in Figure 8.7.

The data in the dialogue box in Figure 8.6 corresponds to DCM operation. For CCM operation, the relevant data are entered in the dialogue box.

The switch function SF for the switch defined in Equation 5.14 is generated using the Pulse Generator block, whose amplitude is 1, pulse width (d * 100) (% of period) and switching period $1/(f_{sw})$, where d is the duty ratio and fsw is the frequency of switching. The switch function for $L_1$ inductor current $SF\_I_{L1}$, defined in Equation 5.15, is generated using the embedded MATLAB® function whose input is $I_{L1}$ and output is $SF\_I_{L1}$, as shown in Figure 8.7.

The switch function for $L_2$ inductor current $SF\_I_{L2}$, defined in Equation 8.26, is also generated in the same embedded MATLAB function, whose input is $I_{L2}$ and output is $SF\_I_{L2}$. Equations 8.25, 8.27, 8.28 and 8.29 are solved using another embedded MATLAB function and integrators, as shown in



SEPIC CONVERTER MODEL (mask)

Enter the DC Supply voltage Vs in Volts, the switching frequency in Hertz, the switching duty cycle D as a ratio, the input side series inductor L1 in Henries, load side parallel inductor L2 in Henries, Energy transfer capacitor C1 in Fards, Filter capacitor CF in Farads and the Load resistance RL in Ohms in the appropriate boxes provided.

Parameters

Enter the DC Input Voltage in Volts
45

Enter the Switching Frequency in Hertz
50e3

Enter the switching duty cycle as a ratio
0.25

Enter the input side series inductor in Henries
3000e-6

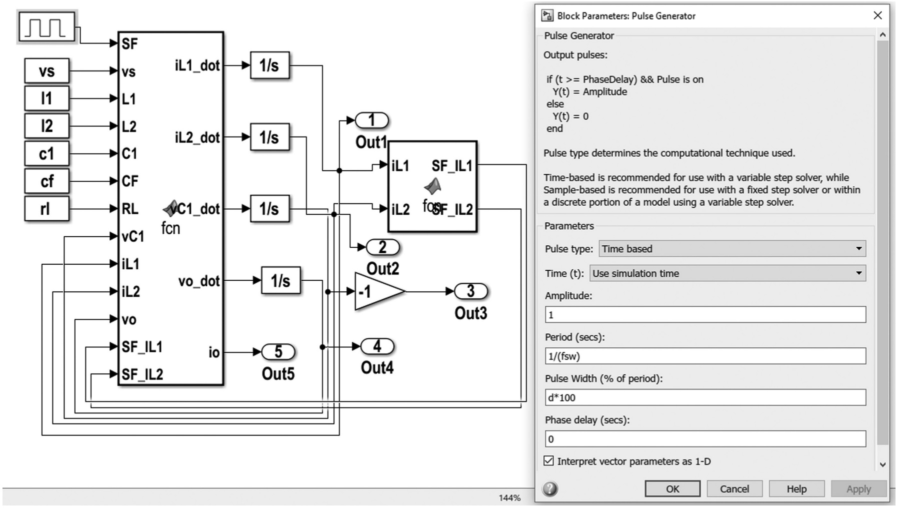
Enter the load side parallel inductor in Henries
1000e-6

Enter the Energy Transfer Capacitor in Farads
5e-6

Enter the Filter capacitor in Farads
600e-6

Enter the Load Resistance in Ohms
300

**FIGURE 8.6**
SEPIC converter.


vs
l1
l2
c1
cf
rl
SF
vs
L1
L2
C1
CF
RL
vC1
iL1
iL2
vo
SF_IL1
SF_IL2
iL1_dot
iL2_dot
vC1_dot
fcn
vo_dot
io
1/s
1/s
1/s
1/s
1 Out1
iL1
iL2
fcn
SF_IL1
SF_IL2
2 Out2
-1
3 Out3
4 Out4
5 Out5
144%

Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): 1/(fsw)

Pulse Width (% of period): d*100

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

OK
Cancel
Help
Apply

**FIGURE 8.7**
SEPIC converter model subsystem.

Figure 8.7. The source code for the two embedded MATLAB functions is given here:

```
function [iL1_dot,iL2_dot,vC1_dot,vo_dot,io] = fcn(SF,vs,L1,L2,
C1,CF,RL,vC1,iL1,iL2,vo,SF_IL1,SF_IL2)
%%SEPIC Converter
iL1_dot = SF*vs/(L1) + (1-SF)*SF_IL1*(-vC1+vs-vo)/(L1);
iL2_dot = SF*(vC1)/(L2) + (1-SF)*SF_IL2*(-vo)/(L2);
vC1_dot = -SF*SF_IL2*iL2/(C1) + (1-SF)*SF_IL1*iL1/(C1);
vo_dot = -SF*vo/(RL*CF) + (1-SF)*(SF_IL1*iL1+SF_IL2*iL2-
          vo/(RL))/(CF);
io = vo/(RL);
```

```
function [SF_IL1,SF_IL2] = fcn(iL1,iL2)
%%SEPIC Converter
if iL1 <= 0
       SF_IL1 = 0;
else
       SF_IL1 = 1;
end
if iL2 <= 0
       SF_IL2 = 0;
else
       SF_IL2 = 1;
end
```

The embedded MATLAB outputs $v_{o\_dot}$, $v_{C1\_dot}$, $i_{L1\_dot}$ and $i_{L2\_dot}$ are integrated using Integrator blocks to obtain the required outputs and are used as feedback inputs along with SF_I$_{L1}$ and SF_I$_{L2}$ to solve Equations 8.25, 8.27, 8.28 and 8.29.

### 8.4.1 Simulation Results

Simulation of the SEPIC converter for CCM and DCM operations was carried out using Simulink® [9]. The ode23t (mod. stiff/trapezoidal) solver was used. The data shown in Table 8.1 were used for simulation. The simulation results

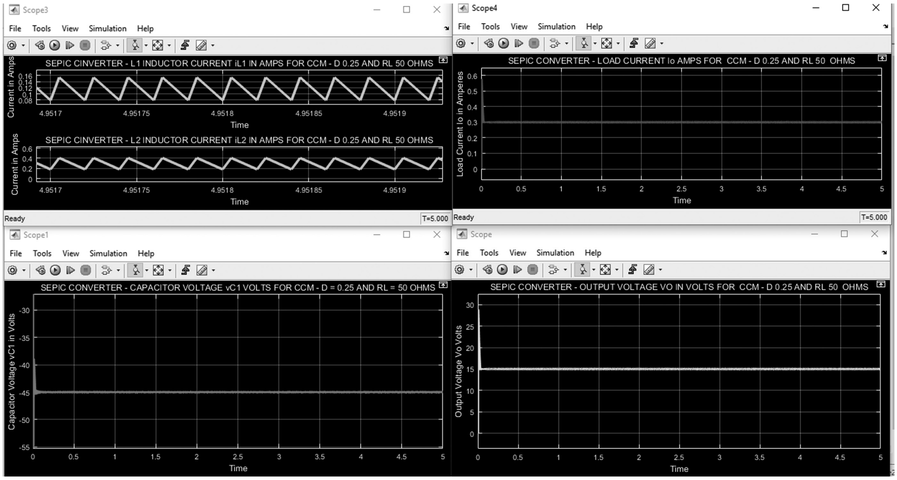

Scope3
File Tools View Simulation Help
SEPIC CINVERTER - L1 INDUCTOR CURRENT iL1 IN AMPS FOR CCM - D 0.25 AND RL 50 OHMS
Current in Amps
0.16
0.14
0.12
0.1
0.08
4.9517
4.95175
4.9518
4.95185
4.9519
Time
SEPIC CINVERTER - L2 INDUCTOR CURRENT iL2 IN AMPS FOR CCM - D 0.25 AND RL 50 OHMS
Current in Amps
0.6
0.4
0.2
0
4.9517
4.95175
4.9518
4.95185
4.9519
Time
Ready
T=5.000
Scope4
File Tools View Simulation Help
SEPIC CONVERTER - LOAD CURRENT Io AMPS FOR CCM - D 0.25 AND RL 50 OHMS
Load Current Io in Amperes
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time
Ready
T=5.000
Scope1
File Tools View Simulation Help
SEPIC CONVERTER - CAPACITOR VOLTAGE vC1 VOLTS FOR CCM - D = 0.25 AND RL = 50 OHMS
Capacitor Voltage vC1 in Volts
-30
-35
-40
-45
-50
-55
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time
Scope
File Tools View Simulation Help
SEPIC CONVERTER - OUTPUT VOLTAGE VO IN VOLTS FOR CCM - D 0.25 AND RL 50 OHMS
Output Voltage Vo Volts
30
25
20
15
10
5
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time

**FIGURE 8.8**
SEPIC converter in CCM: simulation results for $D = 0.25$.

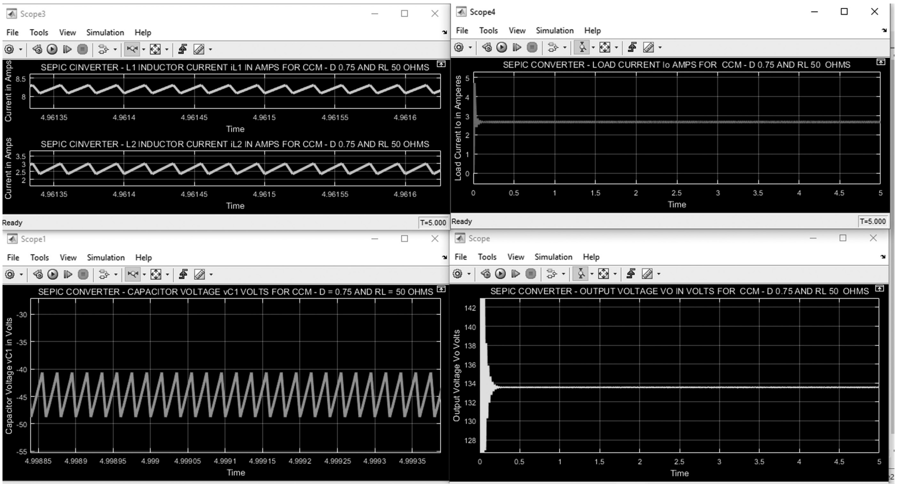

Scope3
File Tools View Simulation Help
SEPIC CINVERTER - L1 INDUCTOR CURRENT iL1 IN AMPS FOR CCM - D 0.75 AND RL 50 OHMS
Current in Amps
8.5
8
4.96135
4.9614
4.96145
4.9615
4.96155
4.9616
Time
SEPIC CINVERTER - L2 INDUCTOR CURRENT iL2 IN AMPS FOR CCM - D 0.75 AND RL 50 OHMS
Current in Amps
3.5
3
2.5
2
4.96135
4.9614
4.96145
4.9615
4.96155
4.9616
Time
Ready
T=5.000
Scope4
File Tools View Simulation Help
SEPIC CONVERTER - LOAD CURRENT Io AMPS FOR CCM - D 0.75 AND RL 50 OHMS
Load Current Io in Amperes
5
4
3
2
1
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time
Ready
T=5.000
Scope1
File Tools View Simulation Help
SEPIC CONVERTER - CAPACITOR VOLTAGE vC1 VOLTS FOR CCM - D = 0.75 AND RL = 50 OHMS
Capacitor Voltage vC1 in Volts
-30
-35
-40
-45
-50
-55
4.99885
4.9989
4.99895
4.999
4.99905
4.9991
4.99915
4.9992
4.99925
4.9993
4.99935
Time
Scope
File Tools View Simulation Help
SEPIC CONVERTER - OUTPUT VOLTAGE VO IN VOLTS FOR CCM - D 0.75 AND RL 50 OHMS
Output Voltage Vo Volts
142
140
138
136
134
132
130
128
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time

**FIGURE 8.9**
SEPIC converter in CCM: simulation results for $D = 0.75$.

**TABLE 8.1**

SEPIC Converter Model Parameters

| Sl. No. | Input Voltage $V_S$ (V) | Switching Frequency $f_{sw}$ (Hz) | Duty Cycle $D$ | Inductor $L_1$ (H) | Inductor $L_2$ (H) | Capacitor $C_1$ (F) | Filter Capacitor $C_F$ (F) | Load Resistor $R_L$ (Ω) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 45 | 50E3 | 0.25 | 3000E−6 | 1000E−6 | 5E−6 | 600E−6 | 50 | CCM |
| 2 | 45 | 50E3 | 0.75 | 3000E−6 | 1000E−6 | 5E−6 | 600E−6 | 50 | CCM |
| 3 | 45 | 50E3 | 0.25 | 3000E−6 | 1000E−6 | 5E−6 | 600E−6 | 300 | DCM |

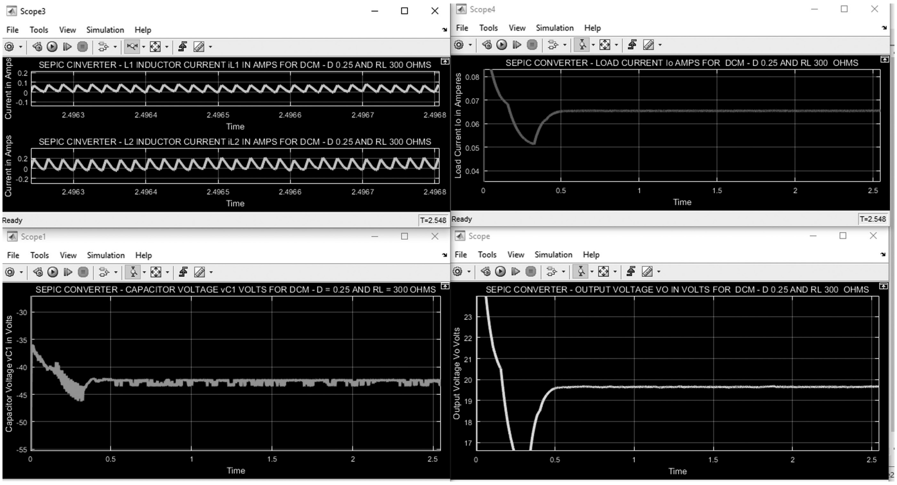

Scope3
File Tools View Simulation Help
SEPIC CINVERTER - L1 INDUCTOR CURRENT iL1 IN AMPS FOR DCM - D 0.25 AND RL 300 OHMS
Current in Amps
0.2
0.1
0
-0.1
2.4963
2.4964
2.4965
2.4966
2.4967
2.4968
Time
SEPIC CINVERTER - L2 INDUCTOR CURRENT iL2 IN AMPS FOR DCM - D 0.25 AND RL 300 OHMS
Current in Amps
0.2
0
-0.2
Ready
T=2.548
Scope4
SEPIC CONVERTER - LOAD CURRENT Io AMPS FOR DCM - D 0.25 AND RL 300 OHMS
Load Current Io in Amperes
0.08
0.07
0.06
0.05
0.04
0
0.5
1
1.5
2
2.5
Time
Scope1
SEPIC CONVERTER - CAPACITOR VOLTAGE vC1 VOLTS FOR DCM - D = 0.25 AND RL = 300 OHMS
Capacitor Voltage vC1 in Volts
-30
-35
-40
-45
-50
-55
Scope
SEPIC CONVERTER - OUTPUT VOLTAGE VO IN VOLTS FOR DCM - D 0.25 AND RL 300 OHMS
Output Voltage Vo Volts
23
22
21
20
19
18
17

**FIGURE 8.10**
SEPIC converter in DCM: simulation results.

for the SEPIC converter in CCM are shown in Figures 8.8 and 8.9 and those for DCM are shown in Figure 8.10.

Simulation results and calculated values are tabulated in Tables 8.2 and 8.3.

## 8.5 Analysis of Quadratic Boost Converter in the CCM

The quadratic boost converter circuit schematic is shown in Figure 8.11 [10, 11].

The switch is driven by a gate pulse whose period is $T$ and duty cycle $D$. The equivalent circuits of this converter in the range $0 <= t <= D.T$ and $D.T <= t <= T$ are shown in Figure 8.12 a, b, respectively. When $S_1$ is closed, the inductor currents find a path via $D_3$ to the short circuit caused by the switch, leaving $D_1$ and $D_2$ open. When $S_1$ is open, the inductor currents find a path through $D_1$ and $D_2$ to the load resistor. The relevant waveforms for CCM operation are shown in Figure 8.13.

Referring to Figure 8.12, noting that the average current through inductors $L_1$ and $L_2$ over one switching cycle is zero, we have the following equations:

$$\frac{V_S.D.T}{L_1}+\frac{(V_S-V_{C1}).(1-D).T}{L_1}=0 \tag{8.30}$$

$$\frac{(V_{C1}\ ).D.T}{L_2}+\frac{(V_{C1}-V_O).(1-D).T}{L_2}=0 \tag{8.31}$$

**TABLE 8.2**

SEPIC Converter: Simulation Results

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $V_{C1}$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.25 | 0.0789 | 0.154 | 0.1825 | 0.407 | −44.98 | 15.040 | 0.3007 | CCM |
| 2 | 0.75 | 8.085 | 8.31 | 2.345 | 3.013 | −44.85 | 133.9 | 2.678 | CCM |
| 3 | 0.25 | −0.0059 | 0.083 | −0.0497 | 0.212 | −42.44 | 19.76 | 0.0658 | DCM |

**TABLE 8.3**

SEPIC Converter: Calculated Values

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $_{C1}$ Voltage $V_{C1}$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.25 | 0.0625 | 0.1375 | 0.1875 | 0.4125 | –45 | 15 | 0.3 | CCM |
| 2 | 0.75 | 7.9875 | 8.2125 | 2.3625 | 3.0375 | –45 | 135 | 2.7 | CCM |
| 3 | 0.25 | 0 | 0.075 | –0.0375 | 0.1875 | –45 | 22.5 | 0.075 | DCM |

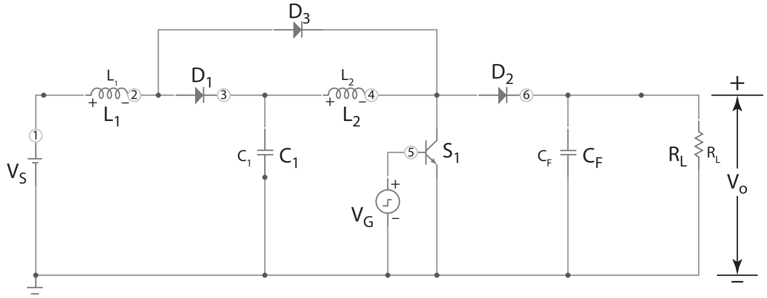

D3
L1
D1
3
L2
4
D2
6
+
1
2
L1
L2
C1
C1
5
S1
CF
CF
RL
RL
Vo
VS
VG
+
−
−

**FIGURE 8.11**
Quadratic boost converter.

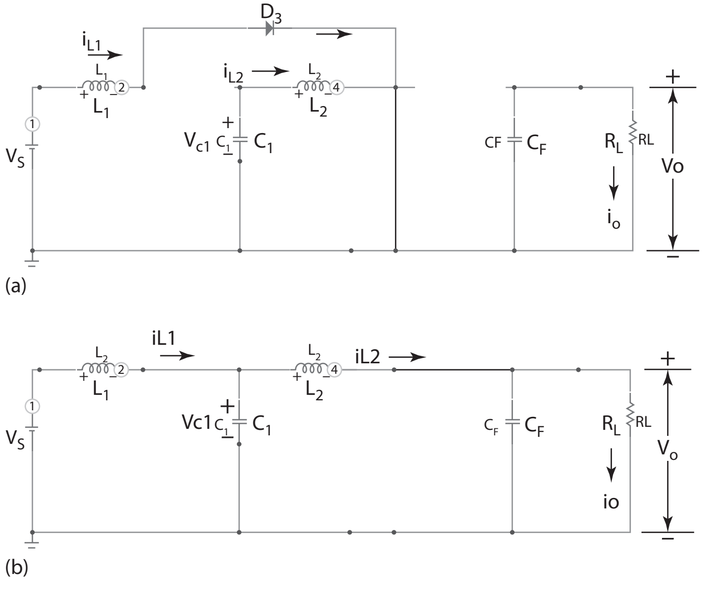

D3
iL1
L1
2
1
L1
iL2
L2
4
L2
+
Vc1
C1
C1
CF
CF
RL
RL
io
Vo
+
−
(a)
iL1
L2
2
L1
1
L2
4
iL2
L2
+
Vc1
C1
C1
CF
CF
RL
RL
io
Vo
+
−
(b)

**FIGURE 8.12**
Quadratic boost converter equivalent in CCM. (a) Switch ON for $0 \leq t \leq D.T$ s. (b) Switch OFF for $D.T \leq t \leq T$ s.

From Equation 8.31, $V_{C1}$ can be expressed as follows:

$$V_{C1} = V_O.(1-D) \tag{8.32}$$

Using Equations 8.30 and 8.32, we have the following:

$$\frac{V_O}{V_S} = M = \frac{1}{(1-D)^2} \tag{8.33}$$

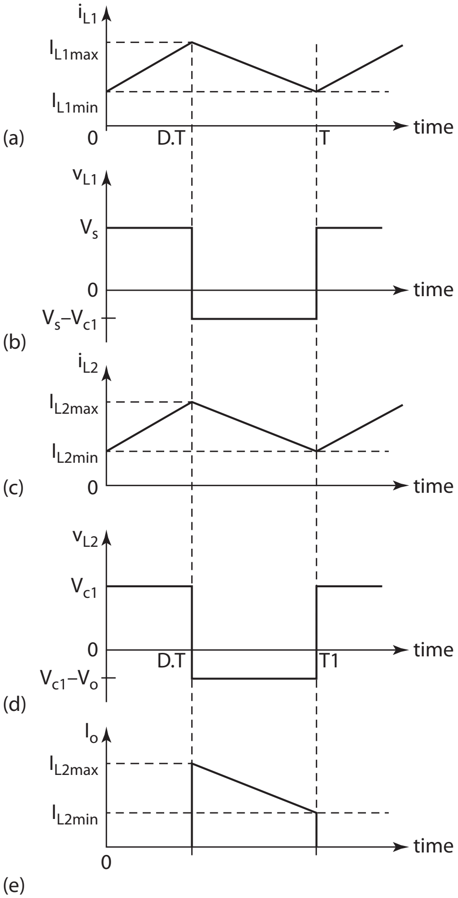


**FIGURE 8.13**

Quadratic boost converter waveforms in CCM. (a) Inductor $L_1$ current $i_{L1}$. (b) Inductor $L_1$ voltage $v_{L1}$. (c) Inductor $L_2$ current $i_{L2}$. (d) Inductor $L_2$ voltage $v_{L2}$. (e) Load current $I_O$.

Neglecting switching losses, the input power and output power are equal. This can be expressed as follows:

$$V_S * I_{L1} = V_O . I_O = \frac{V_O^2}{R_L} \tag{8.34}$$

Using Equations 8.33 and 8.34, we have the following:

$$I_{L1} = \frac{V_S}{(1-D)^4 . R_L} \tag{8.35}$$

The maximum and minimum inductor current for $L_1$ can be expressed as follows:

$$I_{L1\max} = \frac{V_S}{(1-D)^4 .R_L} + \frac{V_S.D.T}{2L_1} \tag{8.36}$$

$$I_{L1\min} = \frac{V_S}{(1-D)^4 .R_L} - \frac{V_S.D.T}{2L_1} \tag{8.37}$$

The average voltage across $C_1$ is zero, which leads to the following equation:

$$\frac{I_{L2}.D.T}{C_1} + \frac{(I_{L2} - I_{L1})(1-D).T}{C_1} = 0 \tag{8.38}$$

$$I_{L2} = I_{L1}.(1-D) = \frac{V_S}{(1-D)^3 .R_L} \tag{8.39}$$

$$I_{L2\max} = \frac{V_S}{(1-D)^3 .R_L} + \frac{V_S.D.T}{2.(1-D).L_2} \tag{8.40}$$

$$I_{L2\min} = \frac{V_S}{(1-D)^3 .R_L} - \frac{V_S.D.T}{2.(1-D).L_2} \tag{8.41}$$

The critical inductances $L_{1\text{crit}}$ and $L_{2\text{crit}}$ to maintain CCM are obtained by setting Equations 8.37 and 8.41 to zero.

$$L_{1\text{crit}} = \frac{(1-D)^4 .D.T.R_L}{2} \tag{8.42}$$

$$L_{2\text{crit}} = \frac{(1-D)^2 .D.T.R_L}{2} \tag{8.43}$$

## 8.6 Analysis of Quadratic Boost Converter in the DCM

In DCM, the two inductor currents are discontinuous. During the switch OFF period, the two inductor currents $i_{L1}$ and $i_{L2}$ decay and reach and maintain zero value for a brief period of time. The equivalent circuit for DCM operation is shown in Figure 8.14. The relevant waveforms for DCM operation are shown in Figure 8.15 [10, 11]. During the switch ON period, the two inductor currents $i_{L1}$ and $i_{L2}$ increase and reach maximum values $I_{L1\max}$ and $I_{L2\max}$ during the interval $0 <= t <= D.T$. When the switch is

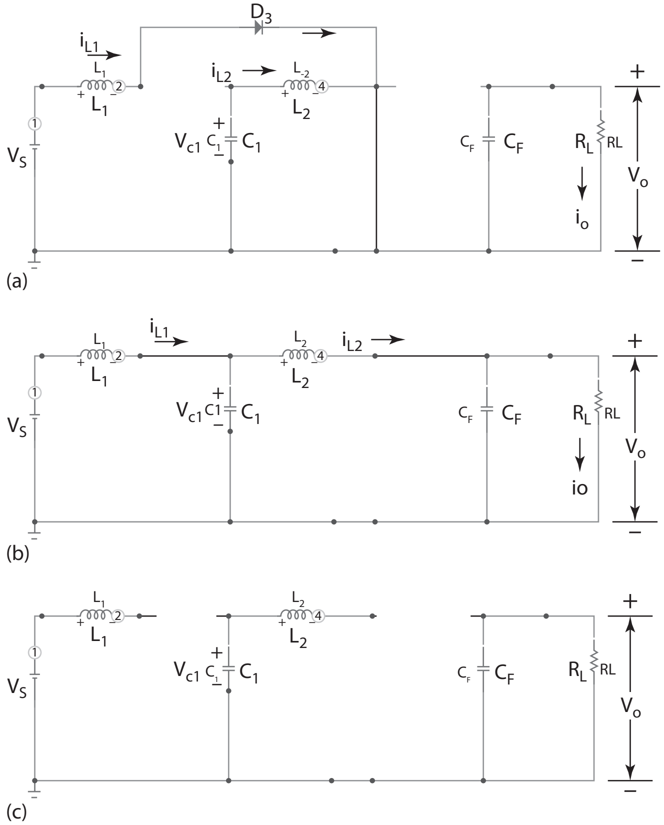

D3
iL1
L1
L1
2
iL2
L-2
4
L2
+
−
1
VS
Vc1
C1
C1
CF
CF
RL
RL
io
Vo
(a)
iL1
L1
L1
2
L2
L2
4
iL2
VS
Vc1
C1
C1
CF
CF
RL
RL
io
Vo
(b)
L1
L1
2
L2
L2
4
VS
Vc1
C1
C1
CF
CF
RL
RL
Vo
(c)

**FIGURE 8.14**
Quadratic boost converter in DCM. (a) Switch ON for 0 <= t <= D.T sec. (b) Switch OFF for D.T <=t <= D1.T sec. (c) Both inductor currents are zero.

OFF, the two inductor currents decay and reach a value of zero during the interval $D.T <= t <= D_1.T$. From $D_1.T$ to $T$ s, the two inductor currents remain zero and the cycle repeats. The $L_2$ inductor current flows through the load only while the switch is OFF from $D.T$ to $D_1.T$ s. The average inductor currents $i_{L1}$ and $i_{L2}$ over one switching cycle are zero and, referring to Figures 8.14 and 8.15, the following equations are valid for inductor currents $i_{L1}$ and $i_{L2}$:

$$\frac{V_S.D.T}{L_1}+\frac{(V_S-V_{C1}).(D_1-D).T}{L_1}=0 \tag{8.44}$$

$$\frac{(V_{C1}).D.T}{L_2}+\frac{(V_{C1}-V_O).(D_1-D).T}{L_2}=0 \tag{8.45}$$

From Equation 8.45,

$$\frac{V_{C1}}{V_O} = \frac{(D_1 - D)}{D_1} \tag{8.46}$$

From Equations 8.44 and 8.46,

$$\frac{V_O}{V_S} = M = \frac{D_1^2}{(D_1 - D)^2} \tag{8.47}$$

$V_O$ has a polarity that is positive at the top and negative at the bottom terminal, as shown in Figure 8.11. From Figure 8.14, it is seen that the load current $I_O$ is the average value of $L_2$ inductor current $i_{L2}$ and flows through the load resistance only during the switch OFF period. Referring to Figure 8.15c, $I_O$ can be expressed as follows:

$$I_O = \frac{V_O}{R_L} = \frac{1}{T}.\left[\frac{(I_{L2\max}).(D_1 - D).T}{2}\right] \tag{8.48}$$

$$I_O = \frac{V_O}{R_L} = \left[\frac{(D_1 - D)}{2}\right] * \left(\frac{V_{C1}.D.T}{L_2}\right) \tag{8.49}$$

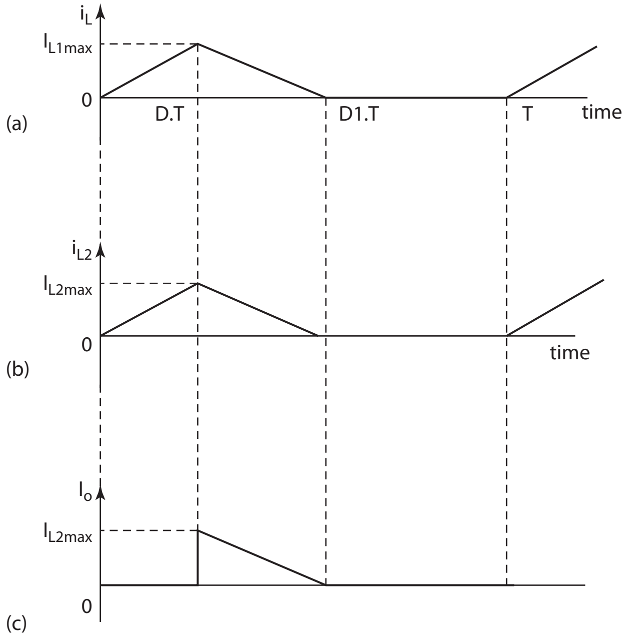


**FIGURE 8.15**
Quadratic boost converter waveforms in DCM. (a) Inductor $L_1$ current $i_{L1}$. (b) Inductor $L_2$ current $i_{L2}$. (c) Load current $I_O$.

Using Equations 8.46 and 8.47 in Equation 8.49 and simplifying gives the following result:

$$I_O = \frac{V_O}{R_L} = \left( \frac{V_S.D_1.D.T}{2.L_2} \right) \tag{8.50}$$

$$I_O * R_L = V_O = \left( \frac{V_S.D_1.D.T.R_L}{2.L_2} \right) \tag{8.51}$$

$$\text{Let} \quad K = \frac{2.L_2}{T.R_L} \tag{8.52}$$

$$\frac{V_O}{V_S} = M = \frac{D_1.D}{K} \tag{8.53}$$

$$D_1 = \frac{K.M}{D} \tag{8.54}$$

Using Equations 8.54 and 8.47 and simplifying,

$$M^2 * K^2 - M * \left[ 2 * K * D^2 + K^2 \right] + D^4 \tag{8.55}$$

Solving Equation 8.55 gives the following result:

$$M = \frac{V_O}{V_S} = \left[ \frac{\left(2 * K * D^2 + K^2\right) \pm \sqrt{\left(2 * K * D^2 + K^2\right)^2 - 4 * K^2 * D^4}}{2 * K^2} \right] \tag{8.56}$$

Equation 8.56 gives two values for *M*, of which one is acceptable.

## 8.7 Model of Quadratic Boost Converter in CCM and DCM

The switching function concept is used to model the quadratic boost converter [6–8]. Quadratic boost converter model parameters are shown in Table 8.4. The development of the model is given here:

Referring to Figures 8.12 and 8.14, the following equations can be derived for CCM and DCM operation:

$$\left. \begin{aligned} i_{L1\_dot} &= \frac{(V_S)}{L_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(V_S - V_{C1})}{L_1} \quad \text{for} \quad D.T \le t \le T \end{aligned} \right| \tag{8.57}$$

**TABLE 8.4**

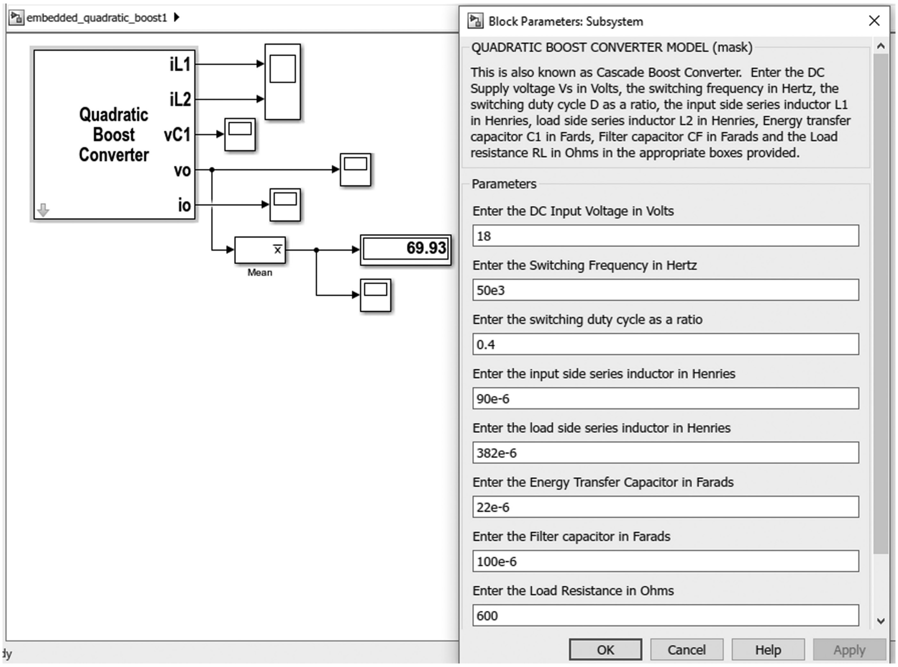
Quadratic Boost Converter Model Parameters

| **Sl. No.** | **Input Voltage $V_S$ (V)** | **Switching Frequency $f_{sw}$ (Hz)** | **Duty Cycle $D$** | **Inductor $L_1$ (H)** | **Inductor $L_2$ (H)** | **Capacitor $C_1$ (F)** | **Filter Capacitor $C_F$ (F)** | **Load Resistor $R_L$ (Ω)** | **Remarks** |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 18 | 50E3 | 0.4 | 90E−6 | 382E−6 | 22E−6 | 100E−6 | 50 | CCM |
| 2 | 18 | 50E3 | 0.4 | 90E−6 | 382E−6 | 22E−6 | 100E−6 | 600 | DCM |

Now, for the switch $S_1$ and inductor current $i_{L1}$, the switching functions SF and SF_I$_{L1}$ have already been defined in Equations 5.14 and 5.15, respectively. For the $L_2$ inductor current $i_{L2}$, the switch function SF_I$_{L2}$ is defined in Equation 8.26. The $L_2$ inductor current $i_{L2}$, capacitor voltage $V_{C1}$ and output voltage $V_O$ are defined as follows:

$$\begin{aligned} i_{L2\_dot} &= \frac{(V_{C1})}{L_2} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(V_{C1} - V_O)}{L_2} \quad \text{for} \quad D.T \le t \le T \end{aligned} \tag{8.58}$$

$$\begin{aligned} v_{C1\_dot} &= \frac{-I_{L2}}{C_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(I_{L1} - I_{L2})}{C_1} \quad \text{for} \quad D.T \le t \le T \end{aligned} \tag{8.59}$$


embedded_quadratic_boost1
Quadratic Boost Converter
iL1
iL2
vC1
vo
io
Mean
69.93
Block Parameters: Subsystem
OK
Cancel
Help
Apply

QUADRATIC BOOST CONVERTER MODEL (mask)

This is also known as Cascade Boost Converter. Enter the DC Supply voltage Vs in Volts, the switching frequency in Hertz, the switching duty cycle D as a ratio, the input side series inductor L1 in Henries, load side series inductor L2 in Henries, Energy transfer capacitor C1 in Fards, Filter capacitor CF in Farads and the Load resistance RL in Ohms in the appropriate boxes provided.

Parameters

Enter the DC Input Voltage in Volts
18

Enter the Switching Frequency in Hertz
50e3

Enter the switching duty cycle as a ratio
0.4

Enter the input side series inductor in Henries
90e-6

Enter the load side series inductor in Henries
382e-6

Enter the Energy Transfer Capacitor in Farads
22e-6

Enter the Filter capacitor in Farads
100e-6

Enter the Load Resistance in Ohms
600

**FIGURE 8.16**
Quadratic boost converter.

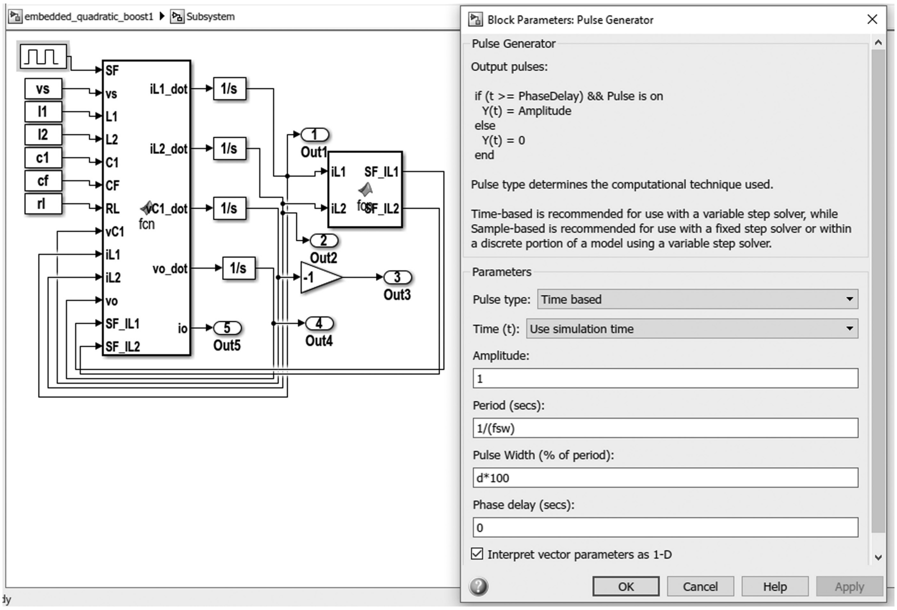
$$
\left.
\begin{aligned}
v_{O\_dot} &= \frac{-V_O}{(R_L.C_F)} \quad \text{for} \quad 0 \le t \le D.T \\
&= \frac{\left(I_{L2} - \dfrac{V_O}{R_L}\right)}{C_F} \quad \text{for} \quad D.T \le t \le T
\end{aligned}
\right| \tag{8.60}
$$

Load current $I_O$ is given by Equation 5.19. In Equations 8.55 through 8.58, the symbol *_dot* indicates the first derivative with respect to time of the respective variable. These equations are valid for DCM by replacing $D.T <= t <= T$ by $D.T <= t <= D_1.T$. The $L_2$ inductor current flows through diode $D_2$ and the load resistor and filter capacitor during the switch OFF period in CCM and in DCM until this inductor current through $L_2$ falls to zero. The output voltage equation is formulated by observation of equivalent circuits for CCM and DCM (Figures 8.12 and 8.14), as shown in Equation 8.60.

The interactive model of the quadratic boost converter suitable for CCM and DCM operation with a dialogue box is shown in Figure 8.16 and the model subsystem with a dialogue box is shown in Figure 8.17.

The data in the dialogue box in Figure 8.16 corresponds to DCM operation. For CCM operation, the relevant data are entered in the dialogue box.

The switch function SF for the switch defined in Equation 5.14 is generated using the Pulse Generator block, whose amplitude is 1, pulse width (d*100) (% of period) and switching period 1/($f_{sw}$), where *d* is the duty ratio and fsw


embedded_quadratic_boost1 ▸ Subsystem
vs
l1
l2
c1
cf
rl
SF
vs
L1
L2
C1
CF
RL
vC1
iL1
iL2
vo
SF_IL1
SF_IL2
iL1_dot
iL2_dot
vC1_dot
fcn
vo_dot
io
1/s
1/s
1/s
1/s
1
Out1
iL1
iL2
SF_IL1
SF_IL2
fcn
2
Out2
-1
3
Out3
4
Out4
5
Out5

Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): 1/(fsw)

Pulse Width (% of period): d*100

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

OK
Cancel
Help
Apply

**FIGURE 8.17**
Quadratic boost converter model subsystem.

is the frequency of switching. The switch function for $L_1$ inductor current SF_I$_{L1}$, defined in Equation 5.15, is generated using the embedded MATLAB function, whose input is $I_{L1}$ and output is SF_I$_{L1}$, as shown in Figure 8.17. The switch function for $L_2$ inductor current SF_I$_{L2}$, defined in Equation 8.26, is also generated in the same embedded MATLAB function, whose input is $I_{L2}$ and output is SF_I$_{L2}$. The source code for generating SF_I$_{L1}$ and SF_I$_{L2}$ are the same as given in Section 8.4. Equations 8.57 through 8.60 are solved using another embedded MATLAB function and integrators as shown in Figure 8.17 and the source code is written as explained in Section 8.4.

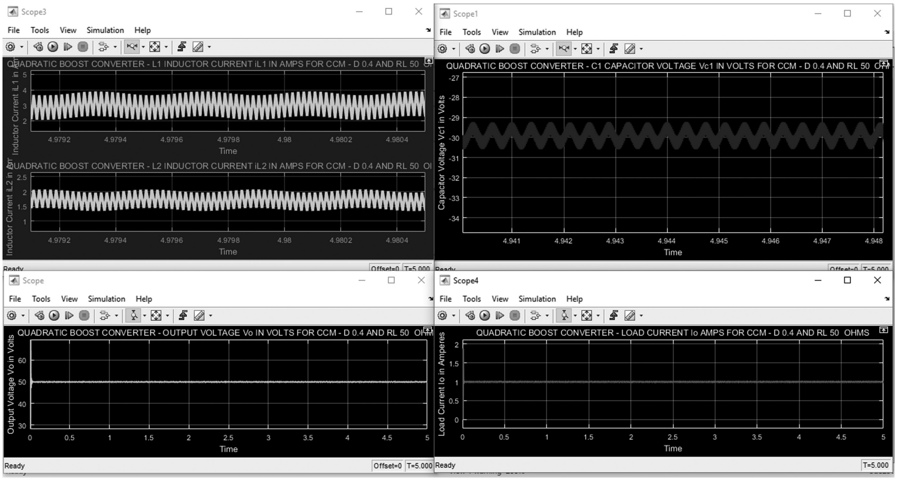

Scope3
File Tools View Simulation Help
QUADRATIC BOOST CONVERTER - L1 INDUCTOR CURRENT iL1 IN AMPS FOR CCM - D 0.4 AND RL 50
Inductor Current iL1 in
QUADRATIC BOOST CONVERTER - L2 INDUCTOR CURRENT iL2 IN AMPS FOR CCM - D 0.4 AND RL 50
Inductor Current iL2 in
Time
Scope1
QUADRATIC BOOST CONVERTER - C1 CAPACITOR VOLTAGE Vc1 IN VOLTS FOR CCM - D 0.4 AND RL 50
Capacitor Voltage Vc1 in Volts
Time
Scope
QUADRATIC BOOST CONVERTER - OUTPUT VOLTAGE Vo IN VOLTS FOR CCM - D 0.4 AND RL 50
Output Voltage Vo in Volts
Time
Scope4
QUADRATIC BOOST CONVERTER - LOAD CURRENT Io AMPS FOR CCM - D 0.4 AND RL 50 OHMS
Load Current Io in Amperes
Time
Ready
Offset=0
T=5.000

**FIGURE 8.18**
Quadratic boost converter in CCM for $D = 0.4$: simulation results.

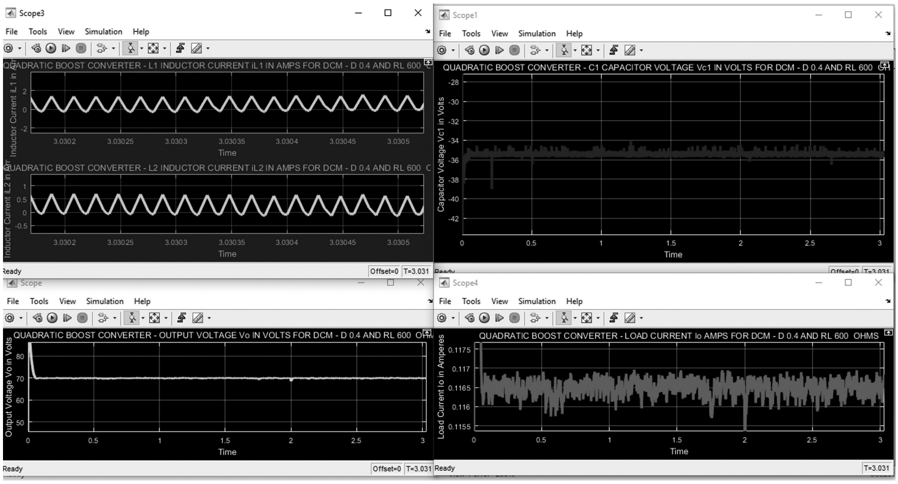

Scope3
File Tools View Simulation Help
QUADRATIC BOOST CONVERTER - L1 INDUCTOR CURRENT iL1 IN AMPS FOR DCM - D 0.4 AND RL 600
Inductor Current iL1 in
QUADRATIC BOOST CONVERTER - L2 INDUCTOR CURRENT iL2 IN AMPS FOR DCM - D 0.4 AND RL 600
Inductor Current iL2 in
Time
Scope1
QUADRATIC BOOST CONVERTER - C1 CAPACITOR VOLTAGE Vc1 IN VOLTS FOR DCM - D 0.4 AND RL 600
Capacitor Voltage Vc1 in Volts
Time
Scope
QUADRATIC BOOST CONVERTER - OUTPUT VOLTAGE Vo IN VOLTS FOR DCM - D 0.4 AND RL 600
Output Voltage Vo in Volts
Time
Scope4
QUADRATIC BOOST CONVERTER - LOAD CURRENT Io AMPS FOR DCM - D 0.4 AND RL 600 OHMS
Load Current Io in Amperes
Time
Ready
Offset=0
T=3.031

**FIGURE 8.19**
Quadratic boost converter in DCM for $D = 0.4$: simulation results.

**TABLE 8.5**

Quadratic Boost Converter: Simulation Results

| **Sl. No.** | **Duty Ratio** | **Minimum $L_1$ Inductor Current (A)** | **Maximum $L_1$ Inductor Current (A)** | **Minimum $L_2$ Inductor Current (A)** | **Maximum $L_2$ Inductor Current (A)** | **Capacitor $C_1$ Voltage $V_{C1}$ (V)** | **Output Voltage $V_O$ (V)** | **Load Current $I_O$ (A)** | **Remarks** |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.4 | 2.04 | 3.9 | 1.34 | 2.07 | −29.9 | 49.9 | 0.9979 | CCM |
| 2 | 0.4 | −0.204 | 1.58 | −0.137 | 0.737 | −35.48 | 70.17 | 0.117 | DCM |

**TABLE 8.6**

Quadratic Boost Converter: Calculated Values

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $V_{C1}$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.4 | 1.977 | 3.577 | 1.038 | 2.2944 | –30 | 50 | 1.0 | CCM |
| 2 | 0.4 | –0.064 | 1.536 | –0.163 | 0.4435 | –38.92 | 84.156 | 0.140 | DCM |

The embedded MATLAB outputs $v_{O\_dot}$, $v_{C1\_dot}$, $i_{L1\_dot}$ and $i_{L2\_dot}$ are integrated using Integrator blocks to obtain the required outputs and are used as feedback inputs along with SF_I$_{L1}$ and SF_I$_{L2}$ to solve Equations 8.57 through 8.60.

### 8.7.1 Simulation Results

The simulation of the quadratic boost converter for CCM and DCM operations were carried out using Simulink [9]. The ode23t (mod. stiff/trapezoidal) solver was used. The data shown in Table 8.4 were used for simulation. The simulation results for the quadratic boost converter in CCM are shown in Figure 8.18 and those for DCM are shown in Figure 8.19. Simulation results and calculated values are tabulated in Tables 8.5 and 8.6.

## 8.8 Analysis of Ultra-Lift Luo Converter in the CCM

The ultra-lift Luo converter schematic is shown in Figure 8.20 [2, 12]. The switch $S_1$ is driven by a gate pulse whose period is $T$ and duty cycle is $D$. The switch $S_1$ is ON for the interval $0 <= t <= 1D.T$ s and OFF for the interval $D.T <= t <= T$ s. The equivalent circuit of the ultra-lift Luo converter in CCM is shown in Figure 8.21. The analysis of this converter in CCM is given next:

Referring to Figure 8.21, the average inductor current through $L_1$ and $L_2$ and, similarly, the average voltage across $C_1$ and $C_F$ over one switching cycle is zero. We have the following equations:

$$\frac{(V_S.D.T)}{L_1}+\frac{(V_{C1}).(1-D).T}{L_1}=0 \tag{8.61}$$

$$\frac{((V_S-V_{C1}).D.T)}{L_2}+\frac{(V_O-V_{C1}).(1-D).T}{L_2}=0 \tag{8.62}$$

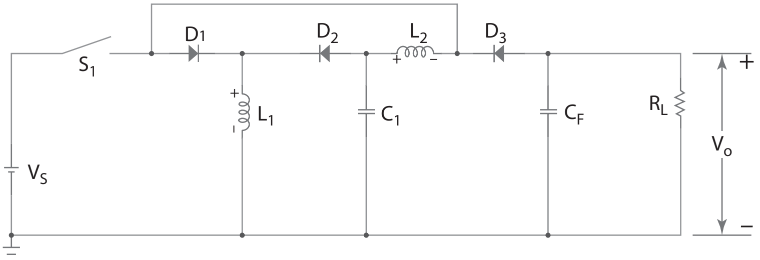


**FIGURE 8.20**
Ultra-lift Luo converter.

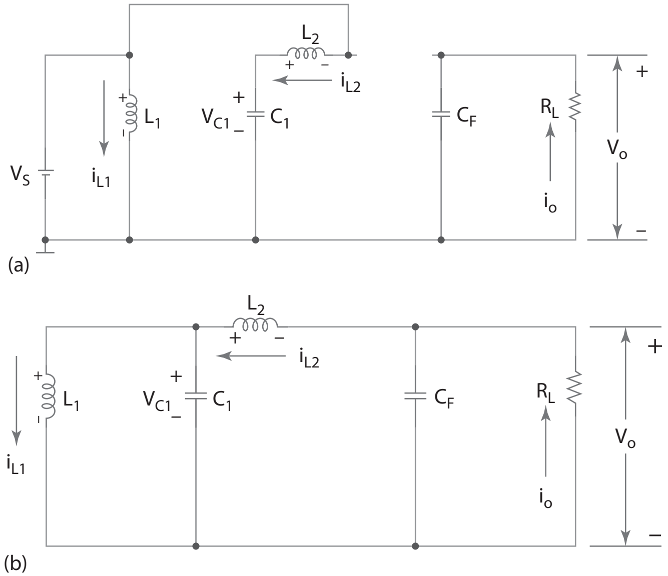


**FIGURE 8.21**
Ultra-lift Luo converter in CCM equivalent circuits. (a) Switch ON for $0 \leq t \leq D.T$ s. (b) Switch OFF for $D.T \leq t \leq T$ s.

From Equation 8.61,

$$\frac{V_{C1}}{V_S} = \frac{-D}{(1-D)} \tag{8.63}$$

Using Equation 8.63 in Equation 8.62 and simplifying,

$$\frac{V_O}{V_S} = \frac{-D.(2-D)}{(1-D)^2} \tag{8.64}$$

The minus sign in Equations 8.63 and 8.64 indicates that the polarities of $V_{C1}$ and $V_O$ in Figure 8.20 are negative at the top and positive at the bottom terminal. The waveforms of inductor currents $i_{L1}$, $i_{L2}$ and load current $i_O$ are shown in Figure 8.22 for CCM operation. The average capacitor voltage across $C_1$ and $C_F$ over one switching cycle is zero. This leads to the following equations:

$$\frac{I_{L2}.D.T}{C_1} + \frac{(I_{L2} - I_{L1}).(1-D).T}{C_1} = 0 \tag{8.65}$$

$$\frac{I_O.D.T}{C_F} + \frac{(I_O - I_{L2}).(1-D).T}{C_F} = 0 \tag{8.66}$$

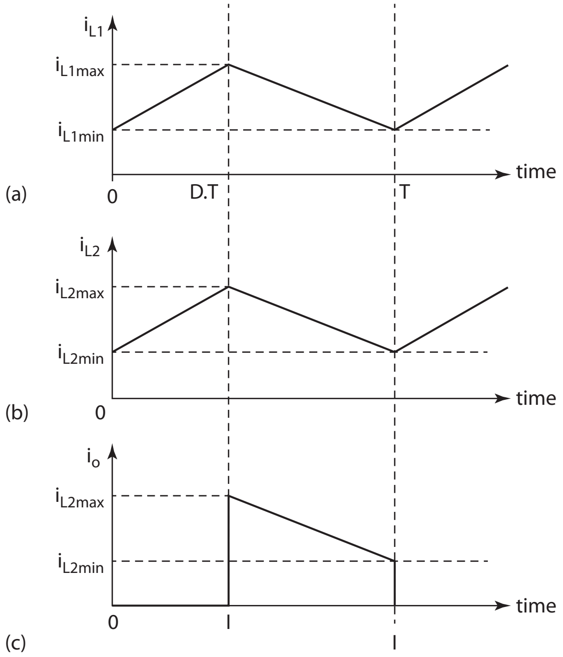


**FIGURE 8.22**
Ultra-lift Luo converter waveforms in CCM. (a) Inductor $L_1$ current $i_{L1}$. (b) Inductor $L_2$ current $i_{L2}$. (c) Load current $I_O$.

From Equations 8.65 and 8.66,

$$\frac{I_{L1}}{I_{L2}} = \frac{1}{(1-D)} \tag{8.67}$$

$$I_{L2} = \frac{I_O}{(1-D)} = \frac{V_O}{R_L.(1-D)} \tag{8.68}$$

Using Equation 8.68 in Equation 8.67,

$$I_{L1} = \frac{I_O}{(1-D)^2} = \frac{V_O}{R_L.(1-D)^2} \tag{8.69}$$

Using Equation 8.64 in Equations 8.68 and 8.69,

$$I_{L2} = \frac{V_S.D.(2-D)}{R_L.(1-D)^3} \tag{8.70}$$

$$I_{L1} = \frac{V_S.D.(2-D)}{R_L.(1-D)^4} \tag{8.71}$$

The maximum and minimum value of current through inductor $L_1$ and $L_2$ can be expressed as follows:

$$\left.\begin{aligned} I_{L1\max} &= \frac{V_S.D.(2-D)}{R_L.(1-D)^4} + \frac{V_S.D.T}{2.L_1} \\ I_{L1\min} &= \frac{V_S.D.(2-D)}{R_L.(1-D)^4} - \frac{V_S.D.T}{2.L_1} \end{aligned}\right| \tag{8.72}$$

$$\left.\begin{aligned} I_{L2\max} &= \frac{V_S.D.(2-D)}{R_L.(1-D)^3} + \frac{V_S.D.T}{2.L_2.(1-D)} \\ I_{L2\min} &= \frac{V_S.D.(2-D)}{R_L.(1-D)^3} - \frac{V_S.D.T}{2.L_2.(1-D)} \end{aligned}\right| \tag{8.73}$$

Equating $I_{L1\min}$ and $I_{L2\min}$ in Equations 8.72 and 8.73 to zero, the critical inductances $L_{1\_\text{crit}}$ and $L_{2\_\text{crit}}$ can be expressed as follows:

$$L_{1\_\text{crit}} = \frac{V_S.D.T.R_L.(1-D)^4}{2.D.(2-D)} \tag{8.74}$$

$$L_{2\_\text{crit}} = \frac{V_S.D.T.R_L.(1-D)^2}{2.D.(2-D)} \tag{8.75}$$

Equations 8.74 and 8.75 give the minimum value of inductance for $L_1$ and $L_2$ to maintain CCM.

## 8.9 Analysis of Ultra-Lift Luo Converter in DCM

In DCM, the inductor currents $i_{L1}$ and $i_{L2}$ decay, reach zero during the switch OFF period and maintain a zero value until the switch is ON for the next cycle. The equivalent circuits for DCM operation are shown in Figure 8.23. The relevant waveforms for DCM operation are shown in Figure 8.24 [2, 12].

Referring to Figure 8.23, the average inductor currents $i_{L1}$ and $i_{L2}$ over one switching cycle is zero, which can be expressed as follows:

$$\frac{V_S.D.T}{L_1} + \frac{V_{C1}.(D_1 - D).\mathrm{T}}{L_1} = 0 \tag{8.76}$$

$$\frac{(V_S - V_{C1}).D.T}{L_2} + \frac{(V_0 - V_{C1}).(D_1 - D).T}{L_2} = 0 \tag{8.77}$$

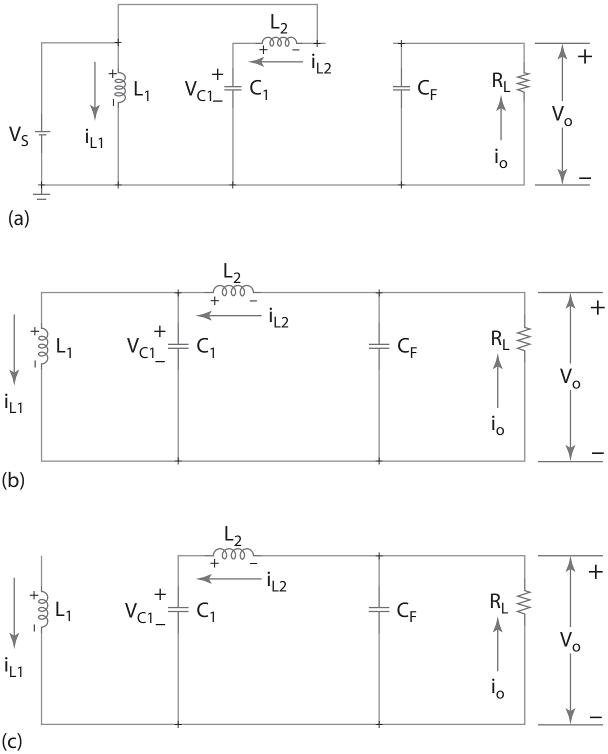


**FIGURE 8.23**
Ultra-lift Luo converter in DCM: equivalent circuits. (a) Switch ON for $0 \le t \le D.T$ s. (b) Switch OFF for $D.T \le t \le D_1.T$ s. (c) DCM operation.

From Equation 8.76, $V_{C1}$ can be expressed as follows:

$$V_{C1} = \frac{-V_S.D}{(D_1 - D)} \tag{8.78}$$

Using Equation 8.78 in 8.77 and simplifying,

$$\frac{V_O}{V_S} = \frac{-D.(2D_1 - D)}{(D_1 - D)^2} \tag{8.79}$$

Referring to Figures 8.23a and b, the inductor current $i_{L2}$ that flows during switch OFF contributes to the load voltage, $V_O$. Referring to Figure 8.24b, the maximum inductor current $i_{L2\max}$ can be expressed as follows:

$$i_{L2\max} = \frac{(V_S - V_{C1}).D.T}{L_2} \tag{8.80}$$

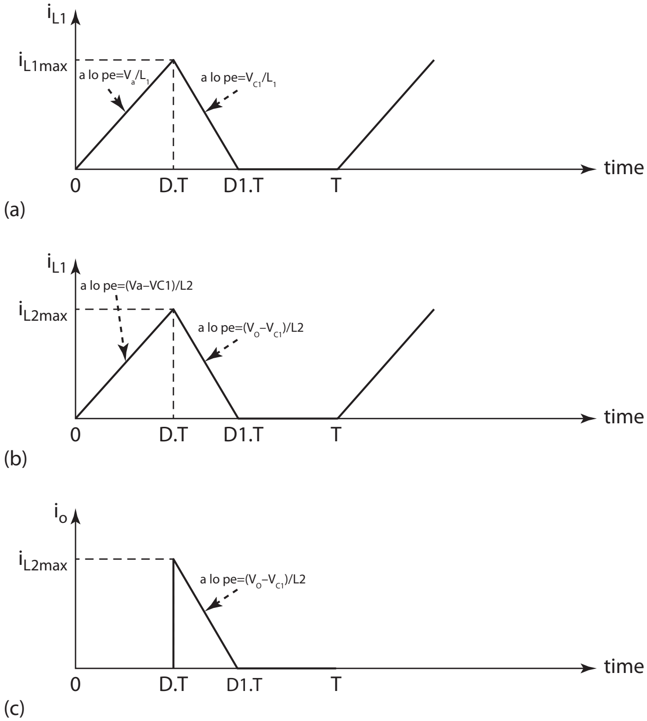


**FIGURE 8.24**
Ultra-lift Luo converter in DCM. (a) Inductor $L_1$ current $iL_1$. (b) Inductor $L_2$ current $iL_2$. and (c) Load current $I_O$.

Using Equation 8.78 in Equation 8.80,

$$i_{L2\max} = \frac{V_S.D_1.D.T}{(D_1 - D).L_2} \tag{8.81}$$

Referring to Figure 8.24c, the average load current $I_O$ can be expressed as follows:

$$\begin{aligned} I_O &= \left[\frac{1}{T} * \frac{1}{2}.(D_1 - D).T.\frac{V_S.D.D_1.T}{(D_1 - D).L_2}\right] \\ &= \frac{V_S.D.D_1.T}{2.L_2} \end{aligned} \tag{8.82}$$

$$V_O = -I_O * R_L = \frac{-V_S.D.D_1.T.R_L}{2.L_2} \tag{8.83}$$

$$\text{Let} \quad K = \frac{2.L_2}{T.R_L} \tag{8.84}$$

Using Equation 8.84 in Equation 8.83,

$$\frac{V_O}{V_S} = M = \frac{D.D_1}{K} \tag{8.85}$$

$$D_1 = \frac{K.M}{D} \tag{8.86}$$

Using Equation 8.86 in Equation 8.79,

$$\frac{V_O}{V_S} = M = \frac{2.K.M.D^2 - D^4}{\left[K^2.M^2 + D^4 - 2.M.K.D^2\right]} \tag{8.87}$$

Simplifying Equation 8.87,

$$M^3.K^2 - 2.M^2.K.D^2 + M.[D^4 - 2.K.D^2] + D^4 = 0 \tag{8.88}$$

The solution of Equation 8.88 gives three values for $M$, of which one is acceptable.

To calculate $D_1$, first find the acceptable value $M_1$ for $M$ from Equation 8.88. Then use this $M_1$ in Equation 8.79 to find acceptable value for $D_1$ whose range is $D < D_1 \leq 1$.

## 8.10 Model of Ultra-Lift Luo Converter in CCM and DCM

The model of the ultra-lift Luo converter is reported in references [2, 12]. Here, the switching function concept is used to develop the model [6–8]. The data used for the model is shown in Table 8.7. The development of the model is given as follows:

**TABLE 8.7**

Ultra-Lift Luo Converter Model Parameters

| **Parameter** | **Value** |
|---|---|
| Supply voltage $V_s$ | 10 V |
| Switching frequency $f_{sw}$ | 50 kHz |
| Duty cycle $D$ used | 0.6 |
| Inductor $L_1$ | 1 mH |
| Inductor $L_2$ | 1 mH |
| E.T. capacitor $C_1$ | 1 μF |
| Filter capacitor $C_F$ | 1 μF |
| Load resistance $R_L$ | 300 Ω for CCM<br>3000 Ω for DCM |

Referring to Figures 8.21 and 8.23, the following equations can be derived for CCM and DCM operation.

$$\left.\begin{aligned} i_{L1\_dot} &= \frac{(V_S)}{L_1} \quad \text{for} \quad 0 \le t \le D.T \\ &\frac{(V_{C1})}{L_1} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.89}$$

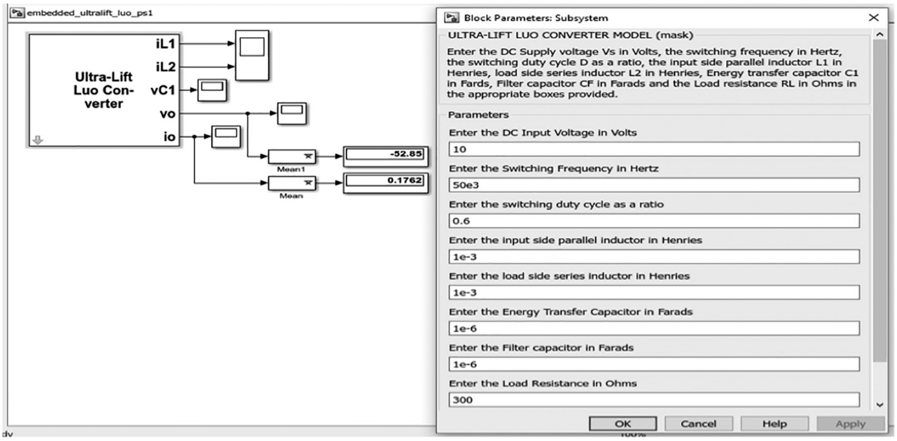
Now, for the switch $S_1$ and inductor current $i_{L1}$, the switching functions SF and SF_I$_{L1}$ have already been defined in Equations 5.14 and 5.15, respectively. For the $L_2$ inductor current $i_{L2}$, the switch function SF_I$_{L2}$ has been defined in Equation 8.26. The $L_2$ inductor current $i_{L2}$, capacitor voltage $V_{C1}$ and output voltage $V_O$ are defined as follows:

$$\left.\begin{aligned} i_{L2\_dot} &= \frac{(V_S - V_{C1})}{L_2} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(V_O - V_{C1})}{L_2} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.90}$$

$$\left.\begin{aligned} v_{C1\_dot} &= \frac{I_{L2}}{C_1} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{(I_{L2} - I_{L1})}{C_1} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.91}$$

$$\left.\begin{aligned} v_{O\_dot} &= \frac{-V_O}{(R_L.C_F)} \quad \text{for} \quad 0 \le t \le D.T \\ &= \frac{\left(I_{L2} - \dfrac{V_O}{R_L}\right)}{C_F} \quad \text{for} \quad D.T \le t \le T \end{aligned}\right| \tag{8.92}$$

Load current $I_O$ is given by Equation 5.19. In Equations 8.89 through 8.92, the symbol *_dot* indicates the first derivative with respect to time of the respective variable. These equations are valid for DCM by replacing $D.T <= t <= T$ by $D.T <= t <= D_1.T$. The $L_2$ inductor current flows through the load resistor and filter capacitor during the switch OFF period in CCM and in DCM until this inductor current through $L_2$ falls to zero. The output voltage equation is formulated by observation of equivalent circuits for CCM and DCM (Figures 8.21 and 8.23), as shown in Equation 8.92.


embedded_ultralift_luo_ps1
Ultra-Lift Luo Con- verter
iL1
iL2
vC1
vo
io
-52.85
0.1762
Mean1
Mean
Block Parameters: Subsystem
OK
Cancel
Help
Apply

ULTRA-LIFT LUO CONVERTER MODEL (mask)

Enter the DC Supply voltage Vs in Volts, the switching frequency in Hertz, the switching duty cycle D as a ratio, the input side parallel inductor L1 in Henries, load side series inductor L2 in Henries, Energy transfer capacitor C1 in Fards, Filter capacitor CF in Farads and the Load resistance RL in Ohms in the appropriate boxes provided.

Parameters

Enter the DC Input Voltage in Volts: 10

Enter the Switching Frequency in Hertz: 50e3

Enter the switching duty cycle as a ratio: 0.6

Enter the input side parallel inductor in Henries: 1e-3

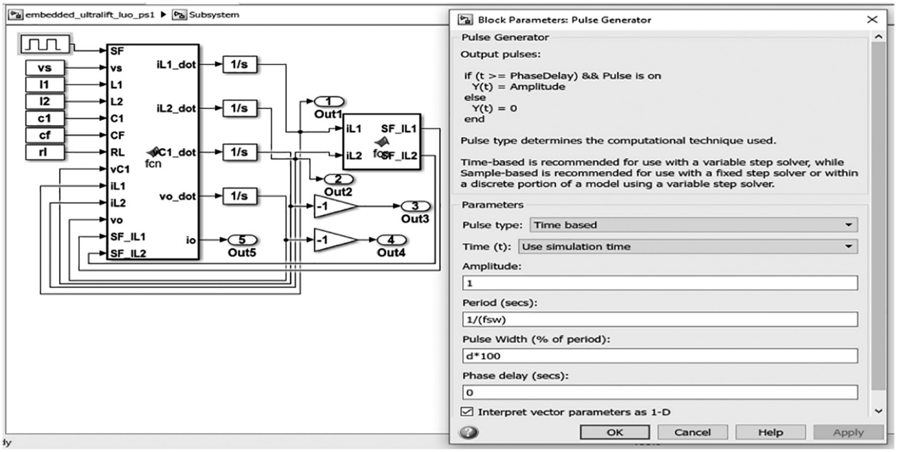
Enter the load side series inductor in Henries: 1e-3

Enter the Energy Transfer Capacitor in Farads: 1e-6

Enter the Filter capacitor in Farads: 1e-6

Enter the Load Resistance in Ohms: 300

**FIGURE 8.25**
Ultra-lift Luo converter model.


embedded_ultralift_luo_ps1 ▶ Subsystem
vs
l1
l2
c1
cf
rl
SF
vs
L1
L2
C1
CF
RL
vC1
iL1
iL2
vo
SF_IL1
SF_IL2
fcn
iL1_dot
iL2_dot
vC1_dot
vo_dot
io
1/s
1/s
1/s
1/s
1
Out1
2
Out2
-1
3
Out3
-1
4
Out4
5
Out5
iL1
iL2
SF_IL1
SF_IL2
fcn
Block Parameters: Pulse Generator
OK
Cancel
Help
Apply

Pulse Generator

Output pulses:

```
 if (t >= PhaseDelay) && Pulse is on
   Y(t) = Amplitude
 else
   Y(t) = 0
 end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): 1/(fsw)

Pulse Width (% of period): d*100

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

**FIGURE 8.26**
Ultra-lift Luo converter model subsystem.

The interactive model of the ultra-lift Luo converter suitable for CCM and DCM operation with a dialogue box is shown in Figure 8.25 and the model subsystem with a dialogue box is shown in Figure 8.26.

The data in the dialogue box in Figure 8.25 corresponds to CCM operation. For DCM operation, the relevant data, 3000 Ω for load resistance, is entered in the dialogue box.

The switch function SF for the switch defined in Equation 5.14 is generated using the Pulse Generator block, whose amplitude is 1, pulse width (d*100) (% of period) and switching period 1/(fsw) where d is the duty ratio and fsw is the frequency of switching.

The switch function for the $L_1$ inductor current SF_I$_{L1}$ defined in Equation 5.15 is generated using the embedded MATLAB function whose input is $I_{L1}$ and output is SF_I$_{L1}$, as shown in Figure 8.26. The switch function for $L_2$ inductor current SF_I$_{L2}$ defined in Equation 8.26 is also generated in the same embedded MATLAB function whose input is $I_{L2}$ and output is SF_I$_{L2}$. The source code for generating SF_I$_{L1}$ and SF_I$_{L2}$ are the same as given in Section 8.4. Equations 8.89 through 8.92 are solved using another embedded MATLAB function and integrators as shown in Figure 8.26 and the source code is written as explained in Section 8.4.

The embedded MATLAB outputs $v_{O\_dot}$, $v_{C1\_dot}$, $i_{L1\_dot}$ and $i_{L2\_dot}$ are integrated using Integrator blocks to obtain the required outputs and are used as feedback inputs along with SF_I$_{L1}$ and SF_I$_{L2}$ to solve Equations 8.89 through 8.92.

### 8.10.1 Simulation Results

The simulation of the ultra-lift Luo converter is carried out using the ode23t (mod. stiff/trapezoidal) solver in Simulink [9]. The MATLAB program to solve Equation 8.88 is shown in Program Segment 8.1 and the result is in Figure 8.27. The simulation results for CCM are shown in Figure 8.28 and those for DCM are shown in Figure 8.29. The simulation results and the theoretically calculated values are tabulated in Tables 8.8 and 8.9 respectively.

```
%%Program Segment 8.1
%%Ultra-Lift Luo Converter in DCM, %%Program author: Dr.
Narayanaswamy.P.R.Iyer
vs = 10;
l1 = 1e-3;
l2 = 1e-3;
c1 = 1e-6;
cf = 1e-6;
rl = 3000;
tsw = 1/(50e3);
d = 0.6;
k = (2*l2)/(tsw*rl);
%%function f(m) = M^(3)*K^(2) - 2.M^(2)*D^(2)*K + M*(D^(4)
                 - 2*K*D^(2)) + D^(4)
%%Let M be the voltage gain Vo/Vs
for M = 1:15,
    m = M;
    x(m) = m;
    f(m) = (m^(3))*(k^(2)) - 2*(m^(2))*(d^(2))*k
           + m*((d^(4)) - 2*k*(d^(2))) + d^(4);
end
plot(x,f,'-k'),grid;
xlabel('Voltage gain M');
ylabel('Function f');
title('Ultra-lift Luo Converter in DCM');
```

From Figure 8.27, the acceptable value of voltage gain *M*, which makes function *f* zero, is 8.2. The value of $D_1$ calculated using Equation 8.86 is not acceptable. The acceptable value $M_1$ of *M* is 8.2, obtained by solving Equation 8.88. This value of $M_1$ is substituted in Equation 8.79 to find the acceptable value of $D_1$, which is found to be 0.8951.

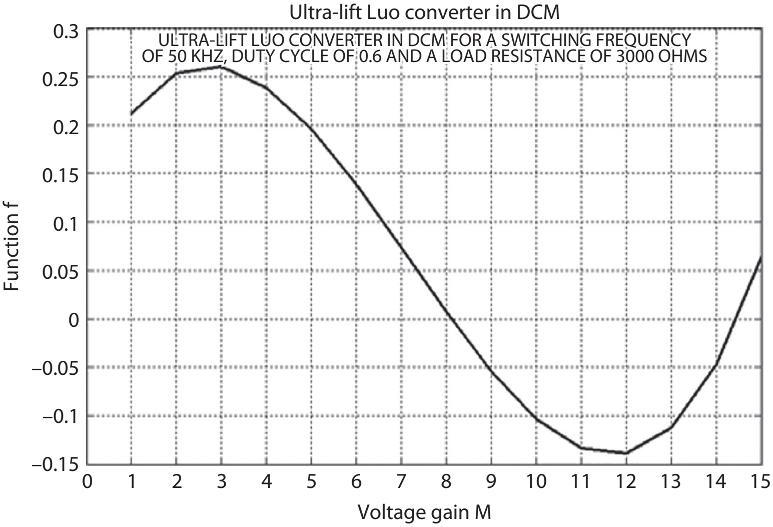


**FIGURE 8.27**
Ultra-lift Luo converter: simulation of Program Segment 8.1.

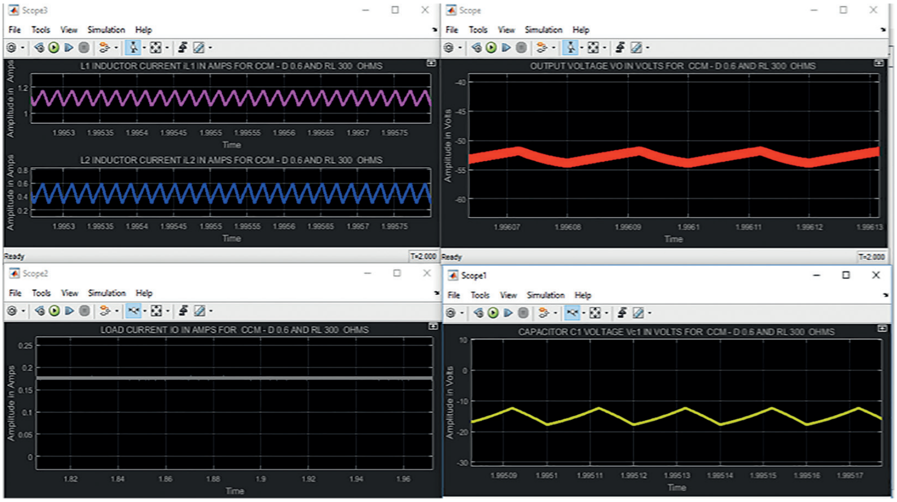

Scope3
File Tools View Simulation Help
L1 INDUCTOR CURRENT iL1 IN AMPS FOR CCM - D 0.6 AND RL 300 OHMS
Amplitude in Amps
1.2
1
1.9953 1.99535 1.9954 1.99545 1.9955 1.99555 1.9956 1.99565 1.9957 1.99575
Time
L2 INDUCTOR CURRENT iL2 IN AMPS FOR CCM - D 0.6 AND RL 300 OHMS
Amplitude in Amps
0.8
0.6
0.4
0.2
1.9953 1.99535 1.9954 1.99545 1.9955 1.99555 1.9956 1.99565 1.9957 1.99575
Time
Ready
T=2.000
Scope
File Tools View Simulation Help
OUTPUT VOLTAGE VO IN VOLTS FOR CCM - D 0.6 AND RL 300 OHMS
Amplitude in Volts
-40
-45
-50
-55
-60
1.99607 1.99608 1.99609 1.9961 1.99611 1.99612 1.99613
Time
Ready
T=2.000
Scope2
File Tools View Simulation Help
LOAD CURRENT IO IN AMPS FOR CCM - D 0.6 AND RL 300 OHMS
Amplitude in Amps
0.25
0.2
0.15
0.1
0.05
0
1.82 1.84 1.86 1.88 1.9 1.92 1.94 1.96
Time
Scope1
File Tools View Simulation Help
CAPACITOR C1 VOLTAGE Vc1 IN VOLTS FOR CCM - D 0.6 AND RL 300 OHMS
Amplitude in Volts
10
0
-10
-20
-30
1.99509 1.9951 1.99511 1.99512 1.99513 1.99514 1.99515 1.99516 1.99517
Time

**FIGURE 8.28**
Ultra-lift Luo converter in CCM: simulation results.

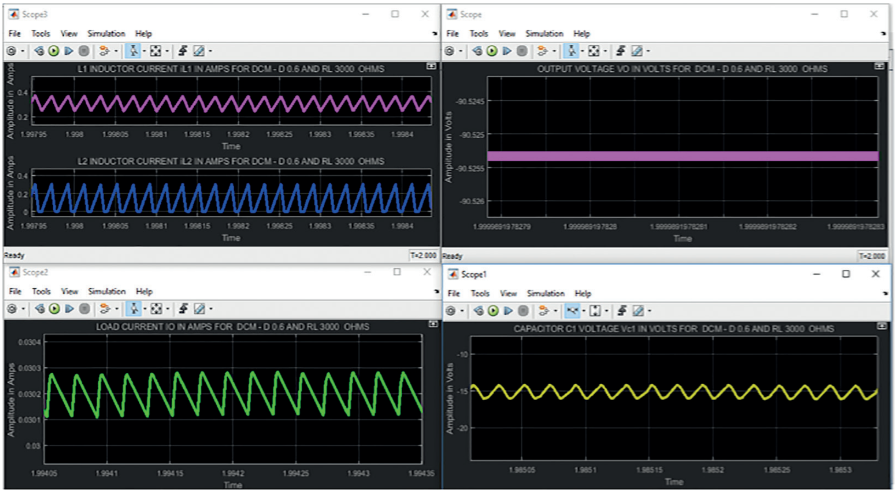

Scope3
File Tools View Simulation Help
L1 INDUCTOR CURRENT iL1 IN AMPS FOR DCM - D 0.6 AND RL 3000 OHMS
Amplitude in Amps
0.4
0.2
1.99795 1.998 1.99805 1.9981 1.99815 1.9982 1.99825 1.9983 1.99835 1.9984
Time
L2 INDUCTOR CURRENT iL2 IN AMPS FOR DCM - D 0.6 AND RL 3000 OHMS
Amplitude in Amps
0.4
0.2
0
1.99795 1.998 1.99805 1.9981 1.99815 1.9982 1.99825 1.9983 1.99835 1.9984
Time
Ready
T=2.000
Scope
File Tools View Simulation Help
OUTPUT VOLTAGE VO IN VOLTS FOR DCM - D 0.6 AND RL 3000 OHMS
Amplitude in Volts
-90.5245
-90.525
-90.5255
-90.526
1.9999891978279 1.999989197828 1.9999891978281 1.9999891978282 1.9999891978283
Time
Ready
T=2.000
Scope2
File Tools View Simulation Help
LOAD CURRENT IO IN AMPS FOR DCM - D 0.6 AND RL 3000 OHMS
Amplitude in Amps
0.0304
0.0303
0.0302
0.0301
0.03
1.99405 1.9941 1.99415 1.9942 1.99425 1.9943 1.99435
Time
Scope1
File Tools View Simulation Help
CAPACITOR C1 VOLTAGE Vc1 IN VOLTS FOR DCM - D 0.6 AND RL 3000 OHMS
Amplitude in Volts
-10
-15
-20
1.98505 1.9851 1.98515 1.9852 1.98525 1.9853
Time

**FIGURE 8.29**
Ultra-lift Luo converter in DCM: simulation results.

## 8.11 Conclusions

Interactive system models for the SEPIC, quadratic boost and ultra-lift Luo converters are presented in this chapter. All the models developed in this chapter can be used for both CCM and DCM.

Simulation results and calculated values for the SEPIC converter in Tables 8.2 and 8.3 show that the deviation of simulation results for $I_{L1\min}$, $I_{L1\max}$, $I_{L2\min}$, $I_{L2\max}$, $V_{C1}$, $V_O$ and $I_O$ from the calculated values using formulae are very small for both CCM and DCM.

In the case of the quadratic boost converter, the simulation values such as $I_{L1\min}$ and $I_{L1\max}$ for CCM almost agree with the calculated values. Similarly, $I_{L2\min}$ and $I_{L2\max}$ for CCM have a small discrepancy with the calculated values. The simulation and calculated values for capacitor voltage $V_{C1}$, output voltage $V_O$ and the load current for the case of CCM agree well. For DCM, shown in Tables 8.5 and 8.6, these values by simulation differ by a small percentage from the calculated values. The deviation of the simulation results for the $V_{C1}$, $V_O$ and $I_O$ values in the case of DCM are, respectively, 12.5%, 16.67% and 14.3% from calculated results.

For the ultra-lift Luo converter, the simulation results for $i_{L1\min}$, $i_{L1\max}$, $i_{L2\min}$, $i_{L2\max}$, $V_{C1}$, $V_O$ and $I_O$ agree closely with the calculated values in the case of CCM, and all these simulation results except $V_{C1}$ agree closely with the calculated values in the case of DCM shown in Tables 8.8 and 8.9. In DCM, the value of $V_{C1}$ by simulation differs by around 25% from the calculated value. Similarly, the simulation result for $V_O$ for DCM differs by 10.9% from the calculated value.

**TABLE 8.8**

Ultra-lift Luo Converter: Simulation Results

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $V_{C1}$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.6 | 1.055 | 1.175 | 0.293 | 0.597 | −15.29 | −52.9 | 0.1763 | CCM |
| 2 | 0.6 | 0.241 | 0.366 | −0.0055 | 0.306 | −15.43 | −90.7 | 0.032 | DCM |

**TABLE 8.9**

Ultra-lift Luo Converter: Calculated Values

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $V_{C1}$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.6 | 1.034 | 1.154 | 0.287 | 0.587 | –15 | –52.5 | 0.175 | CCM |
| 2 | 0.6 | 0.254 | 0.374 | –0.1107 | 0.296 | –20.33 | –82.00 | 0.0273 | DCM |

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# 9

# *Interactive Models for Three-Phase Multilevel Inverters*

## 9.1 Introduction

Multilevel inverters were proposed to obtain higher output voltages without the use of step-up transformers closely following a sinusoidal waveform. Additionally, the harmonic content in the output voltage waveform is greatly reduced in comparison with conventional two-level inverters [1–6]. Hence, they find wide applications in STATCOMs, adjustable speed drives (ASDs) and so on. This chapter describes the interactive system modelling of the three-phase diode-clamped three-level inverter (DCTLI) and the three-phase flying-capacitor three-level inverter (FCTLI). The highest number of levels obtainable with diode-clamped and flying-capacitor multilevel inverters are limited by factors such as the number and voltage ratings of the clamping diodes and capacitors, respectively. In general, if $m$ is the number of voltage levels in the phase-to-ground voltage of the three-phase multilevel inverter, then the number of voltage levels in the line-to-line voltage will be $(2.m-1)$ and the number of switching pulses will be $6*(m-1)$ [2–4]. Thus, for a three-phase DCTLI or FCTLI, the number of voltage levels for the line-to-line voltage will be five and the number of gate pulses required (i.e. semiconductor switches) will be twelve.

Another multilevel inverter topology is the cascaded multilevel inverter (CHB). In this topology, several of the conventional single-phase four-switch H-bridge inverters are connected in cascade to obtain higher output voltage, each H-bridge inverter with a separate DC source. The DC source for each H-bridge inverter can be equal or unequal. In the former case, it is called a *symmetrical cascade H-bridge (SCHB) inverter*, and in the latter, it is called an *unsymmetrical cascaded H-bridge (UCHB) inverter.* The total output voltage is the algebraic sum of the output voltage of each H-bridge inverter cell. The number of output phase-to-ground voltage levels $m$ in a CHB inverter is defined by $m=(2*s+1)$ where $s$ is the number of separate

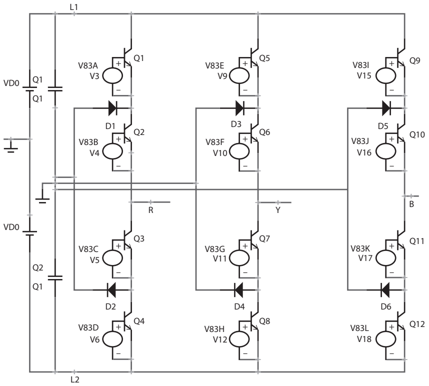
DC sources or the H-bridge inverter cell. Also, CHB inverter topology can be combined with DCTLI and FCTLI topology to form a new multilevel inverter topology.

As for a conventional inverter, several pulse width modulation (PWM) schemes are available for multilevel inverters such as the multi-carrier sine PWM (MSPWM), selective harmonic elimination PWM (SHE-PWM) and space vector PWM (SVPWM). Also, the MSPWM is classified into two groups, namely, multi-carrier level-shift PWM (MLSPWM) and multi-carrier phase-shift PWM (MPSPWM).

In this chapter, interactive system models are developed for three-phase DCTLI, FCTLI, the SCHB inverter, MLSPWM and MPSPWM.

## 9.2 Three-Phase Diode-Clamped Three-Level Inverter

The circuit schematic of the three-phase DCTLI is shown in Figure 9.1 using Microcap11 software [1–6,7]. There are four switches per phase, two at the top leg and two at the bottom leg. Two diodes in series are connected in between the top and bottom switches. The two capacitors at the input act as a potential divider. The DC link voltage is $2.V_{dc}$ V. The simulation results for the three-phase line-to-ground and line-to-line voltages are shown in Figure 9.2. As can be seen from Figure 9.2, the line-to-ground voltage has three voltage levels and the line-to-line voltage has five voltage levels.



```
.DEFINE VDC 190.5

.DEFINE C1 0.1

.DEFINE VGSA PULSE (0  5  0M  0M  0M  5M  20M)

.DEFINE VGSB PULSE (0  5  15M  0M  0M  15M  20M)

.DEFINE VGSC PULSE (0  5  5M  0M  0M  15M  20M)

.DEFINE VGSD PULSE (0  5  10M  0M  0M  5M  20M)

.DEFINE VGSE PULSE (0  5  6.667M 0M  0M  5M  20M)

.DEFINE VGSF PULSE (0  5  1.667M  0M  0M  15M  20M)

.DEFINE VGSG PULSE (0  5  11.667M  0M  0M  15M  20M)

.DEFINE VGSH PULSE (0  5  16.667M  0M 0M  5M  20M)

.DEFINE VGSI PULSE (0  5  13.333M  0M  0M  5M  20M)

.DEFINE VGSJ PULSE (0  5  8.333M  0M  0M  15M  20M)

.DEFINE VGSK PULSE (0  5  18.333M  0M  0M  15M  20M)

.DEFINE VGSL PULSE (0  5  3.333M  0M  0M  5M  20M)

.MODEL D1N4148 D (IS=5.95852N N=1.91266 BV=500 RS=589.498M TT=1.12599N
CJO=1.33941PVJ=8.66264 M=300M RL=3.149686)V

.MODEL 2N2222 NPN (IS=10.017F BF=506.842 NF=979.99M VAF=100 IKF=696.241M
ISE=0.241303F NE=1.05779 BR=154.978M IKR=999.407 ISC=6.94996P RE=668.817M
CJE=42.4239P VJE=700M MJE=642.887M CJC=36.6437P VJC=700M MJC=558.066M
TF=484.887 XTF=500.001M VTF=10 ITF=9.88166M TR=2.26629U)
```

**FIGURE 9.1**
Three-phase DCTLI.

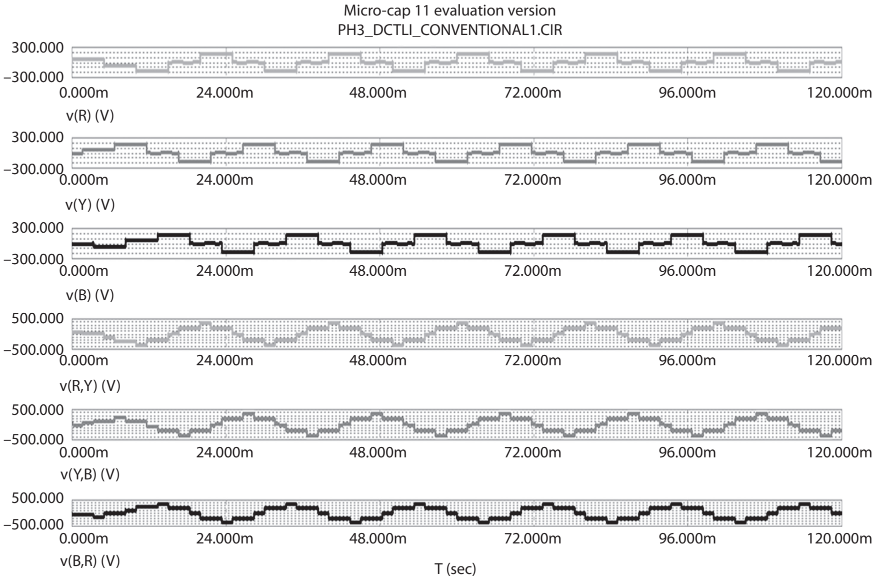


**FIGURE 9.2**
Three-phase DCTLI: output voltage waveforms.

### 9.2.1 Modelling of Three-Phase Diode-Clamped Three-Level Inverter

The model of the three-phase DCTLI is shown in Figure 9.3 [8]. The dialogue boxes are shown in Figure 9.4. The various subsystems are shown in Figure 9.5a,b. A brief description of the various subsystems are given here:

Figure 9.5a corresponds to the dialogue box 'Three-Phase DCTLI Gate Drive' shown in Figure 9.4. The switching frequency of the inverter in hertz is entered in the box provided. The output of gate drives marked Out2, Out6, Out9 and Out12 in Figure 9.5a correspond to the switches Q1, Q2, Q3 and Q4 in Figure 9.1. Similarly, the outputs of gate drives marked Out1, Out5, Out8 and Out10 correspond to switches Q5, Q6, Q7 and Q8, and the gate drive outputs marked Out3, Out4, Out7 and Out11 correspond to switches Q9, Q10, Q11 and Q12 in Figure 9.1. The switching table for the switches Q1, Q2, Q3 and Q4 in Phase R is shown in Table 9.1. The same table can be used for switches in Phases Y and B by replacing Q1 to Q4 by Q5 to Q8 or Q9 to Q12 in respective order. The start point of the appropriate phases may be noted from the remarks column of Table 9.1. If $d$ is the time delay between any two neighbouring or consecutive states in Table 9.1, then this delay $d$ is $\pi/6$ rad. Table 9.1 is implemented as shown in Figure 9.5a using the Pulse Generator block. The amplitude of all the pulses in the Pulse Generator block is set to 1 and the period is set to [1/fsw], where fsw is the switching frequency of the inverter. The phase delay for each of the switches in Phases R, Y and B are tabulated in Table 9.2. The switch names are in Figure 9.1. In Table 9.1,

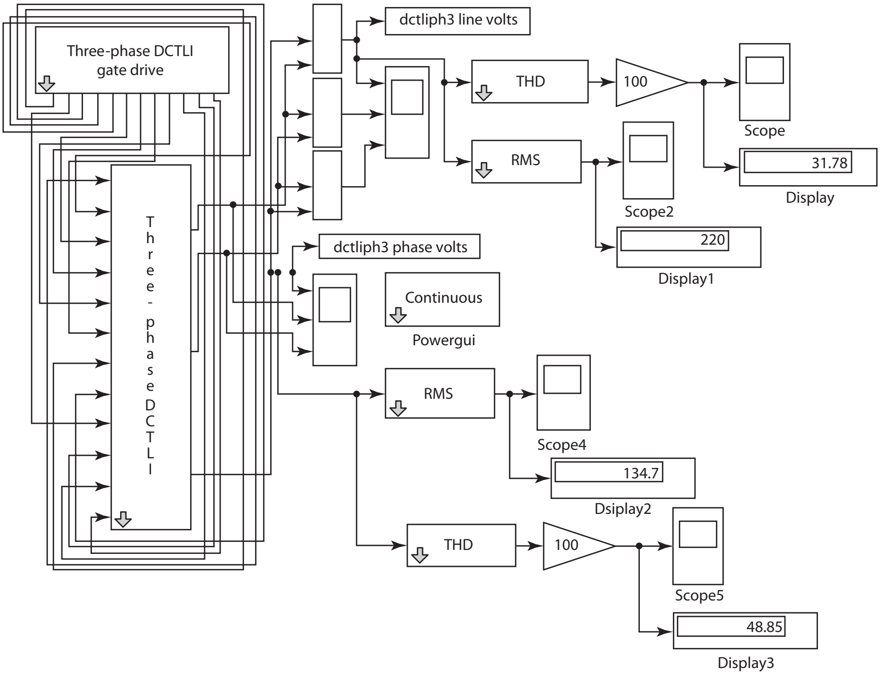

Three-phase DCTLI gate drive
Three-phase DCTLI
dctliph3 line volts
THD
100
Scope
31.78
Display
RMS
Scope2
220
Display1
dctliph3 phase volts
Continuous
Powergui
RMS
Scope4
134.7
Dsiplay2
THD
100
Scope5
48.85
Display3

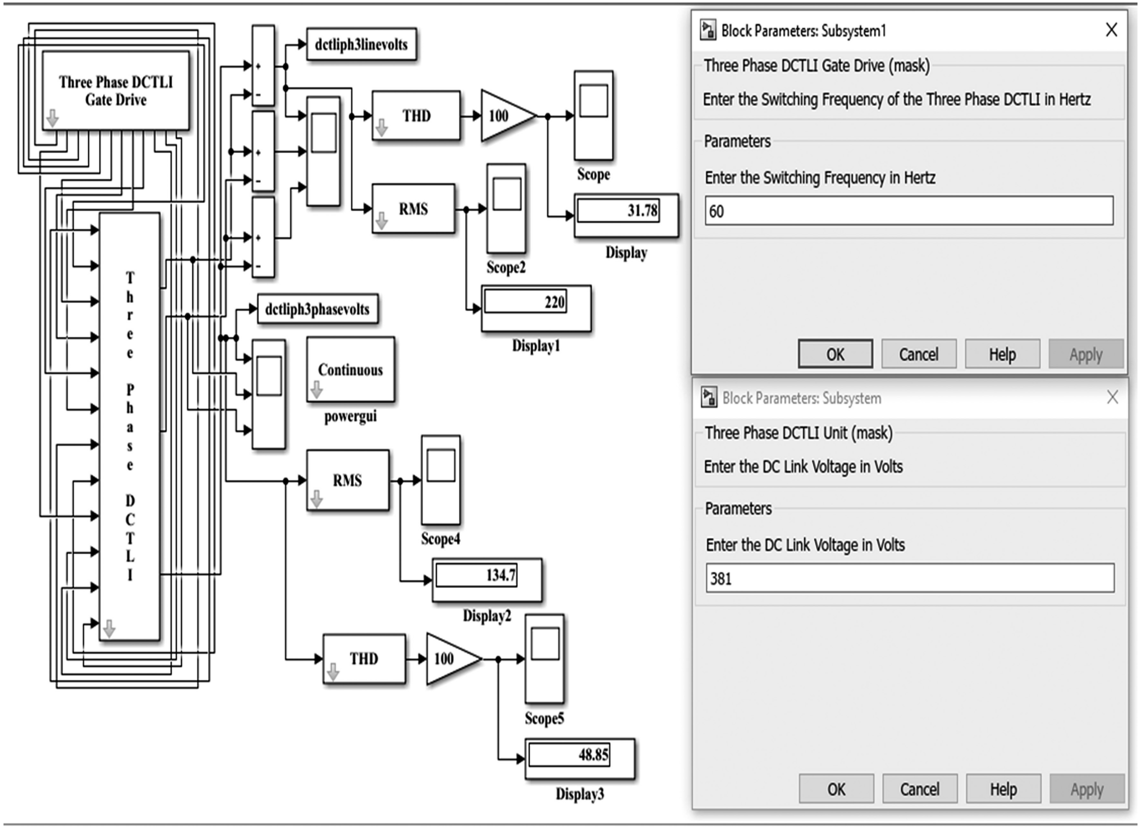
**FIGURE 9.3**
Three-phase DCTLI model.

gate pulse Q1 is HIGH (logic 1) for three entries and LOW (logic 0) for nine entries. Hence, its duty cycle is 3/12 ((3 * π/6)/(12 * π/6)) or 0.25. The duty cycle for the remaining switches can be calculated similarly from Table 9.1.

Figure 9.5b corresponds to the dialogue box 'Three-Phase DCTLI Unit' in Figure 9.4. Here, the DC link voltage is entered in volts in the box provided. The model of the semiconductor switches shown in Figure 9.1 is implemented using threshold switches and summing blocks as shown in Figure 9.5b. The switches Q1, Q2, Q3 and Q4 in Phase R are implemented as per Table 9.1, according to the following modelling statement:

```
If (gate pulse for Q1 is HIGH AND Q2 is HIGH) then
                    Output $V_{rg} = +V_{dc}/2$
Else if (gate pulse for Q2 is HIGH AND Q3 is HIGH) then
                    Output $V_{rg} = 0$
Else if (gate pulse for Q3 is HIGH AND Q4 is HIGH) then
                    Output $V_{rg} = -V_{dc}/2$
                    End if
```

Similar modelling statements hold good for switches in Phases Y and B. The AND gate is implemented using a threshold switch, as shown in


Three Phase DCTLI Gate Drive
Three Phase DCTLI
dctliph3linevolts
dctliph3phasevolts
THD
100
Scope
31.78
Display
RMS
Scope2
220
Display1
Continuous
powergui
RMS
Scope4
134.7
Display2
THD
100
Scope5
48.85
Display3
OK
Cancel
Help
Apply
OK
Cancel
Help
Apply

Block Parameters: Subsystem1

Three Phase DCTLI Gate Drive (mask)

Enter the Switching Frequency of the Three Phase DCTLI in Hertz

Parameters

Enter the Switching Frequency in Hertz: 60

Block Parameters: Subsystem

Three Phase DCTLI Unit (mask)

Enter the DC Link Voltage in Volts

Parameters

Enter the DC Link Voltage in Volts: 381

**FIGURE 9.4**
Three-phase DCTLI model with interactive blocks.

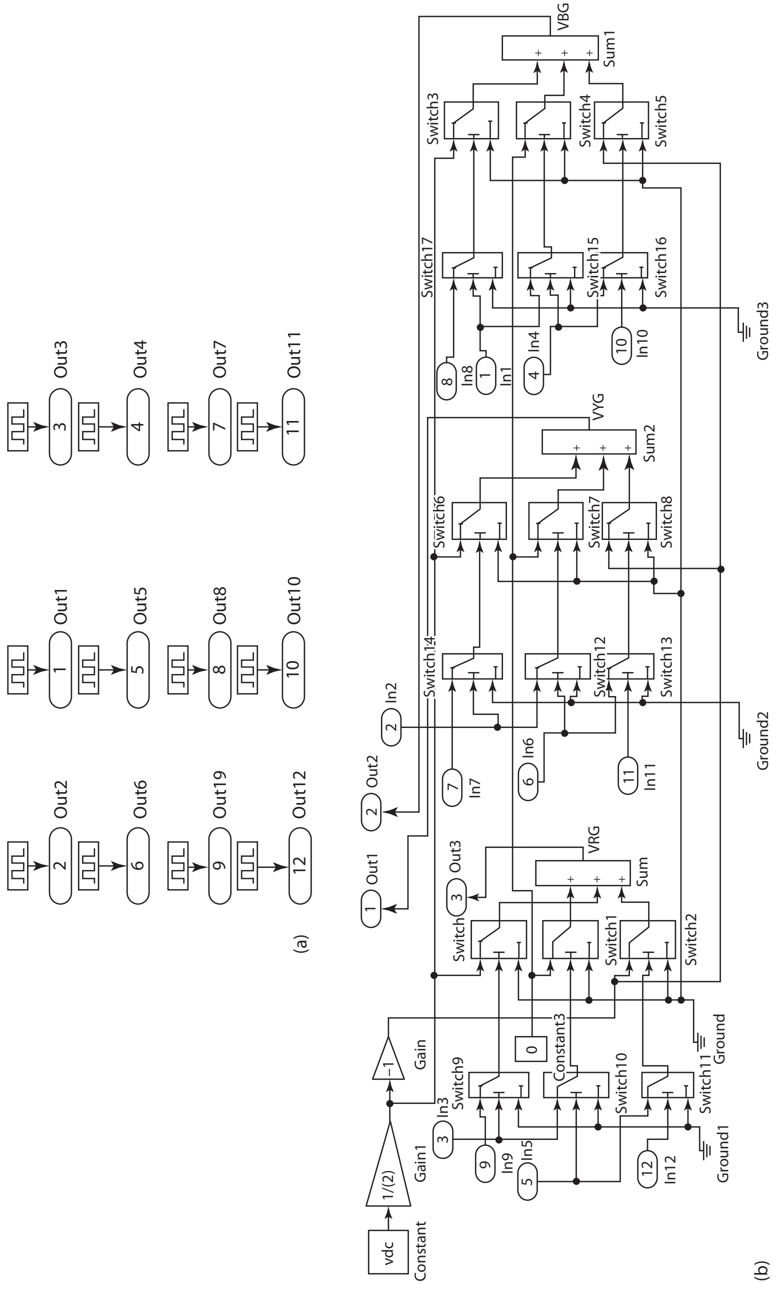
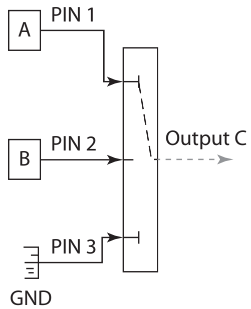

2
Out2
6
Out6
9
Out19
12
Out12
1
Out1
5
Out5
8
Out8
10
Out10
3
Out3
4
Out4
7
Out7
11
Out11
(a)
vdc
Constant
1/(2)
Gain1
−1
Gain
1
Out1
2
Out2
3
Out3
3
In3
9
In9
5
In5
12
In12
Switch9
Switch10
Switch11
Ground1
0
Constant3
Switch
Switch1
Switch2
Ground
Sum
VRG
2
In2
7
In7
6
In6
11
In11
Switch14
Switch12
Switch13
Ground2
Switch6
Switch7
Switch8
Sum2
VYG
8
In8
1
In1
4
In4
10
In10
Switch17
Switch15
Switch16
Ground3
Switch3
Switch4
Switch5
Sum1
VBG
(b)

**FIGURE 9.5.**
(a–c) Three-phase DCTLI model subsystems.



Threshold - 0.5

Criteria for passing first input u(2) >= 0.5

(c)

**FIGURE 9.5.** **(CONTINUED)**

**TABLE 9.1**

Switching Table for Three-Phase DCTLI

| Q1 | Q2 | Q3 | Q4 | $V_{rg}$ | Remarks |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | Phase R start |
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | |
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | |
| 0 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 0 | 0 | Phase B start |
| 0 | 1 | 1 | 0 | 0 | |
| 0 | 0 | 1 | 1 | $-V_{dc}/2$ | |
| 0 | 0 | 1 | 1 | $-V_{dc}/2$ | |
| 0 | 0 | 1 | 1 | $-V_{dc}/2$ | Phase Y start |
| 0 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | Phase R start for next cycle |

**TABLE 9.2**

Three-Phase DCTLI: Gate Pulse Phase Delay

| Sl. No. | Switch Phase R | Phase Delay (s) | Switch Phase Y | Phase Delay (s) | Switch Phase B | Phase Delay (s) |
|---|---|---|---|---|---|---|
| 1 | Q1 | 0 | Q5 | 4/(12.fsw) | Q9 | 8/(12.fsw) |
| 2 | Q2 | 9/(12.fsw) | Q6 | 1/(12.fsw) | Q10 | 5/(12.fsw) |
| 3 | Q3 | 3/(12.fsw) | Q7 | 7/(12.fsw) | Q11 | 11/(12.fsw) |
| 4 | Q4 | 6/(12.fsw) | Q8 | 10/(12.fsw) | Q12 | 2/(12.fsw) |

Figure 9.5c. In Figure 9.5c, the $u(1)$ and $u(2)$ are the inputs A and B with a value of either logic 0 or 1. The $u(3)$ input is the ground or logic 0. The threshold value of the switch is 0.5. When $u(2)$ is greater than or equal to the threshold value, the output corresponds to the $u(1)$ input, else the output is the $u(3)$ input. Thus, Figure 9.5c implements the AND gate. This AND gate principle is used in Figure 9.5b. Referring to the threshold switches from top to bottom on the extreme left of Figure 9.5b, the top switch marked Switch9 performs the AND operation of the gate pulse for Q1 and Q2, the middle switch marked Switch10 performs the AND operation of the gate pulse for Q2 and Q3 and the bottom switch marked Switch11 performs the AND operation of the gate pulse for Q3 and Q4. The top, middle and bottom switch outputs on the extreme left are passed to the $u(2)$ inputs of the second column of the top, middle and bottom switches marked Switch, Switch1 and Switch2, respectively. The $u(1)$ inputs of Switch, Switch1 and Switch2 in the second column are $+V_{dc}/2$, zero and $-V_{dc}/2$, respectively, while their $u(3)$ inputs are all zeros. All these switches have a threshold value of 0.5 and output $u(1)$ when the $u(2)$ input is greater than or equal to the threshold value, else the output is the $u(3)$ input and performs the modelling statement given. The output of the second column of switches marked Switch, Switch1 and Switch2 are added in a summing block to phase-to-ground output voltage $V_{rg}$. The switches for Phases Y and B are developed in the same way.

### 9.2.2 Simulation Results

The simulation results of the line-to-line voltage, line-to-ground voltage, root mean square (RMS) value of the line-to-line and line-to-ground voltages and their total harmonic distortion (THD) are shown in Figure 9.6 for a three-phase 60 Hz DCTLI using the ode23t (mod. stiff/trapezoidal) solver [9]. The DC link voltage is 381 V. The harmonic spectrum of the line-to-line voltages is shown in Figure 9.7a,b, respectively. Simulation results are tabulated in Table 9.3.

## 9.3 Three-Phase Flying-Capacitor Three-Level Inverter

The circuit schematic of the three-phase 50 Hz FCTLI is shown in Figure 9.8 using Microcap11 software [1–6,7]. There are four switches per phase, two at the top leg and two at the bottom leg. The capacitor connecting the switches in each of the three phases is called the *flying capacitor.* The two capacitors at the input act as a potential divider. The DC link voltage is $2V_{dc}$ V. The simulation results for the three-phase line-to-ground and line-to-line voltages are shown in Figure 9.9. As can be seen from Figure 9.9, the line-to-ground voltage has three voltage levels and the line-to-line voltage has five voltage levels, and there are 12 gate pulses, that is, semiconductor switches.

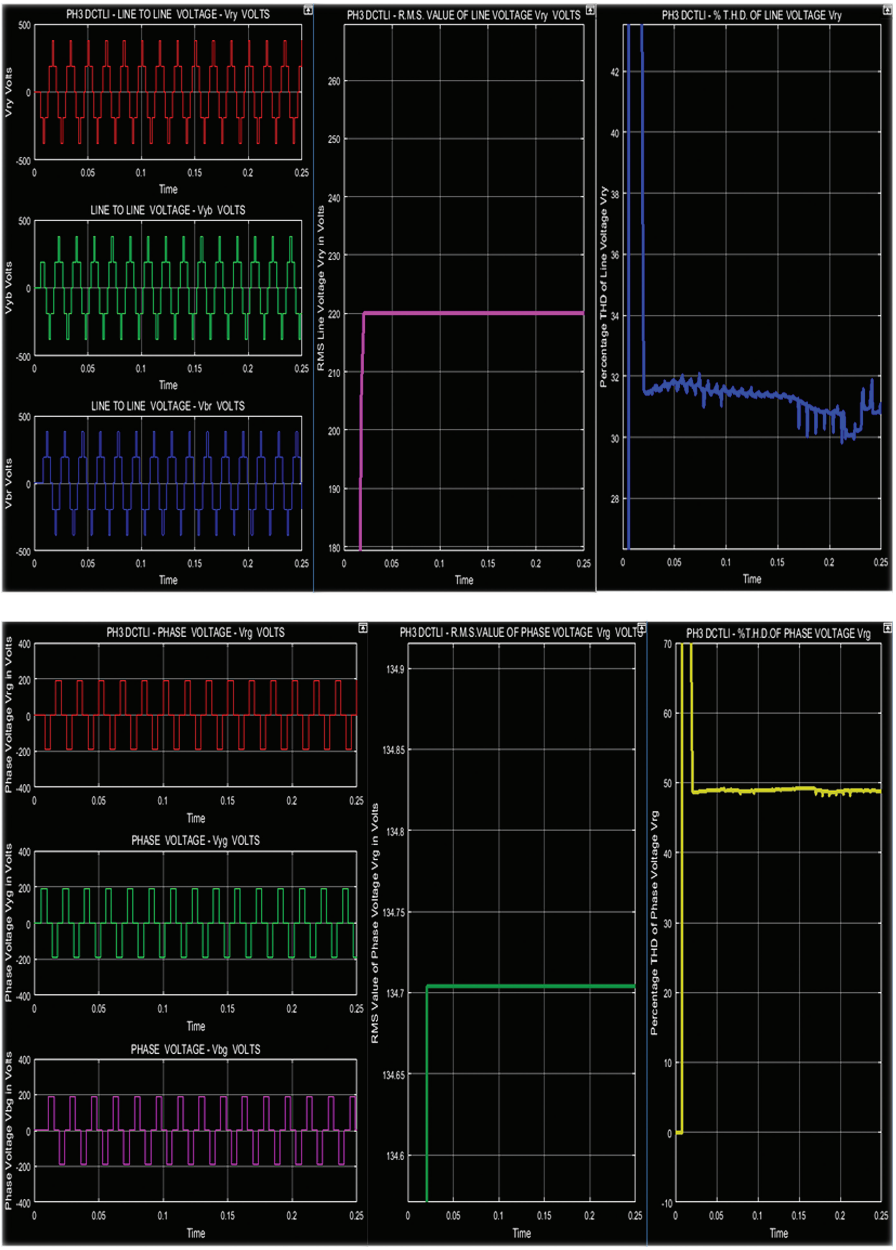
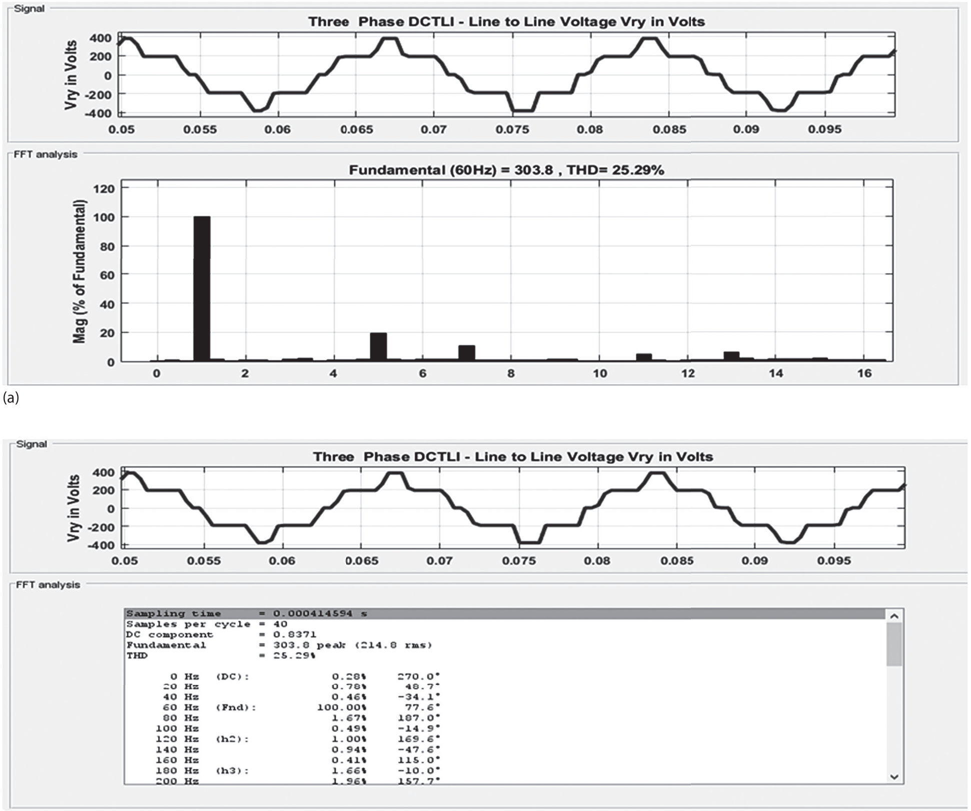


**FIGURE 9.6**
Three-phase DCTLI simulation results.


Signal
Three Phase DCTLI - Line to Line Voltage Vry in Volts
Vry in Volts
400
200
0
-200
-400
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
FFT analysis
Fundamental (60Hz) = 303.8 , THD= 25.29%
Mag (% of Fundamental)
120
100
80
60
40
20
0
0
2
4
6
8
10
12
14
16

(a)

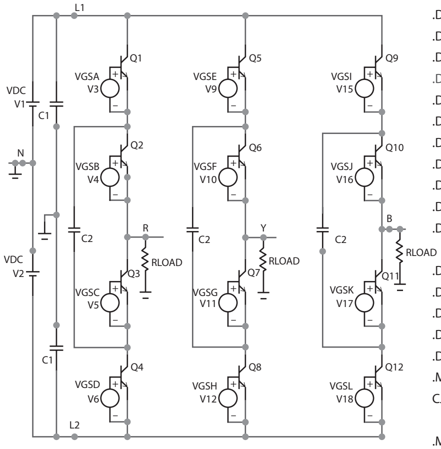
```
Sampling time      = 0.000414594 s
Samples per cycle  = 40
DC component       = 0.8371
Fundamental        = 303.8 peak (214.8 rms)
THD                = 25.29%

      0 Hz  (DC):           0.28%    270.0°
     20 Hz                  0.78%     48.7°
     40 Hz                  0.46%    -34.1°
     60 Hz  (Fnd):        100.00%     77.6°
     80 Hz                  1.67%    187.0°
    100 Hz                  0.49%    -14.9°
    120 Hz  (h2):           1.00%    169.6°
    140 Hz                  0.94%    -47.6°
    160 Hz                  0.41%    115.0°
    180 Hz  (h3):           1.66%    -10.0°
    200 Hz                  1.96%    157.7°
```

(b)

**FIGURE 9.7**
(a and b) Harmonic spectrum of line-to-line voltage.

**TABLE 9.3**
Three-Phase DCTLI: Simulation Results

| Sl. No. | DC Link Voltage (V) | Frequency (Hz) | $V_{LL}$ RMS (V) | $V_{LL}$ THD (%) | $V_{LG}$ RMS (V) | $V_{LG}$ THD (%) |
|---|---|---|---|---|---|---|
| 1 | 381 | 60 | 220 | 30.82 | 134.7 | 48.84 |


L1
Q1
Q5
Q9
VGSA
V3
VGSE
V9
VGSI
V15
VDC
V1
C1
N
Q2
Q6
Q10
VGSB
V4
VGSF
V10
VGSJ
V16
B
R
Y
C2
C2
C2
RLOAD
RLOAD
RLOAD
VDC
V2
Q3
Q7
Q11
VGSC
V5
VGSG
V11
VGSK
V17
C1
Q4
Q8
Q12
VGSD
V6
VGSH
V12
VGSL
V18
L2

```
.DEFINE VDC 190.5
.DEFINE C1 0.1E-12
.DEFINE C2 1.2e-7
.DEFINE RLOAD 500
.DEFINE VGSA PULSE (0  5  15M  0M  0M  15M  20M)
.DEFINE VGSB PULSE (0  5  0M  0M  0M  5M  20M)
.DEFINE VGSC PULSE (0  5  5M  0M  0M  15M  20M)
.DEFINE VGSD PULSE (0  5  10M  0M  0M  5M  20M)
.DEFINE VGSE PULSE (0  5  1.667M 0M  0M  15M  20M)
.DEFINE VGSF PULSE (0  5  6.667M  0M  0M  5M  20M)
.DEFINE VGSG PULSE (0  5  11.667M  0M  0M  15M  20M)

.DEFINE VGSH PULSE (0  5  16.667M  0M 0M  5M  20M)
.DEFINE VGSI PULSE (0  5  8.333M  0M  0M  15M  20M)
.DEFINE VGSJ PULSE (0  5  13.333M  0M  0M  5M  20M)
.DEFINE VGSK PULSE (0  5  18.333M  0M  0M  15M  20M)
.DEFINE VGSL PULSE (0  5  3.333M  0M  0M  5M  20M)
.MODEL D1N4148 D (IS=5.95862N N=1.91266 BV=500 RS=589.498M TT=1.12599N
CJO=1.33941P VJ=8.66264 M=300M RL=3.14968G)

.MODEL 2N2222 NPN (IS=10.017F BF=506.842 NF=979.99M VAF=100 IKF=696.241M
ISE=0.241303F NE=1.05779 BR=154.978M IKR=999.407 ISC=6.94996P RE=668.817M
CJE=42.4239P VJE=700M MJE=642.887M CJC=36.6437P VJC=700M MJC=558.066M
TF=484.887P XTF=500.001M VTF=10 ITF=9.88166M TR=2.26629U)
```

**FIGURE 9.8**
Three-phase FCTLI.

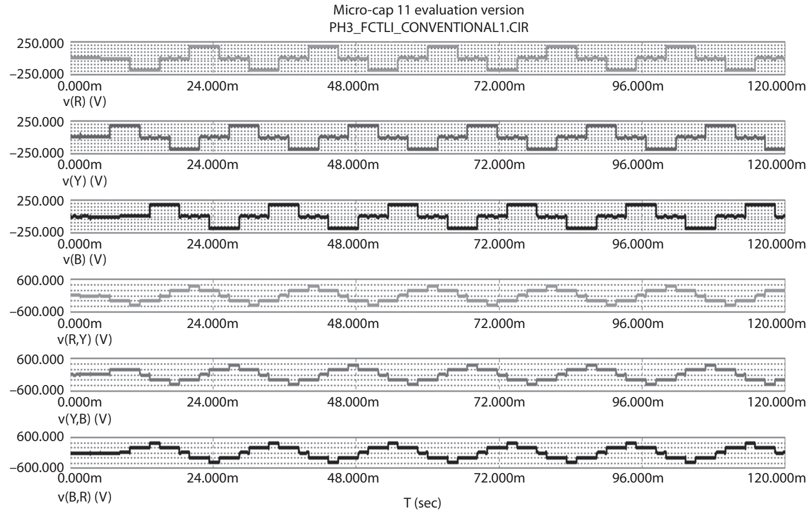


**FIGURE 9.9**
Three-phase FCTLI: output voltage waveforms.

### 9.3.1 Modelling of Three-Phase Flying-Capacitor Three-Level Inverter

The model of the three-phase FCTLI is shown in Figure 9.10 [8]. The FCTLI model, with an interactive dialogue box, is shown in Figure 9.11. The subsystem is shown in Figure 9.12. A brief description of the subsystem is given as follows:

Figure 9.11 corresponds to the dialogue box 'Three-Phase FCTLI and Gate Drive Unit' shown in Figure 9.12. The DC link voltage in volts and the switching frequency of the inverter in hertz are entered in the boxes provided. The outputs of the gate drives marked from Q1 to Q12 in Figure 9.12 correspond to the switches Q1 to Q12 in Figure 9.8. The switching table for the switches Q1, Q2, Q3 and Q4 in Phase R is shown in Table 9.4. The same table can be used for switches in Phases Y and B by replacing Q1 to Q4 by

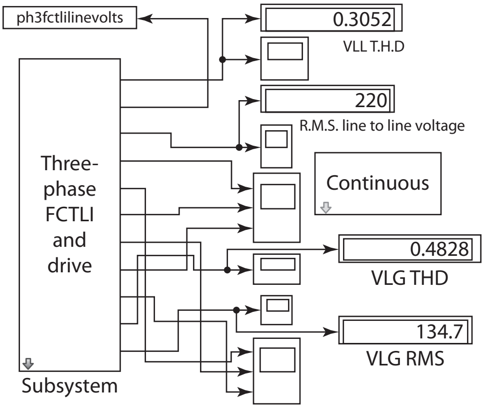
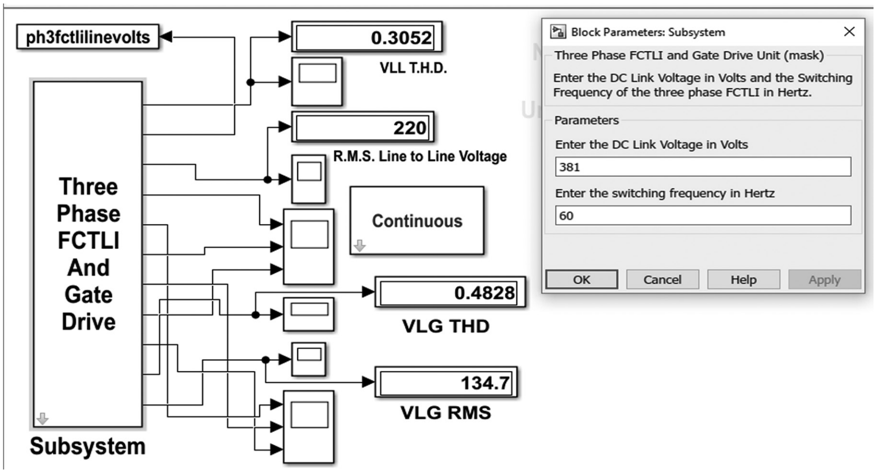

ph3fctlilinevolts
0.3052
VLL T.H.D
220
R.M.S. line to line voltage
Three-phase FCTLI and drive
Continuous
0.4828
VLG THD
134.7
VLG RMS
Subsystem

**FIGURE 9.10**
Three-phase FCTLI model.


ph3fctlilinevolts
0.3052
VLL T.H.D.
220
R.M.S. Line to Line Voltage
Three Phase FCTLI And Gate Drive
Continuous
0.4828
VLG THD
134.7
VLG RMS
Subsystem

Block Parameters: Subsystem

Three Phase FCTLI and Gate Drive Unit (mask)

Enter the DC Link Voltage in Volts and the Switching Frequency of the three phase FCTLI in Hertz.

Parameters

Enter the DC Link Voltage in Volts: 381

Enter the switching frequency in Hertz: 60

OK
Cancel
Help
Apply

**FIGURE 9.11**
Three-phase FCTLI model with interactive blocks.

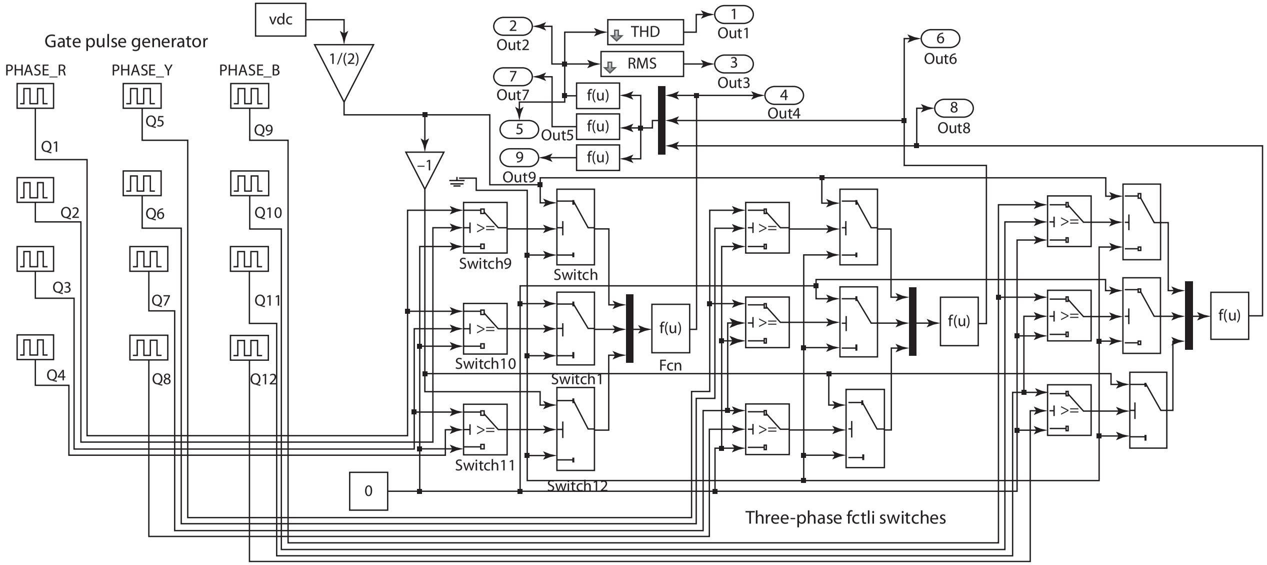

Gate pulse generator
PHASE_R
PHASE_Y
PHASE_B
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
vdc
1/(2)
–1
0
Switch9
Switch10
Switch11
Switch
Switch1
Switch12
Fcn
f(u)
THD
RMS
1
Out1
2
Out2
3
Out3
4
Out4
5
Out5
6
Out6
7
Out7
8
Out8
9
Out9
Three-phase fctli switches

**FIGURE 9.12**
Three-phase FCTLI model subsytem.

Q5 to Q8 or Q9 to Q12 in respective order. The start point of the appropriate phases may be noted from the remarks column of Table 9.4. If *d* is the time delay between any two neighbouring or consecutive states in Table 9.4, then this delay *d* is π/6 rad. Table 9.4 is implemented as shown in Figure 9.12 using Pulse Generator blocks, marked 'Gate Pulse Generator' in Figure 9.12. The amplitude of all the pulses in all the Pulse Generator blocks is set to 1 and the period is set to (1/fsw), where fsw is the switching frequency of the inverter. The phase delay for each of the switches in Phases R, Y and B is tabulated in Table 9.5. In Table 9.4, gate pulse Q1 is HIGH (logic 1) for nine entries and LOW (logic 0) for three entries. Hence, its duty cycle is 9/12 ((9 * π/6)/(12 * π/6)) or 0.75. The duty cycle for the remaining switches can be calculated in the same way from Table 9.4. Switch names are shown in Figure 9.8.

Three-phase FCTLI switches are implemented using threshold switches and summing Fcn blocks, as shown in Figure 9.12. The switches Q1 to Q4 in Phase R are implemented as per Table 9.4, according to the following modelling statement:

**TABLE 9.4**

Switching Table for Three-Phase FCTLI

| Q1 | Q2 | Q3 | Q4 | *V*rg | Remarks |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | Phase R start |
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | |
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | |
| 1 | 0 | 1 | 0 | 0 | |
| 1 | 0 | 1 | 0 | 0 | Phase B start |
| 1 | 0 | 1 | 0 | 0 | |
| 0 | 0 | 1 | 1 | $-V_{dc}/2$ | |
| 0 | 0 | 1 | 1 | $-V_{dc}/2$ | |
| 0 | 0 | 1 | 1 | $-V_{dc}/2$ | Phase Y start |
| 1 | 0 | 1 | 0 | 0 | |
| 1 | 0 | 1 | 0 | 0 | |
| 1 | 0 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 0 | $+V_{dc}/2$ | Phase R start for next cycle |

**TABLE 9.5**

Three-Phase FCTLI: Gate Pulse Phase Delay

| Sl.No. | Switch Phase R | Phase Delay (s) | Switch Phase Y | Phase Delay (s) | Switch Phase B | Phase Delay (s) |
|---|---|---|---|---|---|---|
| 1 | Q1 | 9/(12.fsw) | Q5 | 1/(12.fsw) | Q9 | 5/(12.fsw) |
| 2 | Q2 | 0 | Q6 | 4/(12.fsw) | Q10 | 8/(12.fsw) |
| 3 | Q3 | 3/(12.fsw) | Q7 | 7/(12.fsw) | Q11 | 11/(12.fsw) |
| 4 | Q4 | 6/(12.fsw) | Q8 | 10/(12.fsw) | Q12 | 2/(12.fsw) |

```
If (gate pulse for Q1 is HIGH AND Q2 is HIGH) then
                  Output $V_{rg} = +V_{dc}/2$
Else if (gate pulse for Q1 is HIGH AND Q3 is HIGH) then
                  Output $V_{rg} = 0$
Else if (gate pulse for Q3 is HIGH AND Q4 is HIGH) then
                  Output $V_{rg} = -V_{dc}/2$
                  End if
```

Similar modelling statements hold good for switches in Phases Y and B. The AND gate is implemented using the threshold switch as shown in Figure 9.5c, which has already been explained in Section 9.2.1. This AND gate principle is used for the three-phase FCTLI switches in Figure 9.12. Referring to the threshold switches from top to bottom on the extreme left of the position marked 'Three-Phase FCTLI Switches' in Figure 9.12, the top switch marked Switch9 performs the AND operation of the gate pulse for Q1 and Q2, the middle switch marked Switch10 performs the AND operation of the gate pulse for Q1 and Q3 and the bottom switch marked Switch11 performs the AND operation of the gate pulse for Q3 and Q4. The top, middle and bottom switch outputs on the extreme left are passed to the $u(2)$ inputs of the second column of the top, middle and bottom switches marked Switch, Switch1 and Switch2, respectively. The $u(1)$ input to the switches marked Switch, Switch1 and Switch2 in the second column are $+V_{dc}/2$, zero and $-V_{dc}/2$, respectively, while their $u(3)$ inputs are all zeros. All these switches have a threshold value of 0.5 and output $u(1)$ when the $u(2)$ input is greater than or equal to the threshold value, else the output is the $u(3)$ input and performs the modelling statement given. The output of the switches marked Switch, Switch1 and Switch2 are added in a function block marked Fcn whose output is the line-to-ground voltage $V_{rg}$. The switches for Phases Y and B are developed in the same way.

### 9.3.2 Simulation Results

The simulation results of the line-to-line voltage, line-to-ground voltage, RMS value of the line-to-line voltage and its THD are shown in Figure 9.13 for a three-phase 60 Hz FCTLI using the ode23t (mod. stiff/trapezoidal) solver [9]. The DC link voltage is 381 V. The harmonic spectrum of the line-to-line voltage is shown in Figure 9.14a and b, respectively. Simulation results are tabulated in Table 9.6.

## 9.4 Three-Phase Cascaded H-Bridge Inverter

A three-phase symmetrical five-level cascade H-bridge (CHB) inverter is shown in Figure 9.15 [10–11]. In each phase, there are two H-bridge inverter cells connected in cascade. A separate DC voltage source is connected for each H-bridge, having a value $V_{dc}$. The total output voltage of each phase is

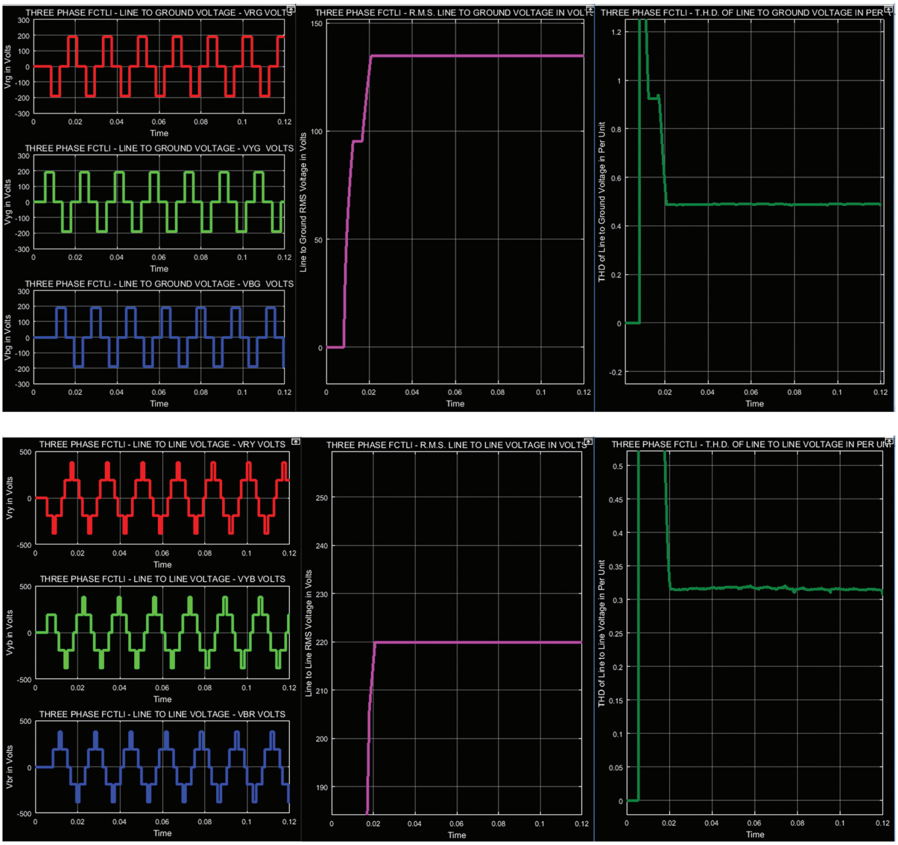


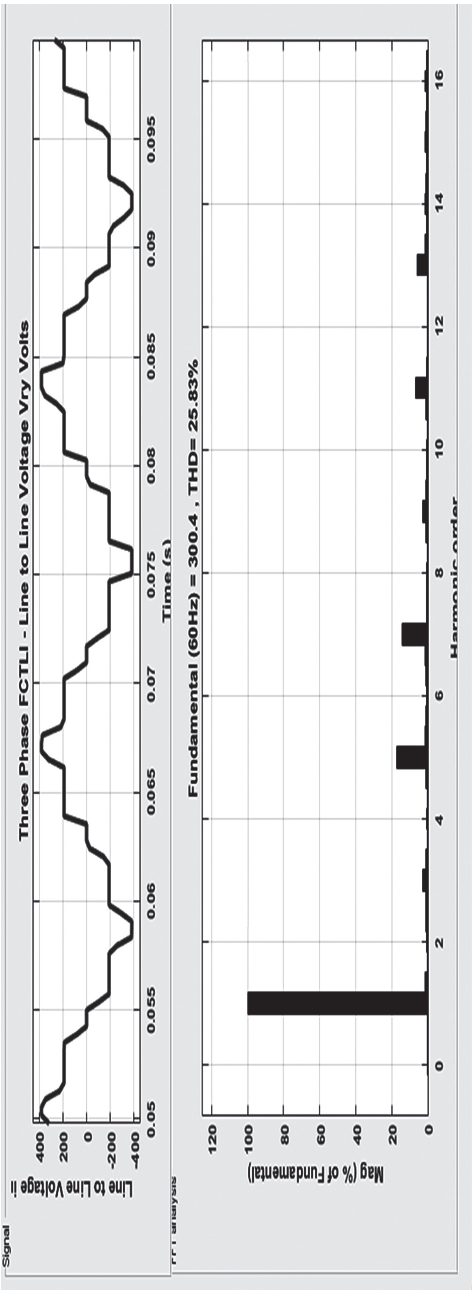
**FIGURE 9.13**
Three-phase FCTLI simulation results.

the algebraic sum of the voltages across each H-bridge inverter cell. Referring to Phase A, the output voltage $v_A$ can be expressed as follows:

$$v_A = \sum_{i=1,2} v_{ai} \tag{9.1}$$

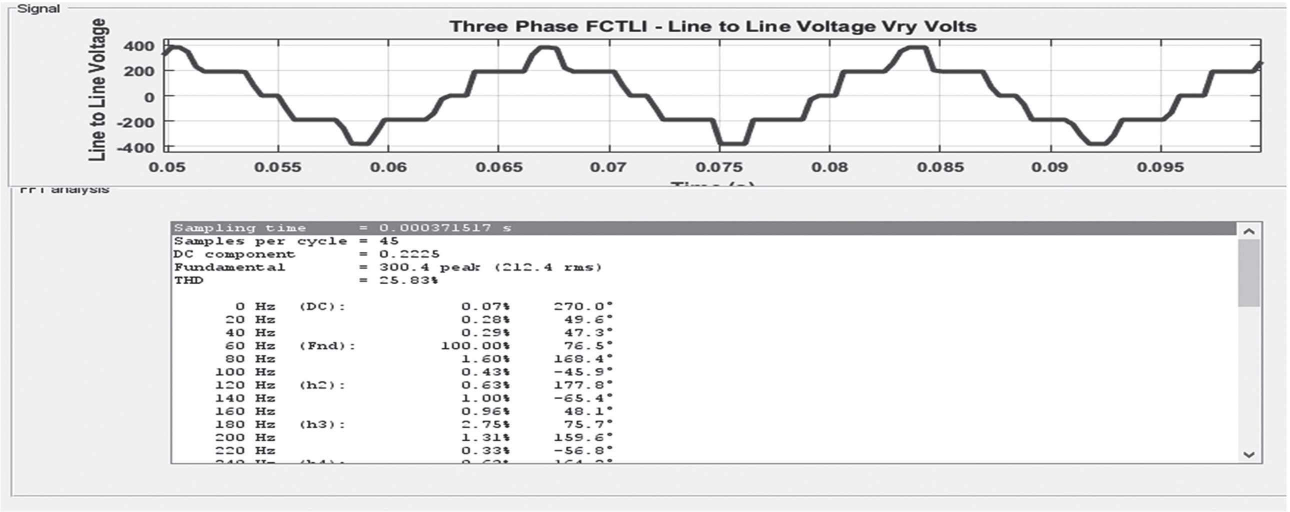
Separate DC voltage sources with unequal values can also be connected to each H-bridge inverter cell. Any number of H-bridge inverter units can be cascaded to obtain the required output voltage value, and the output voltage level also increases. Each semiconductor switch in the cascaded H-bridge must be provided with a separate gate drive unit; this makes the design complex. The CHB inverter finds applications in ASDs, electric traction, electric vehicles, battery charging, renewable energy interface, active filter reactive power compensation, flexible AC transmission systems and high-voltage DC (HVDC) transmission.

Referring to the upper H-bridge in Phase A of Figure 9.15, it is seen that the output voltage $v_{a2}$ takes values of $+V_{dc}$ when switches S1A and S4A are ON,


Signal
Three Phase FCTLI - Line to Line Voltage Vry Volts
Line to Line Voltage i
400
200
0
-200
-400
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
Time (s)
FFT analysis
Fundamental (60Hz) = 300.4 , THD= 25.83%
Mag (% of Fundamental)
120
100
80
60
40
20
0
0
2
4
6
8
10
12
14
16
Harmonic order

(a)

**FIGURE 9.14**
(a,b) Three-phase FCTLI – harmonic spectrum of line-to-line voltage $V_{ry}$.


Signal
Three Phase FCTLI - Line to Line Voltage Vry Volts
Line to Line Voltage
400
200
0
-200
-400
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
FFT analysis

```
Sampling time      = 0.000371517 s
Samples per cycle  = 45
DC component       = 0.2225
Fundamental        = 300.4 peak (212.4 rms)
THD                = 25.83%

      0 Hz  (DC):          0.07%    270.0°
     20 Hz                 0.28%     49.6°
     40 Hz                 0.29%     47.3°
     60 Hz  (Fnd):       100.00%     76.5°
     80 Hz                 1.60%    168.4°
    100 Hz                 0.43%    -45.9°
    120 Hz  (h2):          0.63%    177.8°
    140 Hz                 1.00%    -65.4°
    160 Hz                 0.96%     48.1°
    180 Hz  (h3):          2.75%     75.7°
    200 Hz                 1.31%    159.6°
    220 Hz                 0.33%    -56.8°
```

(b)

**FIGURE 9.14**
Three-phase FCTLI. (b) Harmonic spectrum of line-to-line voltage.

**TABLE 9.6**

Three-Phase FCTLI: Simulation Results

| Sl. No. | DC Link Voltage (V) | Frequency (Hz) | $V_{LL}$ RMS (V) | $V_{LL}$ THD % | $V_{LG}$ RMS (V) | $V_{LG}$ THD % |
|---|---|---|---|---|---|---|
| 1 | 381 | 60 | 220 | 30.52 | 134.7 | 48.28 |

zero when either S1A and S3A are ON or when S2A and S4A are ON, and $-V_{dc}$ when S2A and S3A are ON. Similar logic holds good for output voltage $v_{a1}$ in the lower H-bridge. Thus, the output phase-to-ground voltage $v_A$ takes values $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$, respectively, giving a five-level voltage. The complete truth table for Phase A of Figure 9.15 is shown in Table 9.7. A similar table is applicable to Phases B and C with switches S1A to S8A replaced by S1B to S8B and S1C to S8C, respectively. The $v_A$ column is replaced by $v_B$ and $v_C$ and the initial phase spread in the 'Remarks' column corresponding to serial no. 1 for phase B starts at 120–165° and that for phase C starts at 240–285°.

The model and simulation of a single-phase five-level cascaded H-bridge inverter using PSIM is shown in Figure 9.16a–c. The gate pulses are derived using Table 9.7. The DC voltage source for each H-bridge is 100 V and the switching frequency is 50 Hz. A series-connected R–L load of 50 Ω and 0.5 H is used. The RMS value of the phase-to-ground voltage is found to be 122.469 V by simulation.

### 9.4.1 Modelling of Three-Phase Five-Level Cascaded H-Bridge Inverter

The model of the three-phase five-level cascaded H-bridge inverter (TPFLCHBI) is shown in Figure 9.17 with interactive dialogue boxes. The various subsystems are shown in Figure 9.18a–c. A brief description of the various subsystems are given here:

Figure 9.18a corresponds to the dialogue box 'TPCHB Inverter Gate Pulse Generator' shown in Figure 9.17. The switching period of the inverter in seconds is entered in the box provided. The switches S1A to S8A in Phase A, S1B to S8B in Phase B and S1C to S8C in Phase C are marked with their respective outputs. The dialogue box for switch S1A in Phase A is also shown in Figure 9.18a. Referring to Table 9.7, it is seen that neighbouring or consecutive entries differ by a phase delay *d*, which is 45° (π/4 rad) or *T*/8 s, where *T* is the inverter switching period. Referring to the switch S1A column in Table 9.7, it is seen that there are three '1' (ON) and five '0' (OFF) states. Thus, the duty cycle of the gate pulse for S1A is $(3*\pi/4)/(8*\pi/4)$, which is 3/8 or 300/8 per cent. The duty cycle of the gate pulse for the remaining switches can be calculated in the same way. Also, the gate pulse for S1A goes ON (logic 1) at 315° and remains ON until 450°. This gate pulse phase delay is $7*T/8$ s. Pulse amplitude logic 1 means HIGH. These values are entered in the dialogue box for S1A in Figure 9.18a. The phase delay for the gate pulse of the remaining switches are calculated in the same way and are tabulated in Table 9.8.

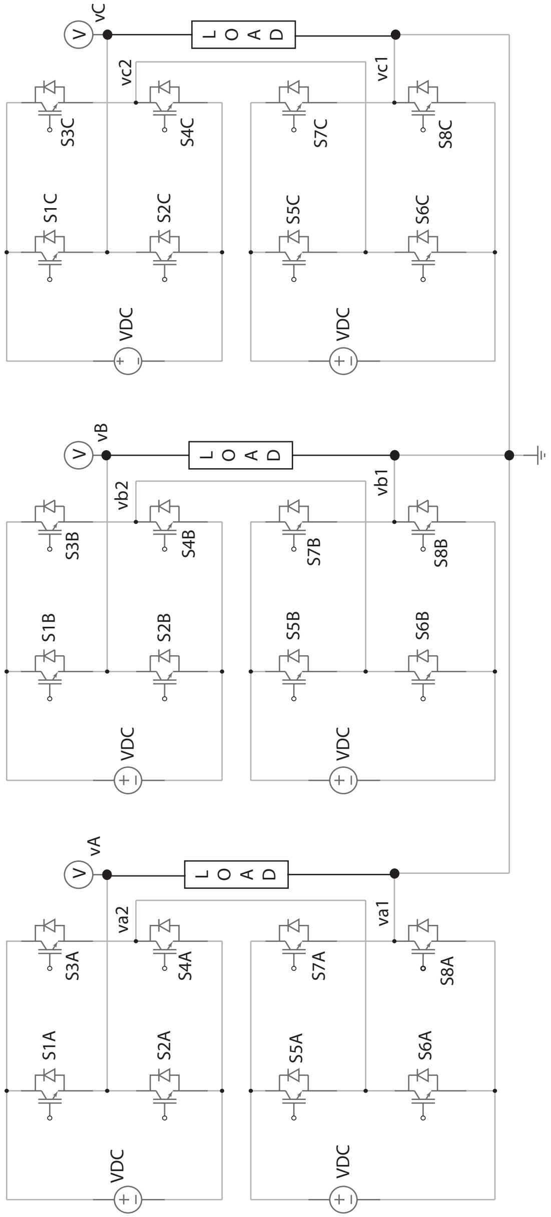

V
vA
vB
vC
LOAD
va1
va2
vb1
vb2
vc1
vc2
S1A
S2A
S3A
S4A
S5A
S6A
S7A
S8A
S1B
S2B
S3B
S4B
S5B
S6B
S7B
S8B
S1C
S2C
S3C
S4C
S5C
S6C
S7C
S8C
VDC
+
−

**FIGURE 9.15**
Three-phase CHB five-level inverter.

**TABLE 9.7**

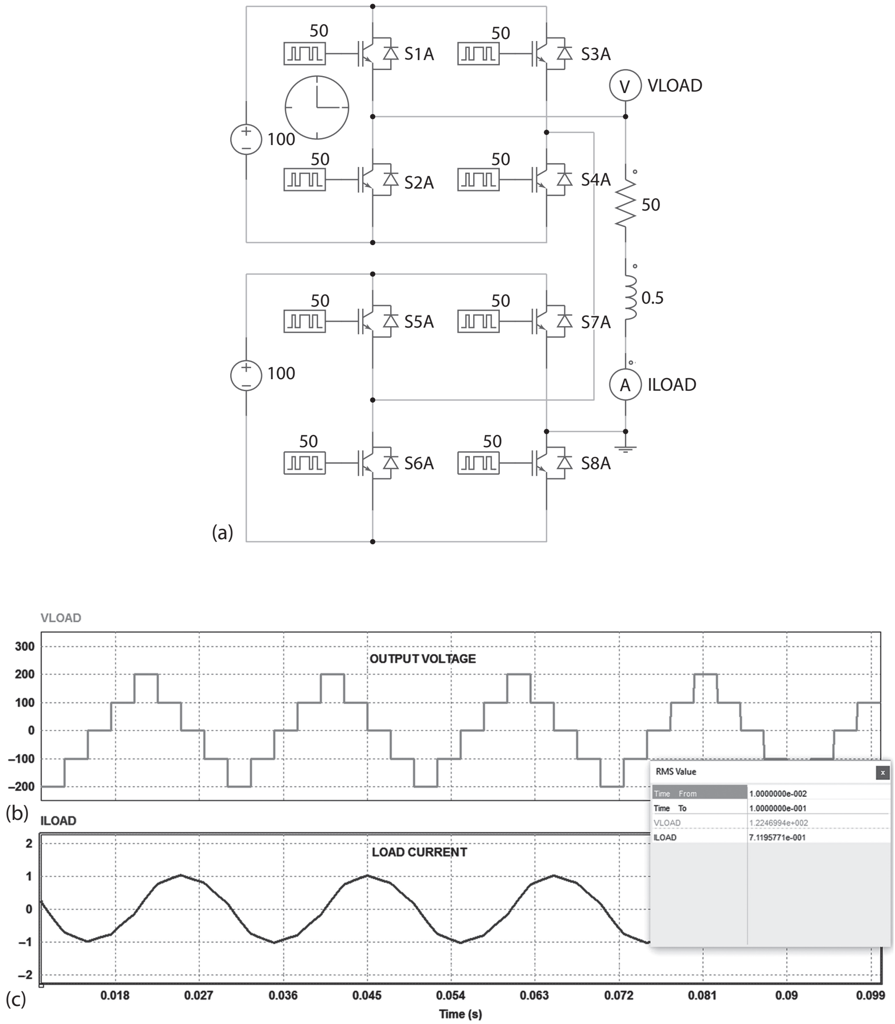
Truth Table: Three-Phase CHB Inverter

| Sl. No. | S1A | S2A | S3A | S4A | S5A | S6A | S7A | S8A | $v_A$ (V) | Remarks 1 ON; 0 OFF |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $+2V_{dc}$ | 0°–45° |
| 2 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $+V_{dc}$ | 45°–90° |
| 3 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 90°–135° |
| 4 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | $-V_{dc}$ | 135°–180° |
| 5 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | $-2V_{dc}$ | 180°–225° |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | $-V_{dc}$ | 225°–270° |
| 7 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 270°–315° |
| 8 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $+V_{dc}$ | 315°–360° |
| 9 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $+2V_{dc}$ | Next cycle |

Figure 9.18b corresponds to the dialogue box ‘TPCHB Inverter Model Switches’ in Figure 9.17. Here, the DC link voltage for the upper or lower H-bridge is entered in volts and the switching frequency in hertz in the box provided. The model of the semiconductor switches shown in Figure 9.15 is implemented using threshold switches and summing blocks as shown in Figure 9.18b. The switches S1A to S8A in Phase A are implemented as per Table 9.7, according to the following modelling statement:

```
If (gate pulses for S1A AND S4A AND S5A AND S8A are HIGH) then
                         Output $V_{Ag} = +2 * V_{dc}$
Else if (gate pulses for S1A AND S4A AND S6A AND S8A are HIGH) then
                         Output $V_{Ag} = +V_{dc}$
Else if (gate pulses for S2A AND S4A AND S6A AND S8A are HIGH) then
                         Output $V_{Ag} = 0$
Else if (gate pulses for S2A AND S3A AND S6A AND S8A are HIGH) then
                         Output $V_{Ag} = -V_{dc}$
Else if (gate pulses for S2A AND S3A AND S6A AND S7A are HIGH) then
                         Output $V_{Ag} = -2 * V_{dc}$
                         End if
```

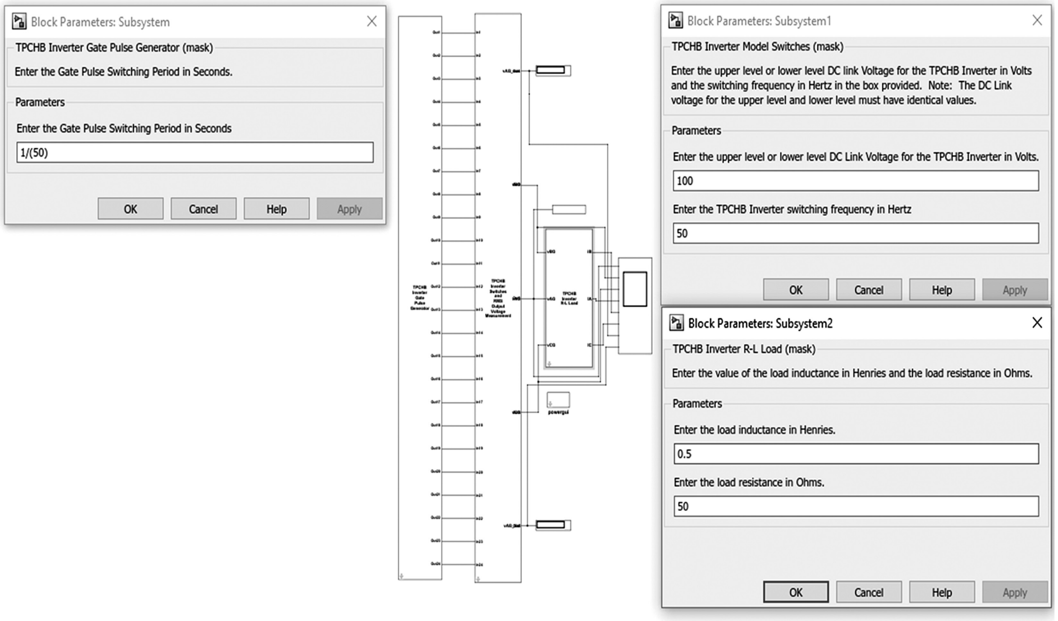
Similar modelling statements hold good for switches in Phases B and C. The AND gate is implemented using a threshold switch as shown in Figure 9.5c. This is explained in Section 9.2.1. This AND gate principle is used in Figure 9.18b. Referring to threshold switches from top to bottom on the extreme left of Figure 9.18b corresponding to Phase A, the top switch marked Switch1 performs the AND operation of the gate pulse for S1A and S2A, the switch marked Switch2 performs the AND operation of the gate pulse for S5A and S8A and Switch3 performs the AND operation of the output of Switch1 and Switch2. The output of Switch3 is passed to the *u*(2) input of Switch4, whose u(1) input is $+2{*}V_{dc}$ and *u*(3) input is zero. Switch1 to Switch4 have a threshold value of 0.5 and output the *u*(1) input when *u*(2) is greater than or equal to 0.5, else output zero value. Thus, when S1A, S4A, S5A and S8A only


50
S1A
50
S3A
V
VLOAD
100
50
S2A
50
S4A
50
50
S5A
50
S7A
0.5
100
A
ILOAD
50
S6A
50
S8A
(a)
VLOAD
300
200
100
0
−100
−200
OUTPUT VOLTAGE
(b)
ILOAD
2
1
0
−1
−2
LOAD CURRENT
(c)
0.018
0.027
0.036
0.045
0.054
0.063
0.072
0.081
0.09
0.099
Time (s)
RMS Value
×

| | |
|---|---|
| Time From | 1.0000000e-002 |
| Time To | 1.0000000e-001 |
| VLOAD | 1.2246994e+002 |
| ILOAD | 7.1195771e-001 |

**FIGURE 9.16**
(a) Single-phase five-level cascaded H-bridge inverter model. (b and c) Single-phase cascaded H-bridge five-level inverter: (b) output voltage; (c) load current.

are ON, the output of Switch4 $v_{Ag}$ is +2*$V_{dc}$ V. All other threshold switches in Phases A, B and C are identical to Switch1 to Switch4. Similarly, Switch5 to Switch8 output is +$V_{dc}$ V when switches S1A, S4A, S6A and S8A only are ON. When S2A, S4A, S6A and S8A only are ON, the output of Switch9 to Switch12 will be 0 V. Swich13 to Switch16 output is –$V_{dc}$ V when S2A, S3A, S6A and S8A only are ON. Finally, Switch17 to Switch20 output is –2*$V_{dc}$ V when S2A, S3A, S6A and S7A only are ON. The final output of the switches marked Switch4, Switch8, Switch12, Switch15 and Switch19 are passed to the Sum of Elements block to obtain the algebraic sum of the output of each of the four threshold



Block Parameters: Subsystem
OK
Cancel
Help
Apply
powergui
Block Parameters: Subsystem1
Block Parameters: Subsystem2

TPCHB Inverter Gate Pulse Generator (mask)

Enter the Gate Pulse Switching Period in Seconds.

Parameters

Enter the Gate Pulse Switching Period in Seconds: 1/(50)

TPCHB Inverter Model Switches (mask)

Enter the upper level or lower level DC link Voltage for the TPCHB Inverter in Volts and the switching frequency in Hertz in the box provided. Note: The DC Link voltage for the upper level and lower level must have identical values.

Parameters

Enter the upper level or lower level DC Link Voltage for the TPCHB Inverter in Volts: 100

Enter the TPCHB Inverter switching frequency in Hertz: 50

TPCHB Inverter R-L Load (mask)

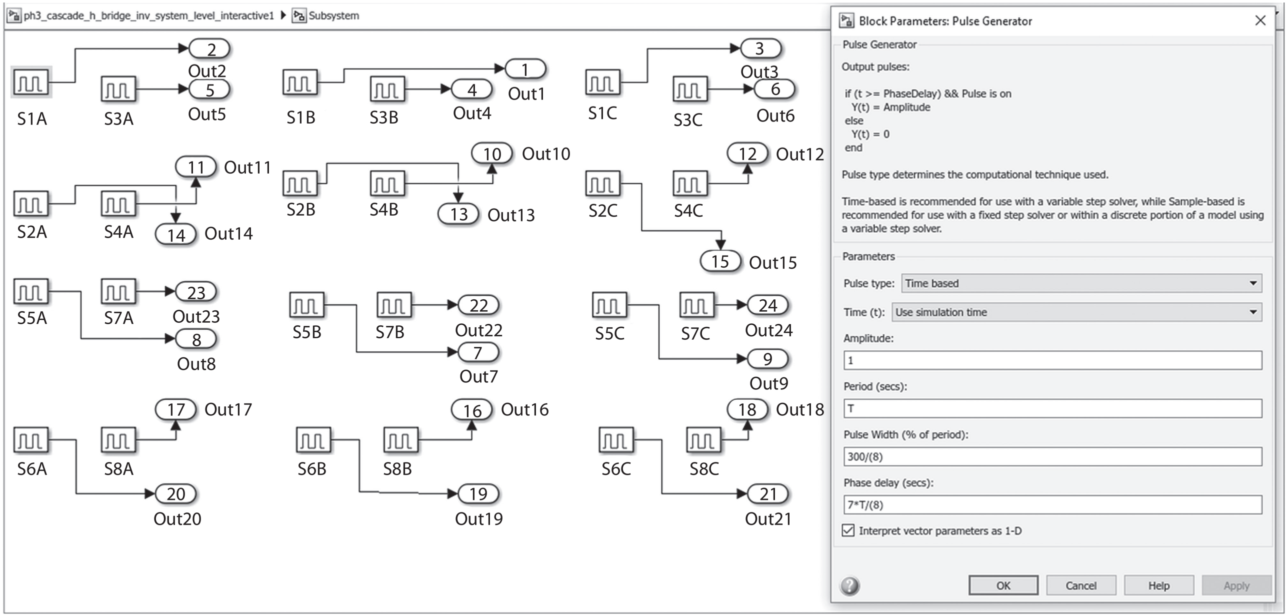
Enter the value of the load inductance in Henries and the load resistance in Ohms.

Parameters

Enter the load inductance in Henries: 0.5

Enter the load resistance in Ohms: 50

**FIGURE 9.17**
Model of three-phase five-level CHB inverter with interactive blocks.


ph3_cascade_h_bridge_inv_system_level_interactive1 ▸ Subsystem
S1A
S3A
2
Out2
5
Out5
S1B
S3B
1
Out1
4
Out4
S1C
S3C
3
Out3
6
Out6
S2A
S4A
11
Out11
14
Out14
S2B
S4B
10
Out10
13
Out13
S2C
S4C
12
Out12
15
Out15
S5A
S7A
23
Out23
8
Out8
S5B
S7B
22
Out22
7
Out7
S5C
S7C
24
Out24
9
Out9
S6A
S8A
17
Out17
20
Out20
S6B
S8B
16
Out16
19
Out19
S6C
S8C
18
Out18
21
Out21
OK
Cancel
Help
Apply

Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: 1

Period (secs): T

Pulse Width (% of period): 300/(8)

Phase delay (secs): 7*T/(8)

☑ Interpret vector parameters as 1-D

(a)

**FIGURE 9.18**
TPFLCHBI. (a) Gate drive.

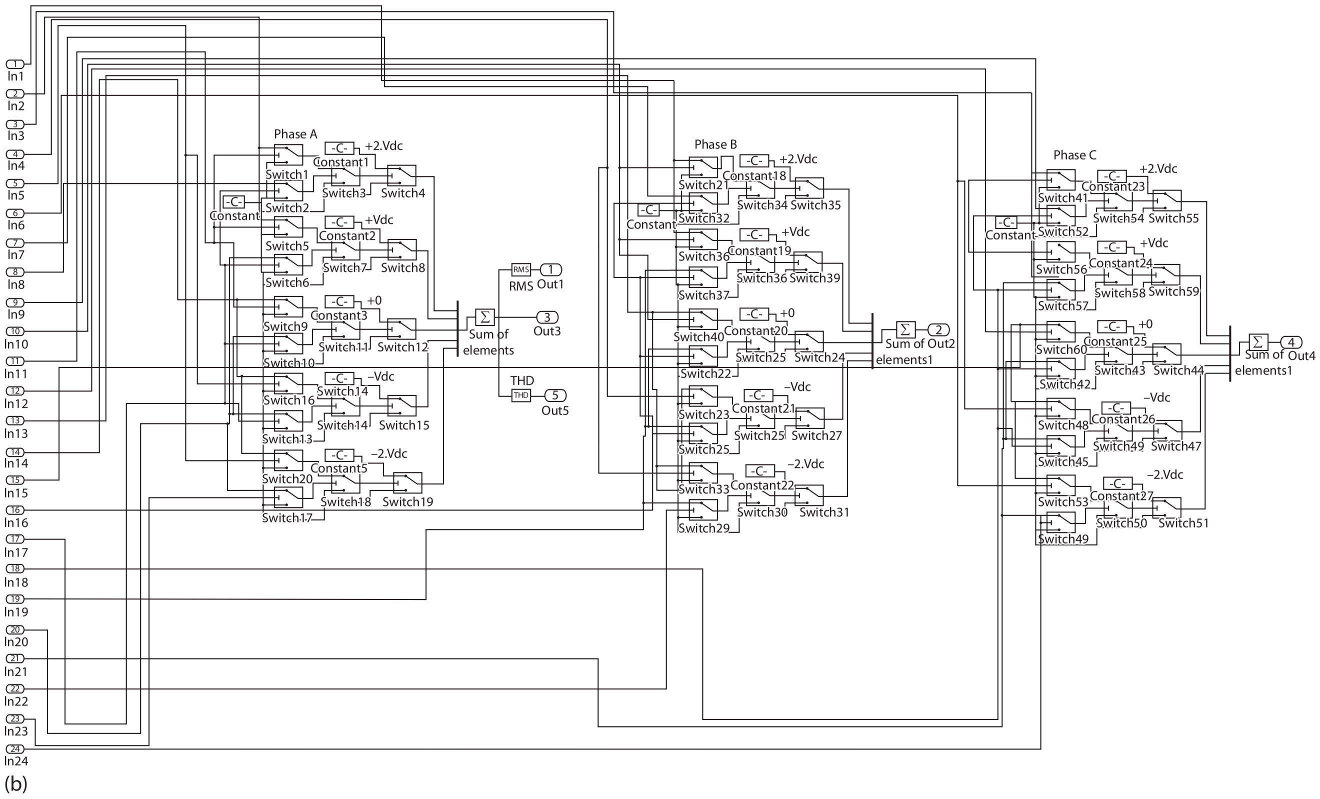

In1
In2
In3
In4
In5
In6
In7
In8
In9
In10
In11
In12
In13
In14
In15
In16
In17
In18
In19
In20
In21
In22
In23
In24
Phase A
-C-
+2.Vdc
Constant1
Switch1
Switch2
Switch3
Switch4
Constant
+Vdc
Constant2
Switch5
Switch6
Switch7
Switch8
+0
Constant3
Switch9
Switch10
Switch11
Switch12
−Vdc
Switch14
Switch16
Switch13
Switch14
Switch15
−2.Vdc
Constant5
Switch20
Switch17
Switch18
Switch19
Sum of elements
RMS
RMS Out1
Out3
THD
Out5
Phase B
+2.Vdc
Constant18
Switch21
Switch32
Switch34 Switch35
+Vdc
Constant19
Switch36
Switch37
Switch36 Switch39
+0
Constant20
Switch40
Switch22
Switch25 Switch24
−Vdc
Constant21
Switch23
Switch25
Switch25 Switch27
−2.Vdc
Constant22
Switch33
Switch29
Switch30 Switch31
Sum of elements1
Out2
Phase C
+2.Vdc
Constant23
Switch41
Switch52
Switch54 Switch55
+Vdc
Constant24
Switch56
Switch57
Switch58 Switch59
+0
Constant25
Switch60
Switch42
Switch43 Switch44
−Vdc
Constant26
Switch48
Switch45
Switch49 Switch47
−2.Vdc
Constant27
Switch53
Switch49
Switch50 Switch51
Sum of elements1
Out4
1
2
3
4
5
(b)

**FIGURE 9.18**
TPFLCHBI. (b) Switches.

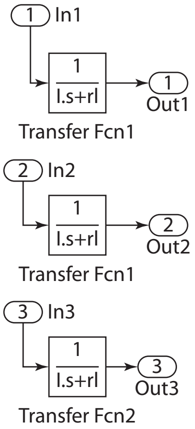


**FIGURE 9.18**
TPFLCHBI. (c) R-L Load.

**TABLE 9.8**
TPFLCHBI: Gate Pulse Phase Delay

| Sl. No. | Switch Phase A | Phase Delay (s) | Switch Phase B | Phase Delay (s) | Switch Phase C | Phase Delay (s) |
|---|---|---|---|---|---|---|
| 1 | S1A | 7*T/8 | S1B | 7*T/8−2*T/3 | S1C | 7*T/8−T/3 |
| 2 | S2A | 2*T/8 | S2B | 2*T/8−2*T/3 | S2C | 2*T/8−T/3 |
| 3 | S3A | 3*T/8 | S3B | 3*T/8−2*T/3 | S3C | 3*T/8−T/3 |
| 4 | S4A | 6*T/8 | S4B | 6*T/8−2*T/3 | S4C | 6*T/8−T/3 |
| 5 | S5A | 0*T/8 | S5B | 0*T/8−2*T/3 | S5C | 0*T/8−T/3 |
| 6 | S6A | T/8 | S6B | T/8−2*T/3 | S6C | T/8−T/3 |
| 7 | S7A | 4*T/8 | S7B | 4*T/8−2*T/3 | S7C | 4*T/8−T/3 |
| 8 | S8A | 5*T/8 | S8B | 5*T/8−2*T/3 | S8C | 5*T/8−T/3 |

switches that represent the output phase voltage $v_{Ag}$. A similar principle of operation holds good for the threshold switches in Phases B and C.

The three-phase load connected to the TPFLCHBI is a series combination of resistor and inductor. This load model is shown in Figure 9.18c. This load is represented by a Transfer Function block ($1/(ls+rl)$) in each of the three phases.

### 9.4.2 Simulation Results

The simulation results of the phase-to-ground voltage of the TPFLCHBI is shown in Figure 9.19 for a three-phase 50 Hz inverter switching frequency, using the ode23t (mod. stiff/trapezoidal) solver [9]. The harmonic spectrum of the phase-to-ground voltage of the TPFLCHBI is shown in Figure 9.20. The DC source voltage for each of the H-bridges is 100 V. The RMS value and THD of the phase-to-ground voltage are displayed in Figure 9.19. Simulation results are tabulated in Table 9.9.

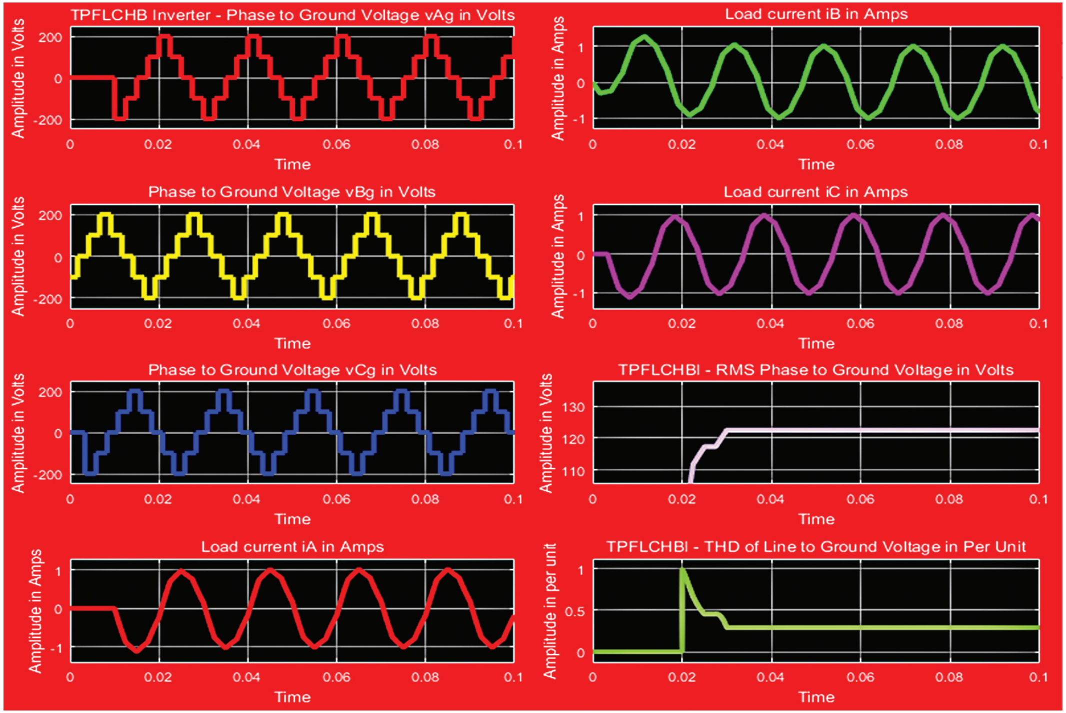


**FIGURE 9.19**
Simulation results for TPFLCHB inverter.

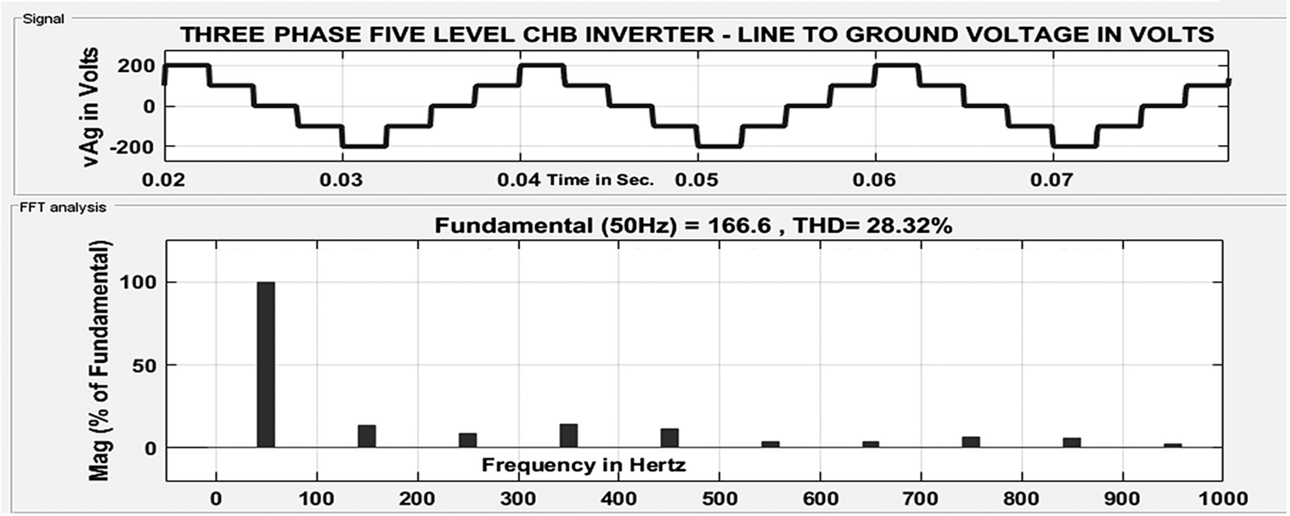


**FIGURE 9.20**
Harmonic spectrum of line-to-ground voltage of TPFLCHB inverter.

**TABLE 9.9**

TPFLCHBI: Simulation Results

| Sl. No. | Symmetrical DC Link Voltage Source (V) | Frequency (Hz) | $V_{Ag}$ RMS (V) | $V_{Ag}$ THD (%) |
|---|---|---|---|---|
| 1 | 100 | 50 | 122.5 | 29.02 |

## 9.5 RMS Value and Harmonic Analysis of the Line-to-Line Voltage of Three-Phase DCTLI and FCTLI

The line-to-ground voltage of the three-phase DCTLI and FCTLI is defined as follows:

$$\begin{aligned} V_{rg} &= +\frac{V_{dc}}{2} \quad \text{for} \quad 0 \le \omega t \le \pi/2 \\ &= 0 \quad \text{for} \quad \pi/2 \le \omega t \le \pi \\ &\quad \text{and} \quad \text{for} \quad 3\pi/2 \le \omega t \le 2\pi \\ &= -\frac{V_{dc}}{2} \quad \text{for} \quad \pi \le \omega t \le 3\pi/2 \end{aligned} \tag{9.2}$$

$$\begin{aligned} V_{rg} &= +\frac{V_{dc}}{2} \quad \text{for} \quad 2\pi/3 \le \omega t \le 7\pi/6 \\ &= 0 \quad \text{for} \quad \pi/6 \le \omega t \le 2\pi/3 \\ &\quad \text{and} \quad \text{for} \quad 7\pi/6 \le \omega t \le 10\pi/6 \\ &= -\frac{V_{dc}}{2} \quad \text{for} \quad 10\pi/6 \le \omega t \le 13\pi/6 \end{aligned} \tag{9.3}$$

Subtracting Equation 9.2 from Equation 9.3, the equation for $V_{ry}$ can be defined as follows:

$$\begin{aligned} V_{ry} &= +V_{dc} \quad \text{for} \quad 0 \le \omega t \le \pi/6 \\ &= +\frac{V_{dc}}{2} \quad \text{for} \quad \pi/6 \le \omega t \le \pi/2 \\ &\quad \text{and} \quad \text{for} \quad 10\pi/6 \le \omega t \le 2\pi \\ &= 0 \quad \text{for} \quad \pi/2 \le \omega t \le 2\pi/3 \\ &\quad \text{and} \quad \text{for} \quad 3\pi/2 \le \omega t \le 10\pi/6 \\ &= -\frac{V_{dc}}{2} \quad \text{for} \quad 2\pi/3 \le \omega t \le \pi \\ &\quad \text{and} \quad \text{for} \quad 7\pi/6 \le \omega t \le 3\pi/2 \\ &= -V_{dc} \quad \text{for} \quad \pi \le \omega t \le 7\pi/6 \end{aligned} \tag{9.4}$$

The line-to-line voltage harmonics are derived as follows using a Fourier series. Considering one half-cycle of line voltage $V_{ry}$ in Figure 9.7a,b or Figure 9.14a,b and using Equation 9.4, with an axis of symmetry where $f(-t) = -f(t)$, the Fourier expression for the $n$th harmonic line-to-line voltage $V_{ryn}$ is derived as follows:

$$V_{ryn} = b_n * \sin(n.\omega.t) \tag{9.5}$$

The coefficient $b_n$ is derived as follows:

$$\begin{aligned} b_n = \frac{2}{\pi} * \left[ \int_{\pi/12}^{5\pi/12} \left(V_{dc}/2\right).\sin\left(n.\omega.t\right).d\left(\omega.t\right) + \int_{5\pi/12}^{7\pi/12} V_{dc}.\sin\left(n.\omega.t\right).d\left(\omega.t\right) \right] \\ + \int_{7\pi/12}^{11\pi/12} \left(V_{dc}/2\right).\sin\left(n.\omega.t\right).d\left(\omega.t\right) \end{aligned} \tag{9.6}$$

Simplifying Equation 9.6, we have the following:

$$b_n = \frac{2V_{dc}.\cos\left(\pi.n/6\right)}{\pi.n} * \left[\cos\left(\pi.n/4\right) - \cos\left(3\pi.n/4\right)\right] \tag{9.7}$$

The RMS value of line-to-line voltage $V_{ry}$ is derived as follows:

$$V_{ry\_rms} = \left[ \frac{1}{\pi} * \left[ \int_{0}^{\pi/3} (V_{dc}^2/4)\, d(\omega t) + \int_{\pi/3}^{\pi/2} (V_{dc}^2)\, d(\omega t) + \int_{\pi/2}^{5\pi/6} (V_{dc}^2/4)\, d(\omega t) \right] \right]^{1/2} \tag{9.8}$$

$$V_{ry\_rms} = \frac{V_{dc}}{\sqrt{3}} \tag{9.9}$$

Similarly, referring to the line-to-ground voltage in Figures 9.6 and 9.13 and using Equation 9.2 and noting that each transition from one level to the next are equally spaced at intervals of π/2 rad, the RMS value of line-to-ground voltage $V_{rg}$ is given by the equation:

$$V_{rg\_rms} = \left[ \frac{1}{2\pi} * \left[ \int_{\pi/2}^{\pi} (V_{dc}^2/4)\, d(\omega t) + \int_{3\pi/2}^{2\pi} (V_{dc}^2/4)\, d(\omega t) \right] \right]^{1/2} \tag{9.10}$$

$$V_{rg\_rms} = \frac{V_{dc}}{2 * \sqrt{2}} \tag{9.11}$$

Thus, for a DC link voltage of 381 V, the values of $V_{ry\_rms}$ and $V_{rg\_rms}$ work out to 220 V and 134.7 V, respectively.

The THD of the line-to-line voltage of a three-phase three-level inverter can be expressed as follows:

$$\text{THD } of\ V_{ry} = \sqrt{\frac{(V_{dc}/\sqrt{3})^2}{(\sqrt{3}.V_{dc}/\pi)^2} - 1} \tag{9.12}$$
$$= 30.9\%$$

## 9.6 RMS Value and THD of Phase-to-Ground Voltage of TPFLCHB Inverter

From Table 9.7, it is clear that each of the five voltage levels of the phase-to-ground voltage $v_{Ag}$ has a duration of π/4 rad. Referring to Figure 9.16b or Figure 9.20, drawing a vertical axis midway between the line corresponding to 0 V, it is seen that $f(+t) = -f(-t)$ and the Fourier expression for the *n*th harmonic of $v_{Agn}$ can be expressed as follows:

$$V_{Agn} = b_n * \sin(n.\omega.t) \tag{9.13}$$

Coefficient $b_n$ is derived as follows:

$$\begin{aligned} b_n = \frac{2}{\pi} * \Bigg[ & \int_{-\pi/8}^{+\pi/8} 0 * d(\omega.t) + \int_{+\pi/8}^{+3\pi/8} V_{dc} * \sin(n.\omega.t) * d(\omega.t) \\ & + \int_{+3\pi/8}^{+5\pi/8} 2.V_{dc} * \sin(n.\omega.t) * d(\omega.t) \\ & + \int_{+5\pi/8}^{+7\pi/8} V_{dc} * \sin(n.\omega.t) * d(\omega.t) + \int_{+7\pi/8}^{+\pi} 0 * d(\omega.t) \Bigg] \end{aligned} \tag{9.14}$$

Equation 9.14 simplifies to the following:

$$b_n = \frac{2 * V_{dc}}{n.\pi} * \left[ \cos\left(\frac{n.\pi}{8}\right) + \cos\left(\frac{3.n.\pi}{8}\right) - \cos\left(\frac{5.n.\pi}{8}\right) - \cos\left(\frac{7.n.\pi}{8}\right) \right] \tag{9.15}$$

$$\begin{aligned} V_{Agn} = \frac{2 * V_{dc}}{n.\pi} * & \left[ \cos\left(\frac{n.\pi}{8}\right) + \cos\left(\frac{3.n.\pi}{8}\right) - \cos\left(\frac{5.n.\pi}{8}\right) - \cos\left(\frac{7.n.\pi}{8}\right) \right] \\ & * \sin(n.\omega.t) \end{aligned} \tag{9.16}$$

Letting *n* equal 1 in Equation 9.16, the RMS value of the fundamental component is as follows:

$$V_{Ag1\_rms} = 1.1765 * V_{dc} \tag{9.17}$$

The RMS value of the phase-to-ground voltage $V_{Ag\_rms}$ can be derived from Figure 9.16b or Figure 9.20, as follows:

$$V_{Ag\_rms} = \left[ \frac{2}{\pi} * \left\{ \int_0^{\pi/4} 0 * d(\omega.t) + \int_{\pi/4}^{\pi/2} V_{dc}^2 * d(\omega.t) + \int_{\pi/2}^{3\pi/4} 4.V_{dc}^2 * d(\omega.t) + \int_{3\pi/4}^{\pi} V_{dc}^2 * d(\omega.t) \right\} \right]^{\frac{1}{2}} \tag{9.18}$$

Equation 9.18 simplifies to the following:

$$V_{Ag\_rms} = \sqrt{\frac{3}{2}} * V_{dc} \tag{9.19}$$

The THD of $V_{Ag}$ is derived as follows:

$$\begin{aligned} \text{THD } of\ V_{Ag} &= \sqrt{\left( \frac{1.2249 * V_{dc}}{1.1765 * V_{dc}} \right)^2 - 1} \\ &= 0.2898 \text{ per unit} \end{aligned} \tag{9.20}$$

## 9.7 Pulse Width Modulation Methods for Multilevel Converters

The methods used for PWM of conventional two-level inverters can be extended for multilevel converters [10–11]. The three PWM methods used for multilevel converters can be classified as (1) multilevel carrier-based sine PWM or multi-carrier sine PWM; (2) selective harmonic elimination PWM; and (3) multilevel space vector PWM.

The multi-carrier-based sine PWM method can be classified into two groups: (1) multi-carrier sine phase-shift PWM (MSPSPWM) and (2) multi-carrier sine level shift PWM (MSLSPWM). In this method, depending on the voltage level of the multilevel converter, triangle carriers having the same peak value $A_c$ and carrier frequency $f_c$ Hz are either shifted in phase or shifted in voltage level and then compared with a sine-wave reference signal or modulating signal whose peak-to-peak value is $A_m$ and frequency $f_m$ Hz and is zero centred at the middle of the triangle carrier set. The reference sine-wave signal is compared with each of the triangle carrier signals. If the carrier signal is less than the sine reference signal, then the switch corresponding to that carrier is turned ON, and if the carrier signal is greater than the sine reference signal, the relevant switch is turned OFF. In multilevel converters having output voltage levels $m$, the amplitude modulation and frequency modulation indices $m_a$ and $m_f$ are defined as follows:

$$m_a = \frac{A_m}{(m-1)*A_c} \tag{9.21}$$

$$m_f = \frac{f_c}{f_m} \tag{9.22}$$

In this chapter, interactive system models for these two types of MSPWM are presented. The models developed are suitable for three-phase DCTLI, FCTLI and TPFLCHBI.

### 9.7.1 Multi-Carrier Sine Phase-Shift PWM

In this method, identical triangle carriers each with a peak value of +1 and −1 V and frequency $f_c$ Hz are shifted in phase from each other by either 360/$k$ or 180/$k$, where $k$ is the number of triangle carriers used. The value of $k$ is based on the output voltage level of the multilevel converter. For three-phase DCTLI and FCTLI, two triangle carriers are used. For a TPFLCHBI, four triangle carriers are required. The number of triangle carriers required is given by ($m-1$), where $m$ is the output phase-to-ground voltage levels.

The interactive model of the MSPSPWM generator is shown in Figure 9.21, along with its dialogue boxes. Up to five triangle carriers are provided, suitable for three-phase DCTLI, FCTLI and FLCHBI. The inner subsystems are shown in Figure 9.22a,b. Referring to Figure 9.21, the two subsystems are 'Multi-Triangle Phase Shift Carrier Generator' and 'Multi-Carrier Phase Shift PWM Three-Phase Sine Modulating Signal Generator'. The schematic of the former and latter subsystems are shown in Figure 9.22a,b.

Program Segment 9.1

```
function [va,vb,vc] = fcn(vm,f,t)
va = vm*sin(2*pi*f*t);
vb = vm*sin(2*pi*f*t - 2*pi/(3));
vc = vm*sin(2*pi*f*t + 2*pi/(3));
```

Figure 9.22a generates phase shifted triangle carriers each with a positive and negative peak of +1 and −1 V, respectively. The 'Pulse Generator'

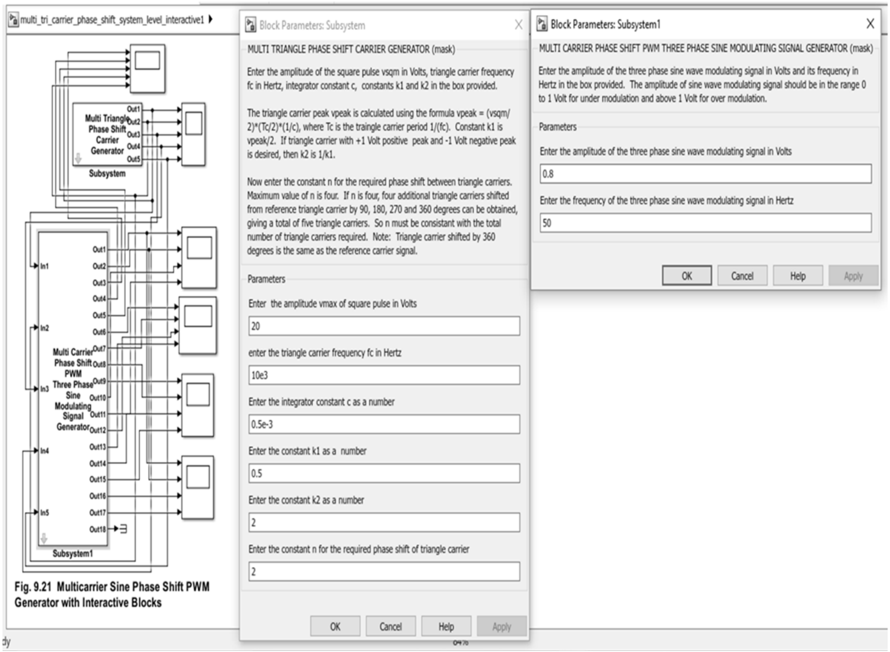

multi_tri_carrier_phase_shift_system_level_interactive1
Multi Triangle Phase Shift Carrier Generator
Subsystem
Out1
Out2
Out3
Out4
Out5
In1
In2
In3
In4
In5
Multi Carrier Phase Shift PWM Three Phase Sine Modulating Signal Generator
Out6
Out7
Out8
Out9
Out10
Out11
Out12
Out13
Out14
Out15
Out16
Out17
Out18
Subsystem1
Block Parameters: Subsystem
OK
Cancel
Help
Apply
Block Parameters: Subsystem1
OK
Cancel
Help
Apply

Fig. 9.21 Multicarrier Sine Phase Shift PWM Generator with Interactive Blocks

MULTI TRIANGLE PHASE SHIFT CARRIER GENERATOR (mask)

Enter the amplitude of the square pulse vsqm in Volts, triangle carrier frequency fc in Hertz, integrator constant c, constants k1 and k2 in the box provided.

The triangle carrier peak vpeak is calculated using the formula vpeak = (vsqm/2)*(Tc/2)*(1/c), where Tc is the traingle carrier period 1/(fc). Constant k1 is vpeak/2. If triangle carrier with +1 Volt positive peak and -1 Volt negative peak is desired, then k2 is 1/k1.

Now enter the constant n for the required phase shift between triangle carriers. Maximum value of n is four. If n is four, four additional triangle carriers shifted from reference triangle carrier by 90, 180, 270 and 360 degrees can be obtained, giving a total of five triangle carriers. So n must be consistant with the total number of triangle carriers required. Note: Triangle carrier shifted by 360 degrees is the same as the reference carrier signal.

Parameters

Enter the amplitude vmax of square pulse in Volts
20

enter the triangle carrier frequency fc in Hertz
10e3

Enter the integrator constant c as a number
0.5e-3

Enter the constant k1 as a number
0.5

Enter the constant k2 as a number
2

Enter the constant n for the required phase shift of triangle carrier
2

MULTI CARRIER PHASE SHIFT PWM THREE PHASE SINE MODULATING SIGNAL GENERATOR (mask)

Enter the amplitude of the three phase sine wave modulating signal in Volts and its frequency in Hertz in the box provided. The amplitude of sine wave modulating signal should be in the range 0 to 1 Volt for under modulation and above 1 Volt for over modulation.

Parameters

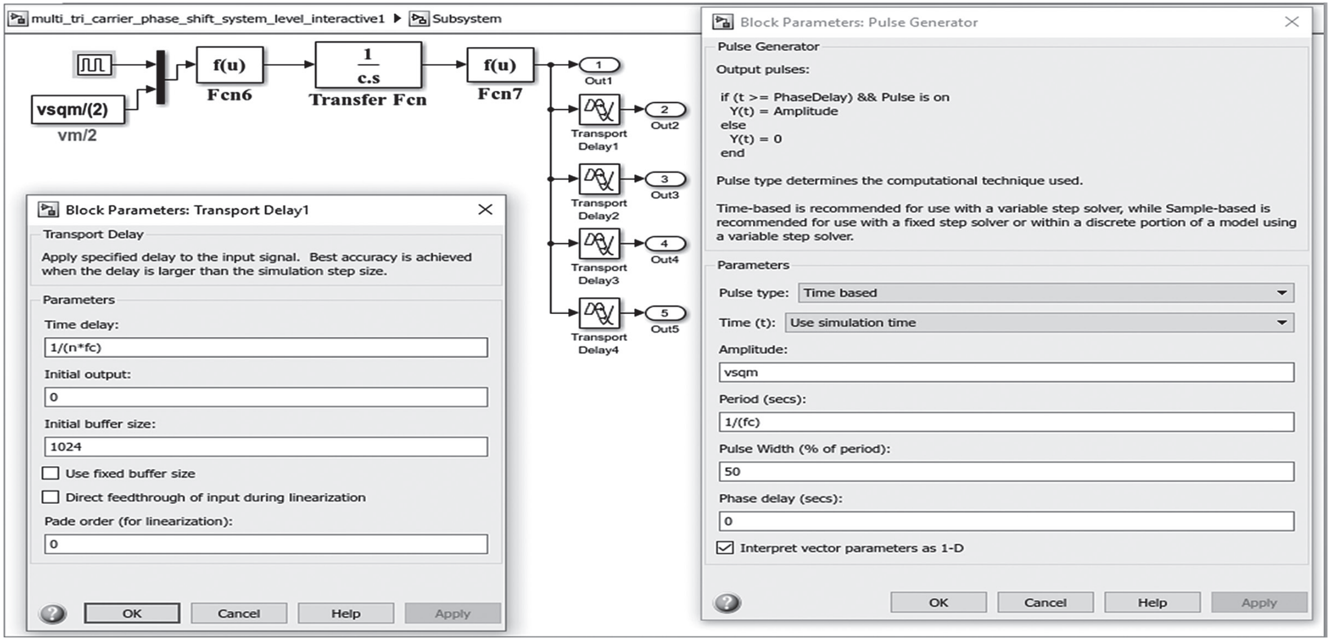
Enter the amplitude of the three phase sine wave modulating signal in Volts
0.8

Enter the frequency of the three phase sine wave modulating signal in Hertz
50

**FIGURE 9.21**
MCSPSPWM generator with interactive blocks.

and 'Transport Delay1' dialogue boxes are shown in Figure 9.22a. The pulse amplitude entered is 'vsqm' and the frequency entered in hertz is 'fc', which corresponds to the triangle carrier frequency. Inputs to the mux are pulse amplitude vsqm and constant vsqm/2. These two values are subtracted using the Fcn6 block and the resulting output is passed to Transfer Function block $1/c.s$, where $c$ is a constant. The output of the Transfer Fcn block is a triangle carrier with frequency $f_c$ Hz, peak value $v_{peak}$ and minimum value zero. This triangle carrier is the input $u$ to the Fcn7 block that performs the operation $(u-k1)*k2$, where $k1=v_{peak}/2$ and $k2=1/k1$. The output of the Fcn7 block is the triangle carrier having frequency $f_c$ Hz, positive peak +1 V and negative peak −1 V. The constant $c$ is calculated using the formula $v_{peak}=(\text{vsqm}/2)*(T_c/2)*1/c$, where $T_c=1/f_c$ is the carrier period.

The Transport Delay1 to 4 blocks generate the necessary phase shift from the reference triangle carrier. The dialogue box for the Transport Delay1 block is shown in Figure 9.22a. Here, Time Delay is entered as '1/(n*fc)', where n is an integer constant, depending on the number of phase shifted triangle carriers required. The value 1 for $n$ creates no phase shift. The values $n=2,3,4$ create a total of two, three and four triangle carriers, each phase shifted by 180°, 120° and 90°, respectively.


multi_tri_carrier_phase_shift_system_level_interactive1 ▶ Subsystem
vsqm/(2)
vm/2
f(u)
Fcn6
1
c.s
Transfer Fcn
f(u)
Fcn7
1
Out1
Transport Delay1
2
Out2
Transport Delay2
3
Out3
Transport Delay3
4
Out4
Transport Delay4
5
Out5
OK
Cancel
Help
Apply
OK
Cancel
Help
Apply

Block Parameters: Transport Delay1

Transport Delay

Apply specified delay to the input signal. Best accuracy is achieved when the delay is larger than the simulation step size.

Parameters

Time delay:
1/(n*fc)

Initial output:
0

Initial buffer size:
1024

☐ Use fixed buffer size

☐ Direct feedthrough of input during linearization

Pade order (for linearization):
0

Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude:
vsqm

Period (secs):
1/(fc)

Pulse Width (% of period):
50

Phase delay (secs):
0

☑ Interpret vector parameters as 1-D

(a)

**FIGURE 9.22**
Multi-carrier (a) generator with interactive blocks.

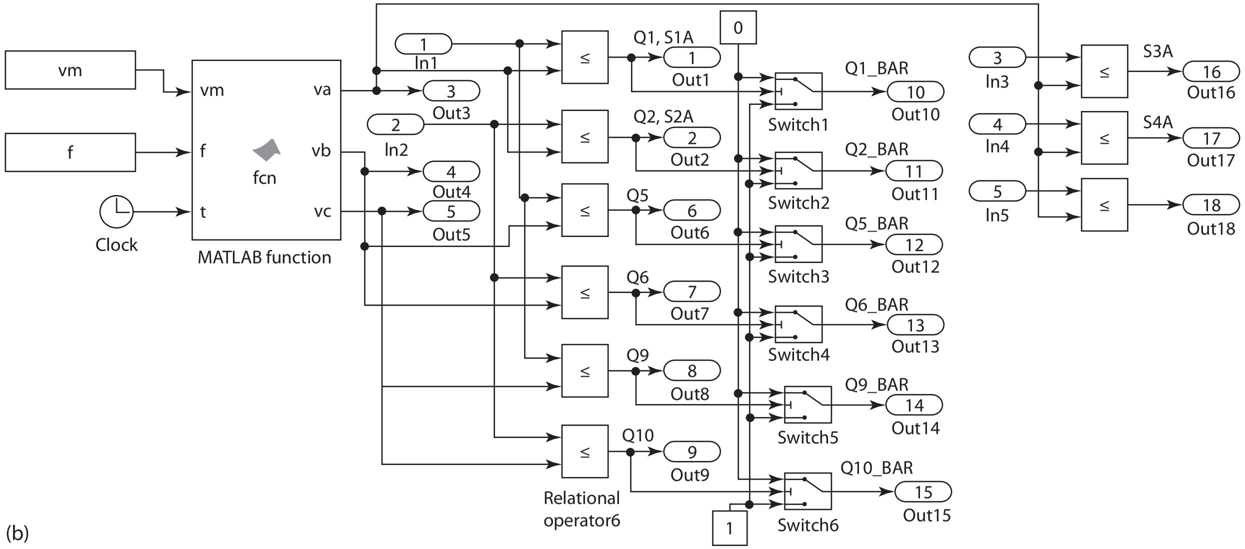

vm
f
Clock
vm
f
t
fcn
va
vb
vc
MATLAB function
1
In1
2
In2
3
Out3
4
Out4
5
Out5
≤
Relational
operator6
Q1, S1A
1
Out1
Q2, S2A
2
Out2
Q5
6
Out6
Q6
7
Out7
Q9
8
Out8
Q10
9
Out9
0
1
Switch1
Switch2
Switch3
Switch4
Switch5
Switch6
Q1_BAR
10
Out10
Q2_BAR
11
Out11
Q5_BAR
12
Out12
Q6_BAR
13
Out13
Q9_BAR
14
Out14
Q10_BAR
15
Out15
3
In3
4
In4
5
In5
S3A
16
Out16
S4A
17
Out17
18
Out18
(b)

**FIGURE 9.22**
Multi-carrier (b) sine PWM generator.

Figure 9.22b shows the model of a multi-carrier sine PWM generator, whose dialogue box is shown in Figure 9.21. The MATLAB® function generates a three-phase sine-wave modulating signal with peak value 'vm' (0.8 V) and frequency '*f*' (50 Hz) as per the code given in Program Segment 9.1. The respective triangle carrier and the sine-wave modulating signals are compared in Relational Operator blocks to obtain the gate pulses for the multilevel converter switches. For three-phase DCTLI and FCTLI, these gate pulses are also inverted using a NOT gate marked Switch1 to Switch6 in Figure 9.22b. For DCTLI, Q3g = (~Q1g) and Q2g = (~Q4g), where the additional suffix g stands for the gate pulse of the respective switch and the tilde symbol (~) stands for a logic NOT operation. Similarly, for FCTLI, Q4g = (~Q1g) and Q3g = (~Q2g). For TPFLCHBI, these NOT gate outputs are not required. The operation of Switch1 to Switch6 as NOT gates is explained next.

Referring to Switch1 to Switch6 in Figure 9.22b, it is seen that their first input $u(1)$ and third input $u(3)$ are 0 and 1, while the control input $u(2)$ is the gate pulse from the respective Relational Operator block. All the switches from 1 to 6 have a threshold value of 0.5 and output $u(1)$ when $u(2)$ is greater than or equal to 0.5 and output $u(3)$ when $u(2)$ is less than 0.5. Thus, when the gate pulse to the respective Switch1 to Switch6 is HIGH (logic 1), the output is 0 (LOW), and when this gate pulse is LOW (logic 0), the output is 1 (HIGH).

### 9.7.2 Simulation Results

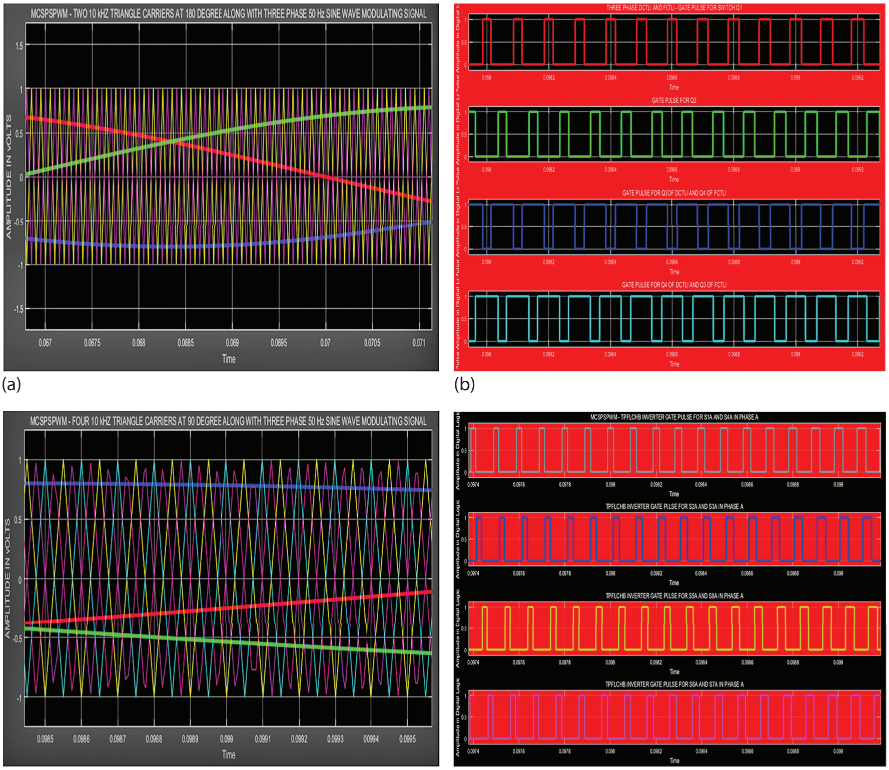
The model simulation of the MSPSPWM generator was carried out using the ode23t (mod. stiff/trapezoidal) solver [9]. The sine-wave peak amplitude and frequency used are 0.8 and 50°Hz respectively. The triangle carrier frequency is 10°kHz. The simulation results for the gate pulse in Phase R of three-phase DCTLI and FCTLI are shown in Figure 9.23a and b and for three-phase FLCHBI are shown in Figure 9.23c and d.

### 9.7.3 Multi-Carrier Sine Level Shift PWM

In the multi-carrier sine level shift PWM (MSLSPWM) method, identical triangle carriers with the same frequency ($f_c$ Hz) and amplitude +1 V are shifted in level. These triangle carriers occupy positions symmetrically above and below relative to the *x*-axis or zero-level axis. The sine-wave modulating signal is centred along the zero-level axis.

The model of the MSLSPWM generator is shown in Figure 9.24a–d. Each one generates a different type of carrier pattern for MSLSPWM. The same model with interactive blocks is shown in Figure 9.25. The internal subsystems of the model are shown in Figure 9.26a,b.

The dialogue boxes relating to subsystems 'Multi-Triangle Carrier PWM Generator' and 'Multi-Carrier Level Shift Three-Phase Sine PWM Generator' are shown in Figure 9.25. The method of generating the level-shifted triangle



(a) (b) (c) (d)

**FIGURE 9.23**
MCSPSPWM. (a) Two 10 kHz triangle carriers and three-phase 50 Hz sine-wave modulating signal. (b) Gate pulse for Phase R of three-phase DCTLI and FCTLI. (c) Four 10 kHz triangle carriers and three-phase 50 Hz sine-wave modulating signal.

carrier is shown in Figure 9.26a and the MSLSPWM three-phase sine PWM gate pulse generator block is shown in Figure 9.26b. In Figure 9.25, in the dialogue box ‘Multi-Triangle Carrier PWM Generator’, the relevant data relating to the peak value of the square pulse $v_{sqm}$, carrier frequency $f_c$ Hz and integrator constant $c$ and the peak value of the triangle carrier are entered. In the dialogue box ‘Multi-Carrier Level Shift Three-Phase Sine PWM Generator’, the data relating to the amplitude and frequency of the modulating sine wave are entered.

Figure 9.26a shows the model to generate the triangle carrier with a peak of +1 V, minimum value zero and frequency $f_c$ Hz. The Pulse Generator and Transport Delay dialogue boxes are shown in Figure 9.26a. The pulse amplitude entered is ‘vsqm’ and the frequency entered in hertz is ‘fc’, which corresponds to the triangle carrier frequency. Inputs to the mux are pulse amplitude vsqm and constant vsqm/2. These two values are subtracted using

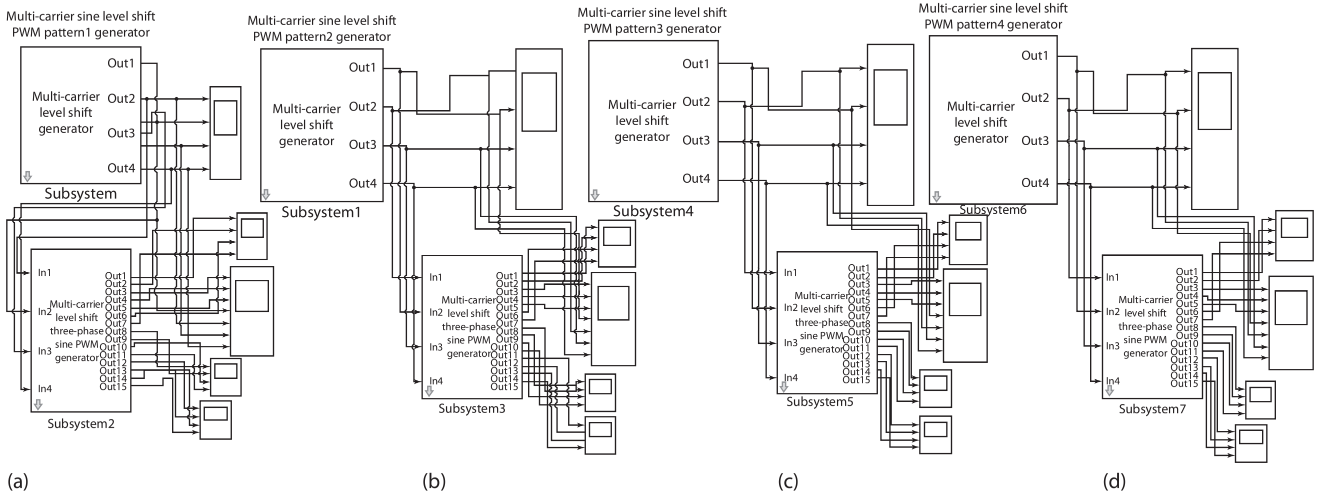
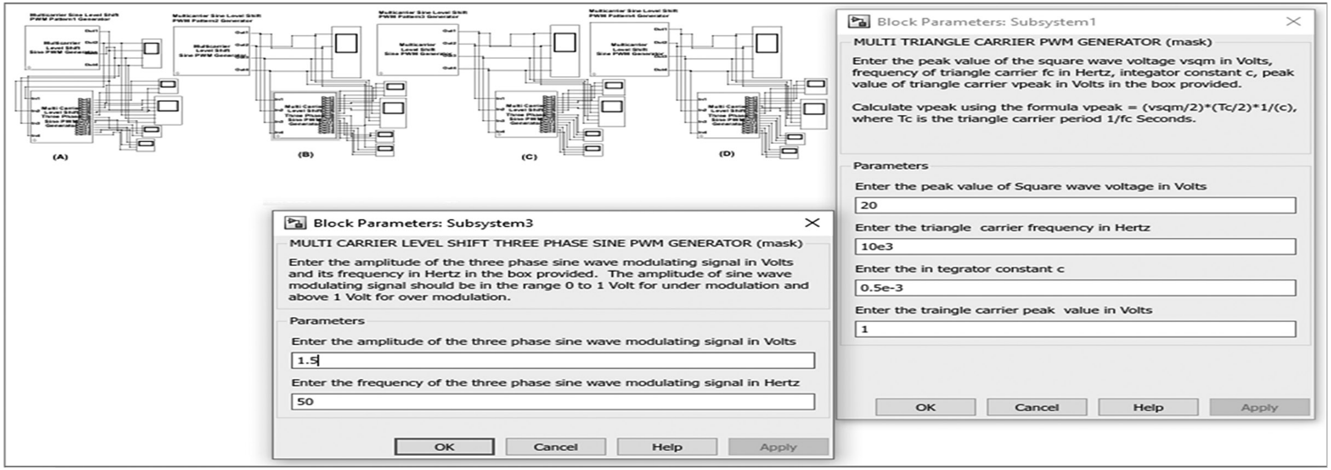

Multi-carrier sine level shift PWM pattern1 generator
Multi-carrier level shift generator
Out1
Out2
Out3
Out4
Subsystem
In1
In2
In3
In4
Multi-carrier level shift three-phase sine PWM generator
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
Out13
Out14
Out15
Subsystem2
(a)
Multi-carrier sine level shift PWM pattern2 generator
Subsystem1
Subsystem3
(b)
Multi-carrier sine level shift PWM pattern3 generator
Subsystem4
Subsystem5
(c)
Multi-carrier sine level shift PWM pattern4 generator
Subsystem6
Subsystem7
(d)

**FIGURE 9.24**
(a–d) MCSLSPWM gate pulse generator.



Block Parameters: Subsystem1

MULTI TRIANGLE CARRIER PWM GENERATOR (mask)

Enter the peak value of the square wave voltage vsqm in Volts, frequency of triangle carrier fc in Hertz, integrator constant c, peak value of triangle carrier vpeak in Volts in the box provided.

Calculate vpeak using the formula vpeak = (vsqm/2)*(Tc/2)*1/(c), where Tc is the triangle carrier period 1/fc Seconds.

Parameters

Enter the peak value of Square wave voltage in Volts

20

Enter the triangle carrier frequency in Hertz

10e3

Enter the in tegrator constant c

0.5e-3

Enter the traingle carrier peak value in Volts

1

Block Parameters: Subsystem3

MULTI CARRIER LEVEL SHIFT THREE PHASE SINE PWM GENERATOR (mask)

Enter the amplitude of the three phase sine wave modulating signal in Volts and its frequency in Hertz in the box provided. The amplitude of sine wave modulating signal should be in the range 0 to 1 Volt for under modulation and above 1 Volt for over modulation.

Parameters

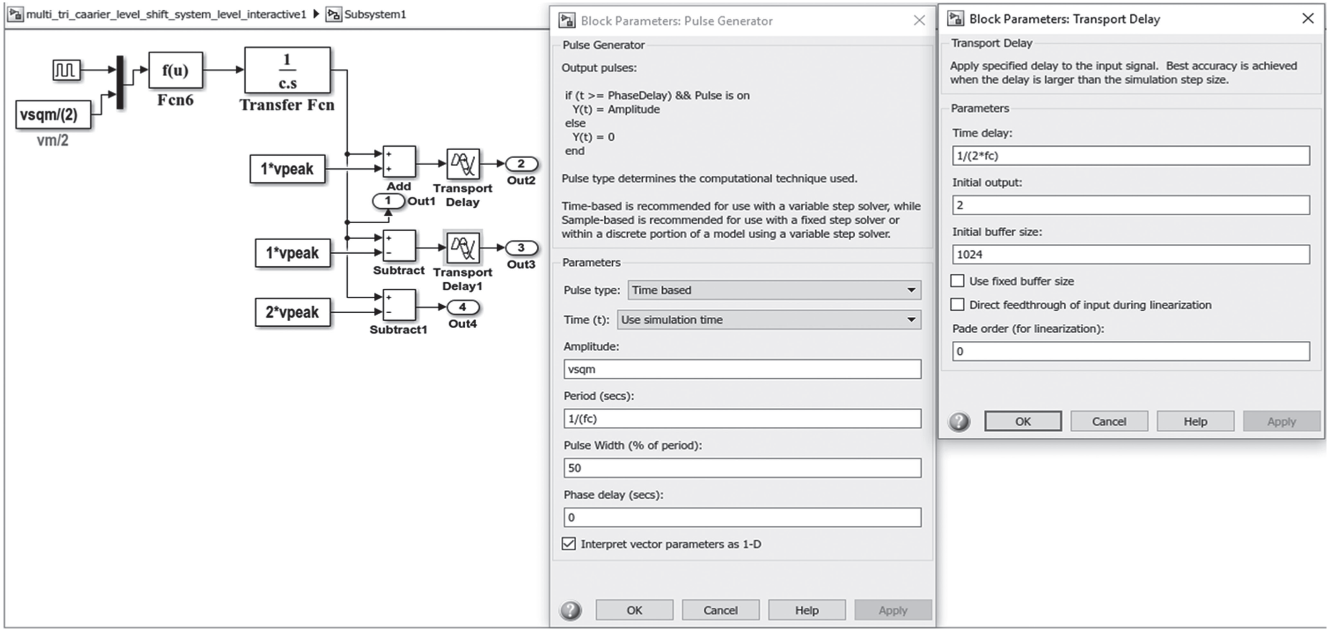
Enter the amplitude of the three phase sine wave modulating signal in Volts

1.5

Enter the frequency of the three phase sine wave modulating signal in Hertz

50

**FIGURE 9.25**
MCSLSPWM gate pulse generator with interactive blocks.


multi_tri_caarier_level_shift_system_level_interactive1 ▶ Subsystem1
vsqm/(2)
vm/2
f(u)
Fcn6
1
c.s
Transfer Fcn
1*vpeak
1*vpeak
2*vpeak
+
+
Add
+
-
Subtract
+
-
Subtract1
Transport Delay
Transport Delay1
1
Out1
2
Out2
3
Out3
4
Out4

Block Parameters: Pulse Generator

Pulse Generator

Output pulses:

```
if (t >= PhaseDelay) && Pulse is on
  Y(t) = Amplitude
else
  Y(t) = 0
end
```

Pulse type determines the computational technique used.

Time-based is recommended for use with a variable step solver, while Sample-based is recommended for use with a fixed step solver or within a discrete portion of a model using a variable step solver.

Parameters

Pulse type: Time based

Time (t): Use simulation time

Amplitude: vsqm

Period (secs): 1/(fc)

Pulse Width (% of period): 50

Phase delay (secs): 0

☑ Interpret vector parameters as 1-D

OK
Cancel
Help
Apply

Block Parameters: Transport Delay

Transport Delay

Apply specified delay to the input signal. Best accuracy is achieved when the delay is larger than the simulation step size.

Parameters

Time delay: 1/(2*fc)

Initial output: 2

Initial buffer size: 1024

☐ Use fixed buffer size

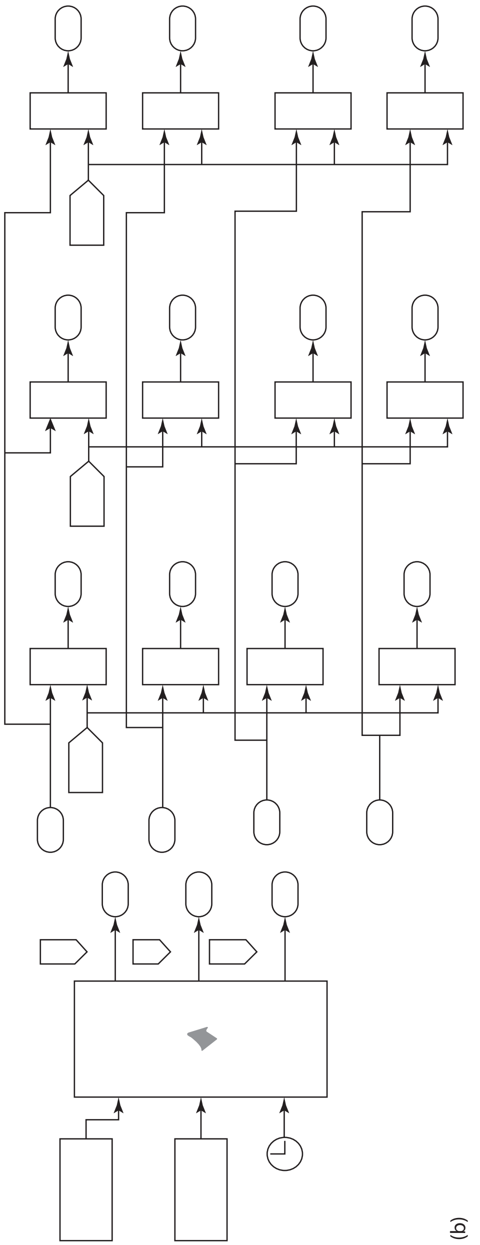
☐ Direct feedthrough of input during linearization

Pade order (for linearization): 0

OK
Cancel
Help
Apply

(a)

**FIGURE 9.26**
MCSLSPWM. (a) Carrier generator.



(b)

**FIGURE 9.26**
MCSLSPWM. (b) Gate pulse generator.

the Fcn6 block and the resulting output is passed to the Transfer Function block $1/c.s$, where $c$ is a constant. The output of the Transfer Fcn block is a triangle carrier with frequency $f_c$ Hz, peak value $v_{peak}$ and minimum value zero. The constant $c$ is calculated using the formula $v_{peak} = (\text{vsqm}/2) * (T_c/2) * (1/c)$, where $T_c = 1/f_c$ is the carrier period. The output of the Transfer Fcn block is a triangle carrier with peak value +1 V, minimum value zero and frequency $f_c$ Hz.

In the Transport Delay and Transport Delay1 dialogue boxes, the time delay entered is '1/(2*fc)'. The triangle carrier output of Transfer Fcn block is added with $1 * v_{peak}$, subtracted from $1 * v_{peak}$ and $2 * v_{peak}$ and delayed by $1/(2 * f_c)$ with two Transport Delay blocks to obtain four different triangle carrier patterns. Figure 9.26a corresponds to carrier pattern B in Figure 9.24. The carrier pattern in Figure 9.24a has *no* Transport Delay blocks. Carrier patterns C and D in Figure 9.24 are generated by relocating the position of the Transport Delay and Transport Delay1 blocks in Figure 9.26a. Referring to Figure 9.26a, by relocating the Transport Delay and Transport Delay1 blocks to the output of the Add and Subtract1 blocks generates one additional carrier pattern, and relocating them to the output of the Subtract and Subtract1 blocks generates a second additional pattern.

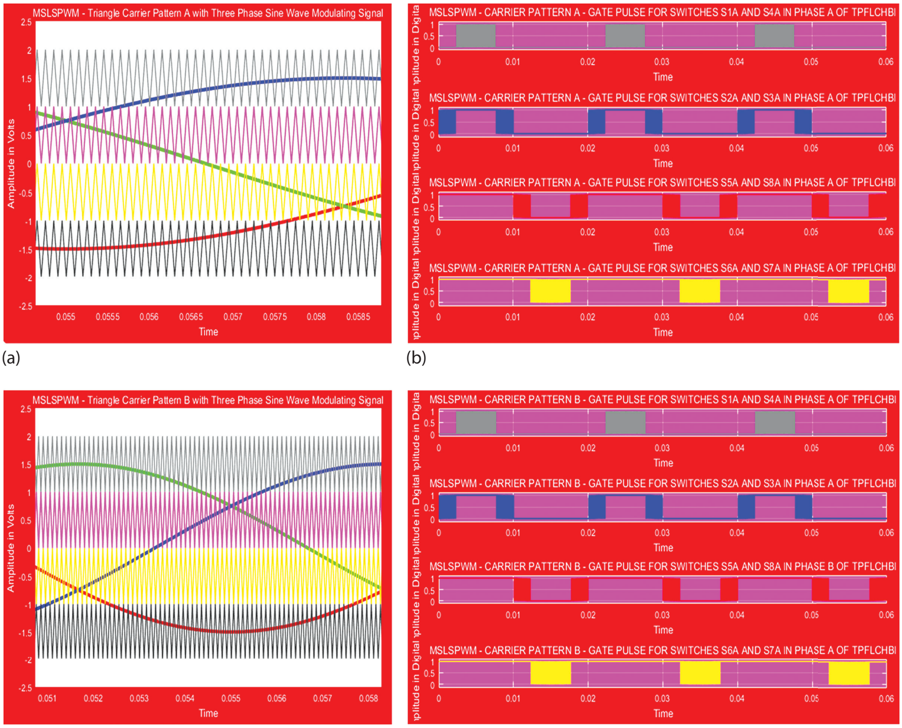
Figure 9.26b shows the model of the MSLSPWM gate pulse generator for the switches of a multilevel converter, using the MATLAB Function and Relational Operator blocks. This model is the same as that already explained in Section 9.7.1.

### 9.7.4 Simulation Results

The simulation of the model of the MSLSPWM generator was carried out using the ode23t (mod. stiff/trapezoidal) solver [9]. The simulation results for the triangle carrier with a three-phase modulating sine-wave and gate pulse for Phase A of the TPFLCHBI are shown in Figure 9.27a–h. The triangle carrier frequency is 10 kHz. The three-phase sine-wave modulating signal has an amplitude of 1.5 V and frequency of 50 Hz. For three-phase DCTLI and FCTLI, two carriers above and below the $x$-axis with the sine-wave peak below +1 V along with NOT gates have to be used, as explained in Section 9.7.1.

## 9.8 Conclusions

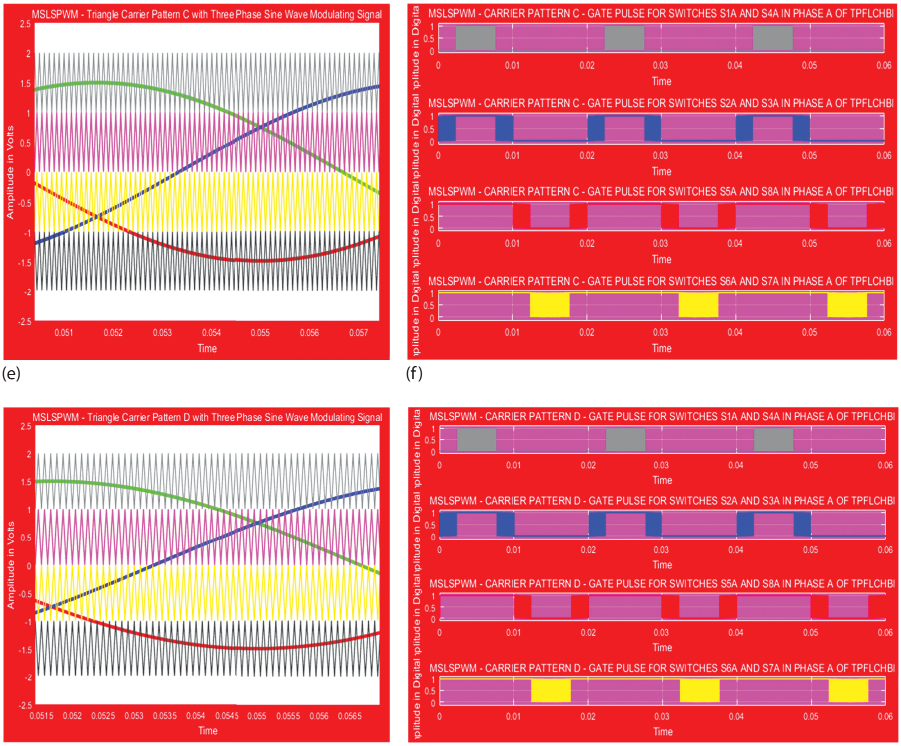
The system models for three-phase DCTLI, FCTLI and FLCHBI have been successfully developed. In these three models, the time intervals for all the voltage levels are equal. By reducing the time duration for the zero voltage level to a lower value compared with the other two voltage levels, it is



(a) (b) (c) (d)

**FIGURE 9.27**
(a) Triangle carrier pattern A with three-phase sine-wave modulating signal (left). (b) Phase A gate pulse for switches of TPFLCHBI (right). (c) Triangle carrier pattern B with three-phase sine-wave modulating signal (left). (d) Phase A gate pulse for switches of TPFLCHBI (right).

possible to reduce the THD of the line-to-line voltage and improve its harmonic spectrum still further [5]. The THD of the line-to-line voltage for the conventional three-phase three-level inverter with equal time duration for all three voltage levels is 31.08% [5]. The THD of the line-to-line voltage by simulation for this DCTLI is found to be around 30.82% and that for the FCTLI is found to be 30.52%, respectively, whereas the calculated value is 30.9%. The RMS line-to-line voltage for the DCTLI and for the FCTLI agree well with the formula given by Equations 9.7 and 9.8. The THD of the phase-to-ground voltage of the TPFLCHBI is found to be 28.98%, whereas by model simulation this value is 29.02%. Similarly, the RMS value of the phase-to-ground voltage of the TPFLCHBI is found to be 122.49 V by derivation, whereas this value is 122.5 V by model simulation. It is also seen from Figures 9.1, 9.8 and 9.15 that the voltage stress across individual semiconductor switches is reduced for a given DC link voltage for the former two topologies and for a given output



(e) (f) (g) (h)

**FIGURE 9.27**
(e) Triangle carrier pattern C with three-phase sine-wave modulating signal (left). (f) Phase A gate pulses for switches of TPFLCHBI (right). (g) Triangle pattern D with three-phase sine-wave modulating signal (left). (h) Gate pulse for Phase A switches of TPFLCHBI (right).

voltage for the third topology, as compared with the conventional three-phase two-level inverter. As the multilevel triangle carrier PWM technique is used for voltage control of multilevel converters, a section on the development of interactive models for MSPSPWM and MSLSPWM techniques are presented with simulation results.

## References

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# 10

# *Interactive Model Verification*

## 10.1 Introduction

In this chapter, interactive component-level models for the power electronic converters discussed in the previous chapters are presented. These are developed using active and passive components used in the power electronic circuits such as semiconductor switches, diodes, the AC source, the DC source and passive components such as resistors, inductors and capacitors. These active and passive components are mainly from the Power Systems block set in Simulink® [1]. The component-level model simulation results presented here provide verification of the system model simulation results of power electronic converters discussed in the previous chapters.

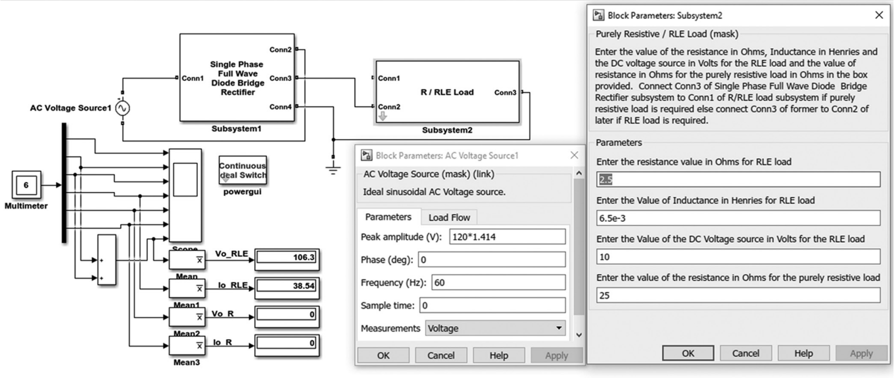
## 10.2 AC to DC Converters

In this section, interactive component-level models for the single-phase full-wave diode bridge rectifier (SFWDBR), single-phase full-wave silicon-controlled rectifier (SCR) converter and three-phase full-wave diode bridge rectifier (TFWDBR) discussed in Chapter 3 are presented [2–5].

### 10.2.1 Single-Phase Full-Wave Diode Bridge Rectifier

The SFWDBR system model presented in Section 3.1 is verified in this section using interactive component-level models [2–5]. The data shown in Table 3.1 are used here. This model with interactive blocks is shown in Figure 10.1. The inner subcircuits of SFWDBR consisting of a semiconductor diode bridge and the purely resistive/RLE load is shown in Figure 10.2a,b. Simulation results for the SFWDBR are shown in Figure 10.3 for RLE load and tabulated in Table 10.1, closely agreeing with Table 3.2.

Simulation results for SFWDBR with purely resistive load can be found similarly and are not shown here.



Block Parameters: AC Voltage Source1

AC Voltage Source (mask) (link)

Ideal sinusoidal AC Voltage source.

Peak amplitude (V): 120*1.414

Phase (deg): 0

Frequency (Hz): 60

Sample time: 0

Measurements: Voltage

Block Parameters: Subsystem2

Purely Resistive / RLE Load (mask)

Enter the value of the resistance in Ohms, Inductance in Henries and the DC voltage source in Volts for the RLE load and the value of resistance in Ohms for the purely resistive load in Ohms in the box provided. Connect Conn3 of Single Phase Full Wave Diode Bridge Rectifier subsystem to Conn1 of R/RLE load subsystem if purely resistive load is required else connect Conn3 of former to Conn2 of later if RLE load is required.

Parameters

Enter the resistance value in Ohms for RLE load: 2.5

Enter the Value of Inductance in Henries for RLE load: 6.5e-3

Enter the Value of the DC Voltage source in Volts for the RLE load: 10

Enter the value of the resistance in Ohms for the purely resistive load: 25

**FIGURE 10.1**
Model of SFWDBR with interactive blocks.

### 10.2.2 Single-Phase Full-Wave SCR Bridge

The circuit schematic of the single-phase full-wave controlled bridge rectifier (SFWCBR) is shown in Figure 3.7 and the derivations for output voltage and current for purely resistive and RLE loads are shown in Section 3.2 [2–5]. In this section, a component-level model for SFWCBR is developed and simulation is carried out for an RLE load as per data given in Table 3.3 and compared.

This model of the SFWCBR is shown in Figure 10.4 and interactive blocks are shown in Figure 10.5. The subsystems for this model are shown Figure 10.6a–e. Figure 10.6a is the single-phase full-wave thyristor bridge rectifier, Figure 10.6b is the thyristor gate firing pulse generator using the Pulse Generator block, Figure 10.6c is the R/RLE load, Figure 10.6d selects either the R or RLE load and Figure 10.6e is the output voltage and current measurement unit.

Referring to Figure 10.6d, if the constant entered is zero, then the switch whose threshold value is 0.5 outputs –1 and the logic comparator on the top marked '<0' becomes HIGH and turns on S2, selecting the RLE load. If the constant entered is 1, then the bottom logic comparator marked '>0' output becomes HIGH, turns on S1 and selects the purely resistive load.

The simulation results for the RLE load are shown in Figure 10.7. The results are tabulated in Table 10.2. The simulation results for the purely resistive load are not shown here. The simulation results in Table 10.2 agree closely with those shown in Table 3.4.

### 10.2.3 Three-Phase Full-Wave Diode Bridge Rectifier

The TFWDBR discussed in Section 3.3 is presented here with a component-level model. The circuit configuration of the TFWDBR is shown in Figure 3.13 [2–5]. The model parameters are shown in Table 3.5. This model of the

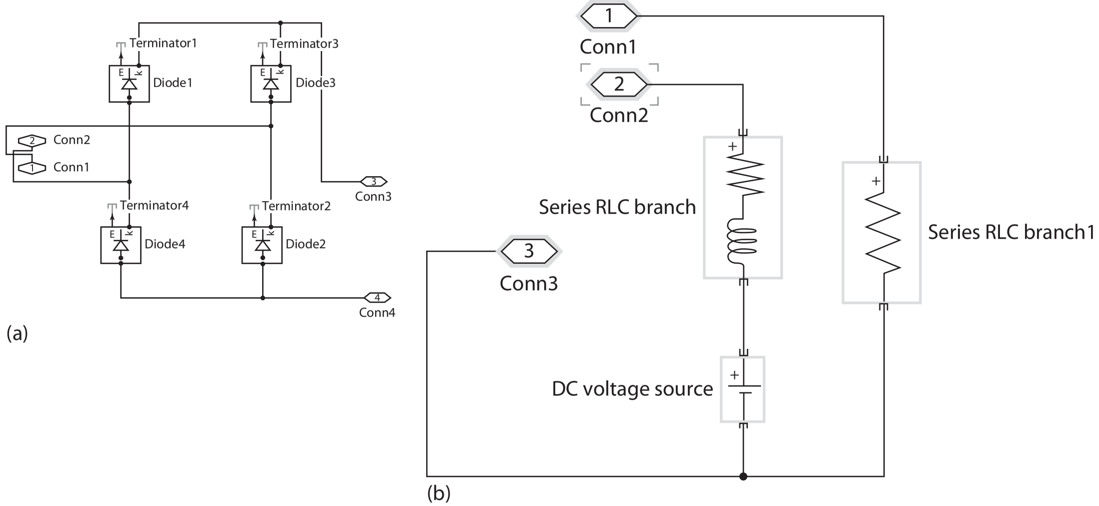

Terminator1
Terminator3
Diode1
Diode3
Conn2
Conn1
Conn3
Terminator4
Terminator2
Diode4
Diode2
Conn4
(a)
1
Conn1
2
Conn2
Series RLC branch
Series RLC branch1
3
Conn3
DC voltage source
(b)

**FIGURE 10.2**
Subcircuits of SFWDBR. (a) Full bridge diode rectifier. (b) RLE and purely resistive loads.

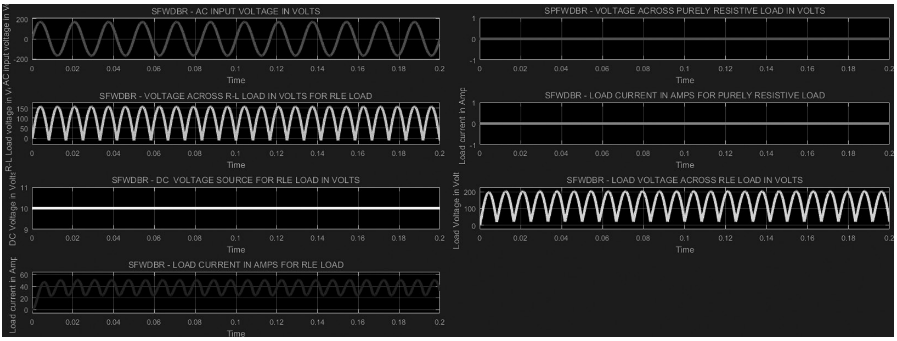


**FIGURE 10.3**
SFWDBR: simulation results for RLE load.

**TABLE 10.1**
SFWDBR: Simulation Results for RLE Load

| Sl. No. | Type of Load | Udc(RMS) (V) | Udc(AVG) (V) | I_load(AVG) (A) |
|---|---|---|---|---|
| 1 | RLE | 120 | 106.3 | 38.5 |

TFWDBR is shown in Figure 10.8. The interactive blocks of this model and its inner subsystems are shown in Figure 10.9 and Figure 10.10a–c, respectively. The three-phase diode rectifier is a built-in model from the Power System block set. This is marked 'Rectifier' in Figure 10.8. The three-phase AC voltage source, resistive load and measurement blocks are shown in Figure 10.10a–c, respectively. The simulation results of this model are shown in Figure 10.11a,b, respectively. The results are tabulated in Table 10.3. The simulation results in Table 10.3 agree closely with those shown in Table 3.6.

## 10.3 DC to AC Converters

In this section, interactive component-level models are developed using semiconductor and passive components for three-phase 180° mode and 120° mode inverters discussed in Chapter 4 [2–5]. The three-phase sine pulse width modulation (PWM) inverter component-level model is presented in Section 10.9. The results obtained by component-level simulation are compared with those in Chapter 4.

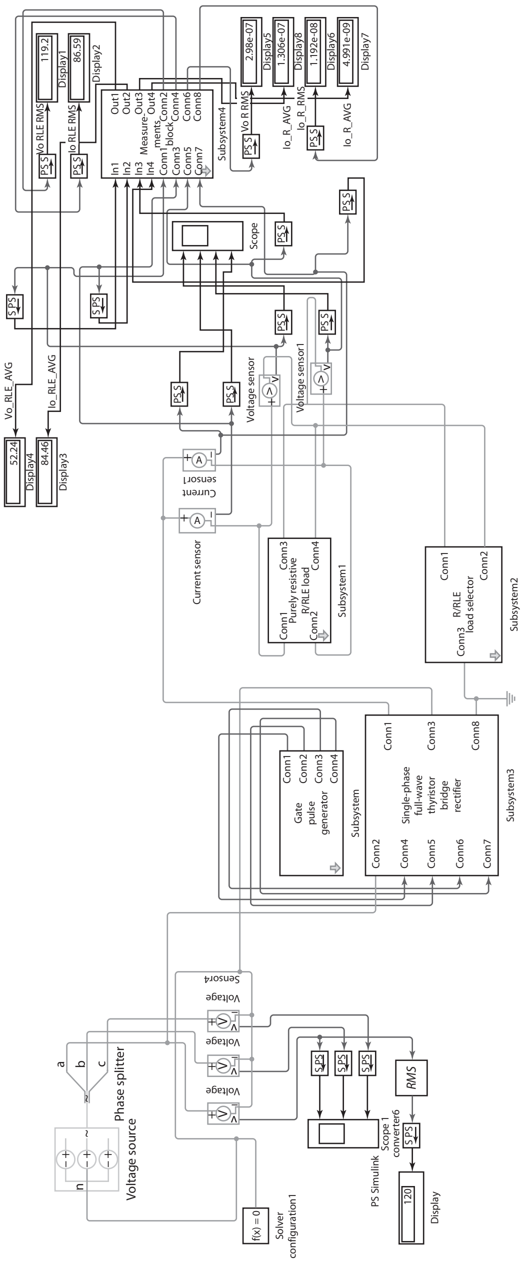
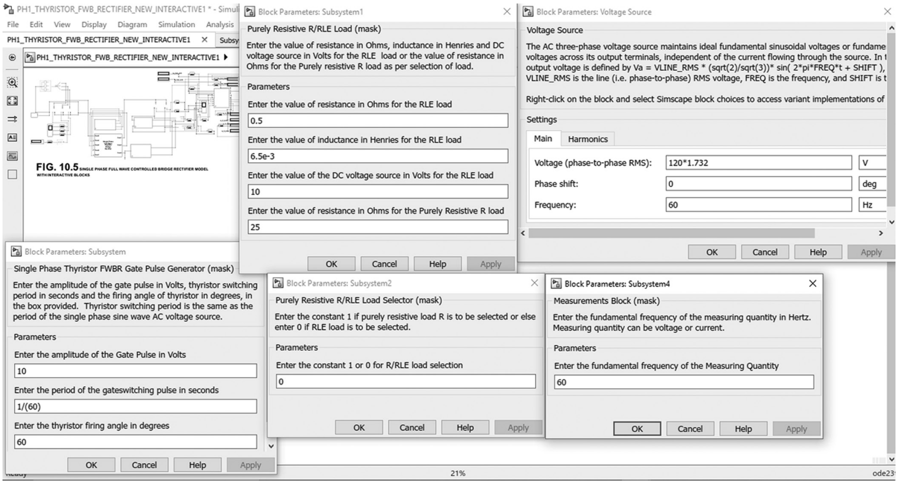

Voltage source
Phase splitter
a
b
c
n
Solver configuration1
f(x) = 0
Voltage
Voltage
Voltage
Sensor4
S PS
RMS
Scope 1
PS Simulink converter6
Display
120
Gate pulse generator
Conn1
Conn2
Conn3
Conn4
Subsystem
Single-phase full-wave thyristor bridge rectifier
Conn5
Conn6
Conn7
Conn8
Subsystem3
Current sensor
Current sensor1
Purely resistive R/RLE load
Subsystem1
R/RLE load selector
Subsystem2
Voltage sensor
Voltage sensor1
PS S
Scope
Vo_RLE_AVG
Io_RLE_AVG
52.24
Display4
84.46
Display3
Vo RLE RMS
119.2
Display1
Io RLE RMS
86.59
Display2
In1
In2
In3
In4
Out1
Out2
Out3
Out4
Measurements block
Subsystem4
Vo R RMS
2.98e-07
Display5
Io_R_AVG
1.306e-07
Display8
Io_R_RMS
1.192e-08
Display6
Io_R_AVG
4.991e-09
Display7

**FIGURE 10.4**
SFWCBR model.


PH1_THYRISTOR_FWB_RECTIFIER_NEW_INTERACTIVE1 * - Simul
File Edit View Display Diagram Simulation Analysis
PH1_THYRISTOR_FWB_RECTIFIER_NEW_INTERACTIVE1
FIG. 10.5 SINGLE PHASE FULL WAVE CONTROLLED BRIDGE RECTIFIER MODEL WITH INTERACTIVE BLOCKS
OK
Cancel
Help
Apply
21%
ode23

Block Parameters: Subsystem1

Purely Resistive R/RLE Load (mask)

Enter the value of resistance in Ohms, inductance in Henries and DC voltage source in Volts for the RLE load or the value of resistance in Ohms for the Purely resistive R load as per selection of load.

Parameters

Enter the value of resistance in Ohms for the RLE load: 0.5

Enter the value of inductance in Henries for the RLE load: 6.5e-3

Enter the value of the DC voltage source in Volts for the RLE load: 10

Enter the value of resistance in Ohms for the Purely Resistive R load: 25

Block Parameters: Voltage Source

Voltage Source

The AC three-phase voltage source maintains ideal fundamental sinusoidal voltages or fundame voltages across its output terminals, independent of the current flowing through the source. In t output voltage is defined by Va = VLINE_RMS * (sqrt(2)/sqrt(3))* sin( 2*pi*FREQ*t + SHIFT ), VLINE_RMS is the line (i.e. phase-to-phase) RMS voltage, FREQ is the frequency, and SHIFT is t

Right-click on the block and select Simscape block choices to access variant implementations of

Settings

Main | Harmonics

Voltage (phase-to-phase RMS): 120*1.732 V

Phase shift: 0 deg

Frequency: 60 Hz

Block Parameters: Subsystem

Single Phase Thyristor FWBR Gate Pulse Generator (mask)

Enter the amplitude of the gate pulse in Volts, thyristor switching period in seconds and the firing angle of thyristor in degrees, in the box provided. Thyristor switching period is the same as the period of the single phase sine wave AC voltage source.

Parameters

Enter the amplitude of the Gate Pulse in Volts: 10

Enter the period of the gateswitching pulse in seconds: 1/(60)

Enter the thyristor firing angle in degrees: 60

Block Parameters: Subsystem2

Purely Resistive R/RLE Load Selector (mask)

Enter the constant 1 if purely resistive load R is to be selected or else enter 0 if RLE load is to be selected.

Parameters

Enter the constant 1 or 0 for R/RLE load selection: 0

Block Parameters: Subsystem4

Measurements Block (mask)

Enter the fundamental frequency of the measuring quantity in Hertz. Measuring quantity can be voltage or current.

Parameters

Enter the fundamental frequency of the Measuring Quantity: 60

**FIGURE 10.5**
SFWCBR model with interactive blocks.

### 10.3.1 Three-Phase 180° Mode Inverter

Detailed analysis of the three-phase 180° mode inverter is given in Section 4.2. The system model for the three-phase 180° mode inverter is presented in Section 4.2.4. Here, the interactive component-level model for this inverter is developed using semiconductor and passive components in the Power Systems block set; the simulation is carried out and compared with that presented in Chapter 4.

This model of the three-phase 180° mode inverter is shown in Figure 10.12, the interactive blocks are shown in Figure 10.13 and the inner subsystems are shown in Figure 10.14a–c [2–5]. Simulation results are shown in Figure 10.15a–d and tabulated in Table 10.4.

Tabulated results for the line-to-line voltage agree well with Tables 4.1 and 4.2.

### 10.3.2 Three-Phase 120° Mode Inverter

Detailed analysis of the three-phase 120° mode inverter is presented in Section 4.3 A detailed system model for this inverter is also presented, in Section 4.3.4. In this section, an interactive component-level model for this inverter is presented; a simulation was carried out and compared with that given in Section 4.3.

This model of this inverter is the same as for the 180° mode inverter shown in Figures 10.12, 10.13 and 10.14. In this 120° mode, the gate pulse duration is only for ($T/3$) seconds, where $T$ is the switching period of the inverter [2–5]. Referring to Figure 10.13, in the Gate Pulse Generator block, against the box 'Enter the Duty-cycle of gate pulse as a percentage', the value 33.3333

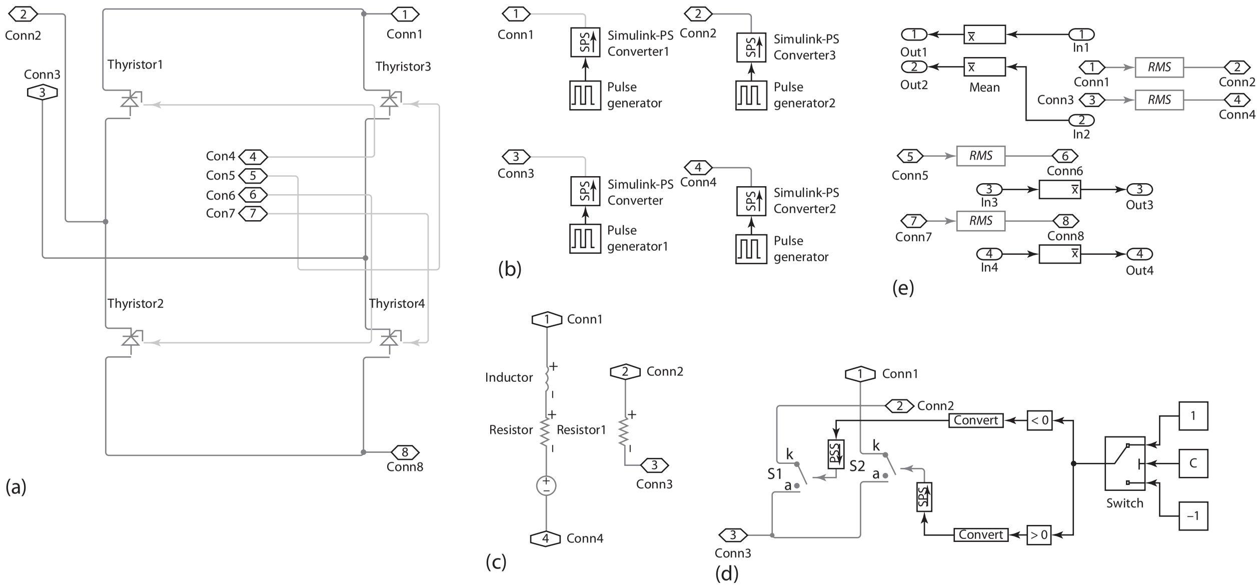

Conn2
Conn1
Conn3
Thyristor1
Thyristor3
Con4
Con5
Con6
Con7
Thyristor2
Thyristor4
Conn8
(a)
Conn1
Simulink-PS Converter1
Pulse generator
Conn2
Simulink-PS Converter3
Pulse generator2
Conn3
Simulink-PS Converter
Pulse generator1
Conn4
Simulink-PS Converter2
Pulse generator
(b)
Conn1
Inductor
Resistor
Resistor1
Conn2
Conn3
Conn4
(c)
Conn1
Conn2
Convert
< 0
k
S1
a
S2
k
a
Switch
1
C
−1
Conn3
Convert
> 0
(d)
Out1
Out2
Mean
In1
Conn1
RMS
Conn2
Conn3
RMS
Conn4
In2
Conn5
RMS
Conn6
In3
Out3
Conn7
RMS
Conn8
In4
Out4
(e)

**FIGURE 10.6**
(a–e) SFWCBR subsystems.

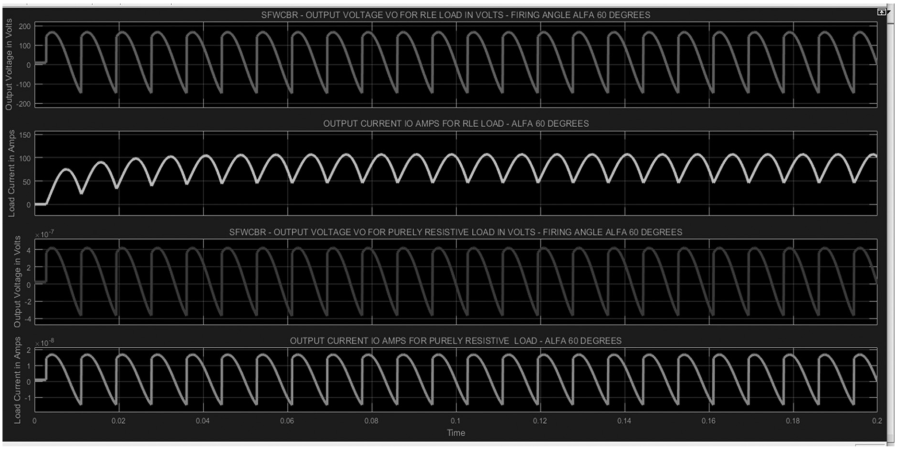


**FIGURE 10.7**
SFWCBR simulation results for RLE load.

**TABLE 10.2**

SFWCBR: Simulation Results with RLE Load: Firing Angle α = 60°

| Sl. No. | Type of Load | $V_{dc}$(RMS) (V) | $V_{dc}$(AVG) (V) | I_load(RMS) (A) | I_load(AVG) (A) | P_out (W) |
|---|---|---|---|---|---|---|
| 1 | RLE | 119.2 | 52.24 | 86.59 | 84.46 | 4412.19 |

is entered. The same three-phase inverter then performs as a 120° mode inverter.

A simulation of this inverter was carried out and the results are presented in Figure 10.16a–d. The results are also tabulated in Table 10.5. The tabulated results in Table 10.5 agree well with the results tabulated in Tables 4.3 and 4.4.

## 10.4 DC to DC Converter

In this section, interactive component-level models for buck, boost and buck–boost converters are developed using semiconductor and passive components [2–5,6,7]. This model simulation is performed for these DC to DC converters and the results obtained are compared with those presented in Chapter 5.

### 10.4.1 Buck Converter

The buck converter analysis in the continuous conduction mode (CCM) and in the discontinuous conduction mode (DCM) is given in Sections 5.2 and 5.3. The data given in Table 5.1 are used here for circuit simulation of the buck converter. The component-level model of the buck converter

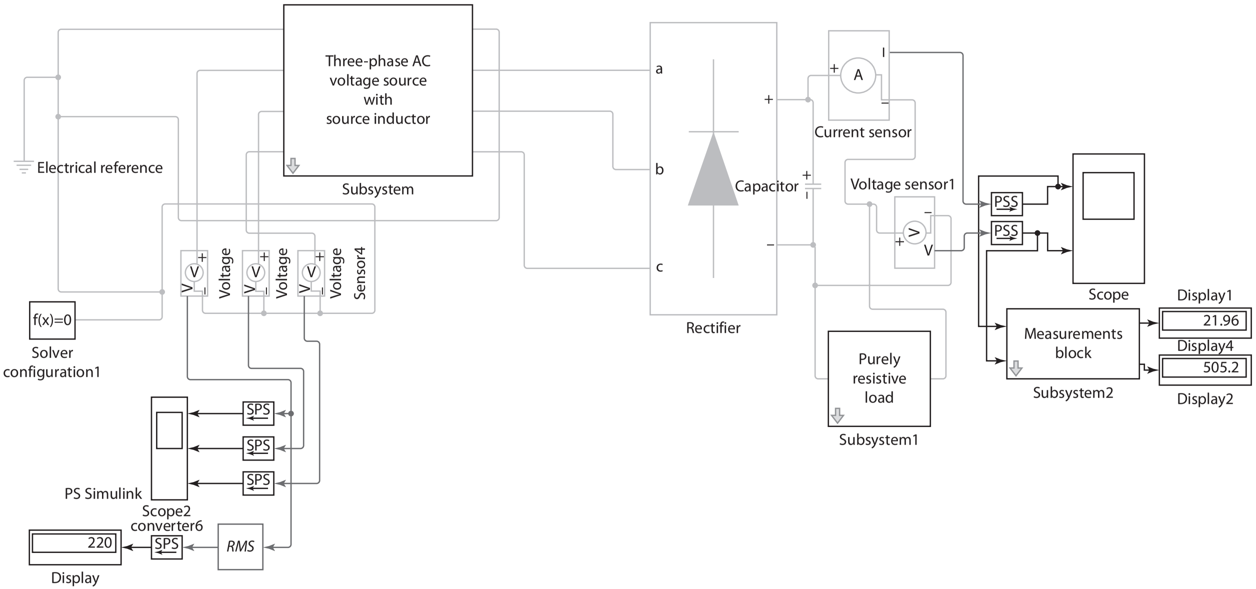
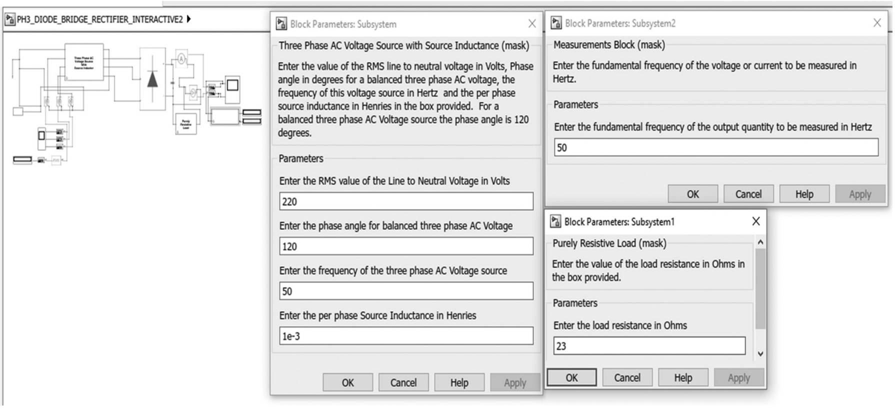

Three-phase AC voltage source with source inductor
Subsystem
Electrical reference
f(x)=0
Solver configuration1
V
+
-
Voltage
Voltage
Voltage Sensor4
SPS
SPS
SPS
PS Simulink
Scope2
converter6
RMS
SPS
220
Display
a
b
c
Rectifier
+
-
Capacitor
A
+
-
I
Current sensor
Voltage sensor1
PSS
PSS
Scope
Purely resistive load
Subsystem1
Measurements block
Subsystem2
Display1
21.96
Display4
505.2
Display2

**FIGURE 10.8**
TFWDBR model.


PH3_DIODE_BRIDGE_RECTIFIER_INTERACTIVE2

Block Parameters: Subsystem

Three Phase AC Voltage Source with Source Inductance (mask)

Enter the value of the RMS line to neutral voltage in Volts, Phase angle in degrees for a balanced three phase AC voltage, the frequency of this voltage source in Hertz and the per phase source inductance in Henries in the box provided. For a balanced three phase AC Voltage source the phase angle is 120 degrees.

Parameters

Enter the RMS value of the Line to Neutral Voltage in Volts: 220

Enter the phase angle for balanced three phase AC Voltage: 120

Enter the frequency of the three phase AC Voltage source: 50

Enter the per phase Source Inductance in Henries: 1e-3

OK Cancel Help Apply

Block Parameters: Subsystem2

Measurements Block (mask)

Enter the fundamental frequency of the voltage or current to be measured in Hertz.

Parameters

Enter the fundamental frequency of the output quantity to be measured in Hertz: 50

OK Cancel Help Apply

Block Parameters: Subsystem1

Purely Resistive Load (mask)

Enter the value of the load resistance in Ohms in the box provided.

Parameters

Enter the load resistance in Ohms: 23

OK Cancel Help Apply

**FIGURE 10.9**
TFWDBR model with interactive blocks.

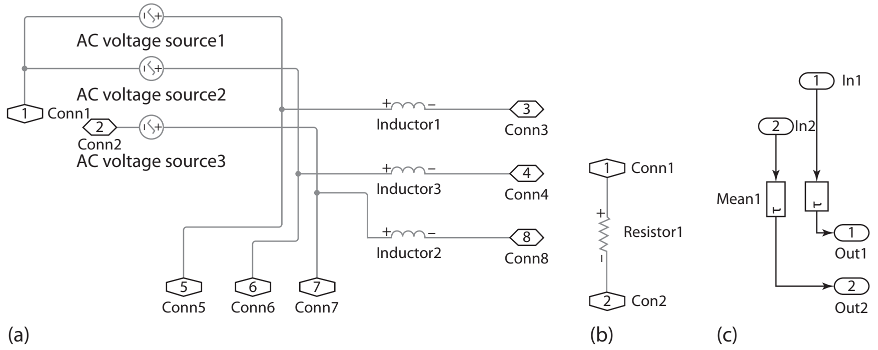

AC voltage source1
AC voltage source2
AC voltage source3
1 Conn1
2 Conn2
+ Inductor1 −
3 Conn3
+ Inductor3 −
4 Conn4
+ Inductor2 −
8 Conn8
5 Conn5
6 Conn6
7 Conn7
(a)
1 Conn1
+ Resistor1 −
2 Con2
(b)
1 In1
2 In2
Mean1
1 Out1
2 Out2
(c)

**FIGURE 10.10**
(a) Three-phase AC voltage source with source inductance. (b) R load. (c) Measurements unit.

is shown in Figure 10.17 with interactive blocks [6,7]. The subsystems are shown in Figure 10.18a,b. The simulation of this buck converter is carried out for the parameters shown in Table 5.1. The simulation results are shown in Figures 10.19 and 10.20 for CCM and DCM, respectively. The simulation results for both cases are tabulated in Table 10.5. Comparison of the results shown in Table 10.5 with Tables 5.2 and 5.3 reveals that they almost agree. The discrepancies are minor. In this model, the semiconductor switch has a forward voltage drop and on resistance, whereas in the system model of the buck converter, the switch is ideal.

## 10.4.2 Boost Converter

The analysis of the boost converter in CCM and DCM is shown in Sections 5.5 and 5.6. The data shown in Table 5.4 are used here for this model. Component-level model simulation was carried out for both CCM and DCM

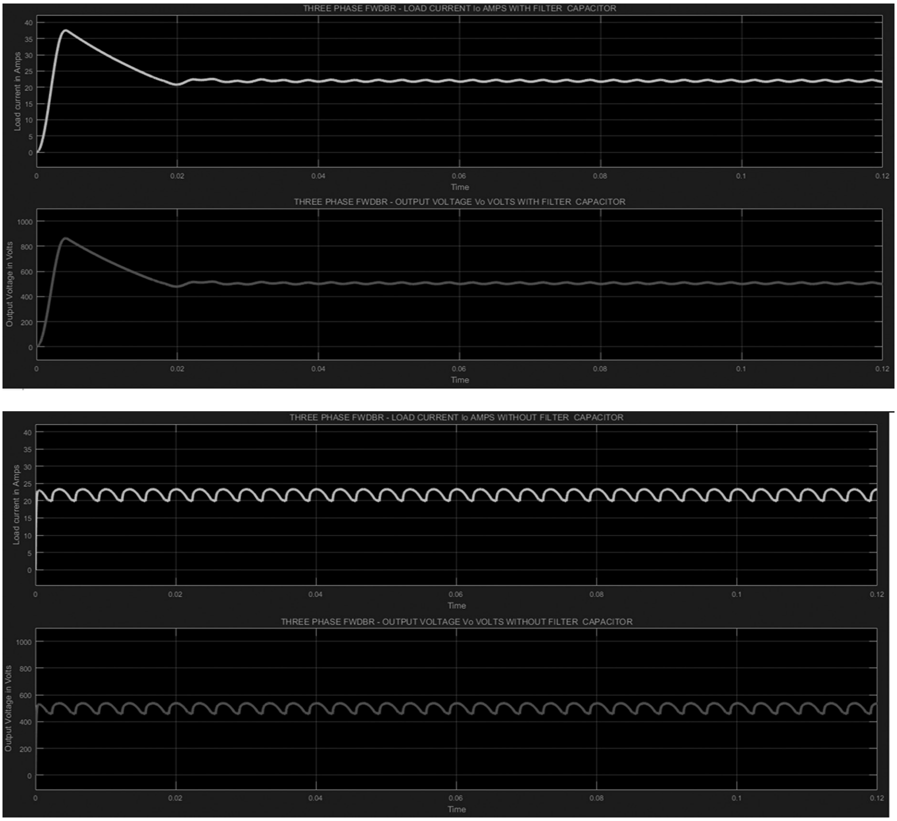


**FIGURE 10.11**
TFWDBR: simulation results. (a) With capacitor filter. (b) Without filter capacitor.

**TABLE 10.3**
Three-Phase FWDBR Simulation Results

| Sl. No. | Average Load Voltage (V) | Average Load Current (A) | Remarks |
|---|---|---|---|
| 1 | 506.7 | 22.03 | No filter capacitor |
| 2 | 505.4 | 21.97 | With filter capacitor of 0.0011 F |

and the simulation results obtained are compared with those presented in Section 5.7.1.

This model of the boost converter with interactive blocks using semiconductor switches and passive components is shown in Figure 10.21, and the subsystems of this model are shown in Figure 10.22 [6,7]. Simulation results of this model for CCM and DCM operation are shown in Figures 10.23 and 10.24, respectively. Simulation results are tabulated in Table 10.6.

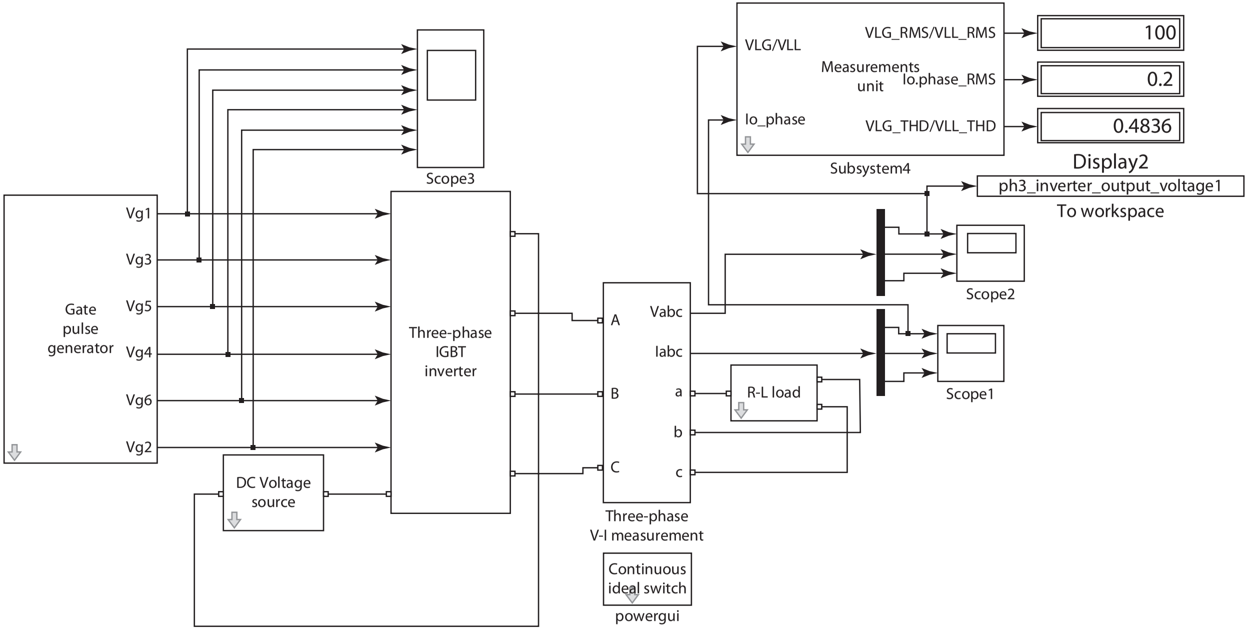
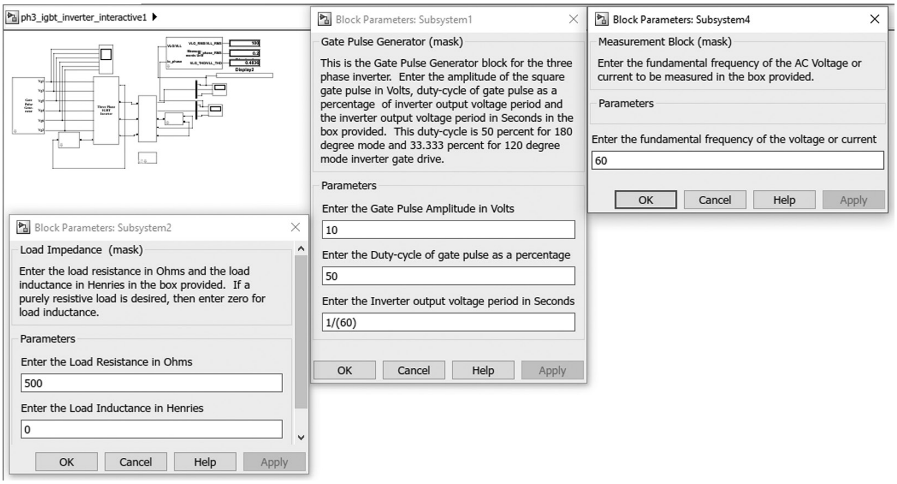

Scope3
Gate
pulse
generator
Vg1
Vg3
Vg5
Vg4
Vg6
Vg2
Three-phase
IGBT
inverter
DC Voltage
source
A
B
C
Vabc
Iabc
a
b
c
Three-phase
V-I measurement
Continuous
ideal switch
powergui
R-L load
VLG/VLL
Io_phase
Measurements
unit
VLG_RMS/VLL_RMS
Io.phase_RMS
VLG_THD/VLL_THD
Subsystem4
100
0.2
0.4836
Display2
ph3_inverter_output_voltage1
To workspace
Scope2
Scope1

**FIGURE 10.12**
Three-phase inverter model.



Block Parameters: Subsystem1

Gate Pulse Generator (mask)

This is the Gate Pulse Generator block for the three phase inverter. Enter the amplitude of the square gate pulse in Volts, duty-cycle of gate pulse as a percentage of inverter output voltage period and the inverter output voltage period in Seconds in the box provided. This duty-cycle is 50 percent for 180 degree mode and 33.333 percent for 120 degree mode inverter gate drive.

Parameters

Enter the Gate Pulse Amplitude in Volts: 10

Enter the Duty-cycle of gate pulse as a percentage: 50

Enter the Inverter output voltage period in Seconds: 1/(60)

Block Parameters: Subsystem4

Measurement Block (mask)

Enter the fundamental frequency of the AC Voltage or current to be measured in the box provided.

Parameters

Enter the fundamental frequency of the voltage or current: 60

Block Parameters: Subsystem2

Load Impedance (mask)

Enter the load resistance in Ohms and the load inductance in Henries in the box provided. If a purely resistive load is desired, then enter zero for load inductance.

Parameters

Enter the Load Resistance in Ohms: 500

Enter the Load Inductance in Henries: 0

**FIGURE 10.13**
Three-phase inverter model with interactive blocks.

The simulation results in Table 10.6 almost agree with the results presented in Tables 5.5 and 5.6. In this model, the semiconductor components have forward voltage and on resistance and are not ideal.

### 10.4.3 Buck–Boost Converter

Analysis of the buck–boost converter in CCM and DCM is shown in Sections 5.8 and 5.9. The data shown in Table 5.7 are used here for the circuit model. A component-level model simulation was carried out for both CCM and DCM and the simulation results obtained are compared with those presented in Section 5.10.1.

This model of the buck–boost converter with interactive blocks is shown in Figure 10.25, and the model subsystems are shown in Figure 10.26 [6,7]. The simulation results of this model for CCM and DCM operation are shown in Figures 10.27 and 10.28. The results are tabulated in Table 10.7. Comparison of the circuit model simulation results in Table 10.7 with Tables 5.8 and 5.9 reveals that the results agree closely. As mentioned, the semiconductor components in the circuit model are not ideal.

## 10.5 AC to AC Converter

The component-level models for the two three-phase AC controllers discussed in Chapter 6 is presented in this section. The first one is the three-phase back-to-back connected thyristor AC to AC controller connected

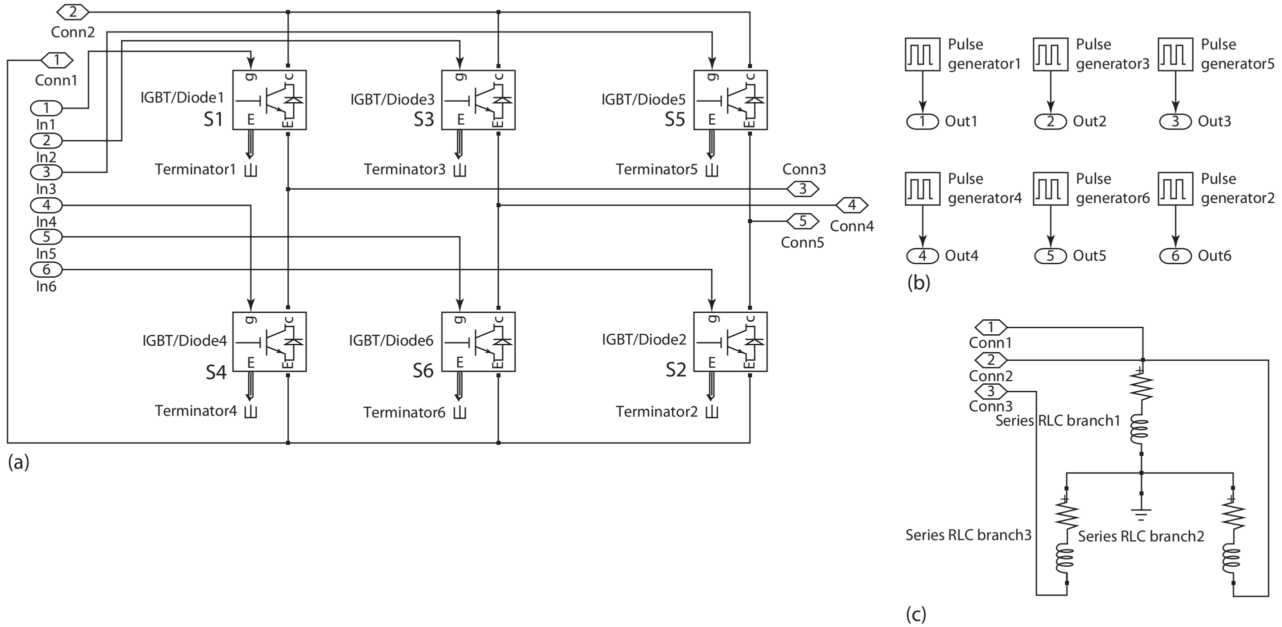
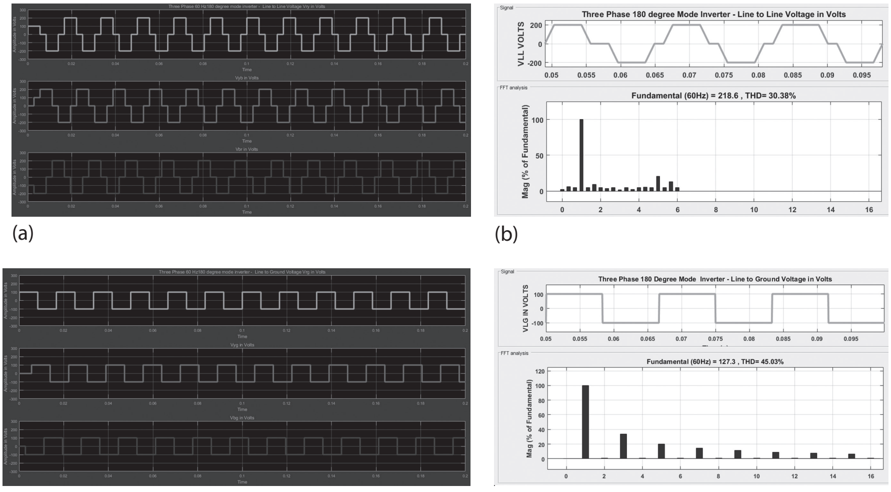

Conn2
Conn1
In1
In2
In3
In4
In5
In6
IGBT/Diode1
S1
Terminator1
IGBT/Diode3
S3
Terminator3
IGBT/Diode5
S5
Terminator5
IGBT/Diode4
S4
Terminator4
IGBT/Diode6
S6
Terminator6
IGBT/Diode2
S2
Terminator2
g
c
E
Conn3
Conn4
Conn5
(a)
Pulse generator1
Pulse generator3
Pulse generator5
Out1
Out2
Out3
Pulse generator4
Pulse generator6
Pulse generator2
Out4
Out5
Out6
(b)
Conn1
Conn2
Conn3
Series RLC branch1
Series RLC branch3
Series RLC branch2
(c)

**FIGURE 10.14**
Three-phase 180° mode inverter model subsystems.



(a) (b)

(c) (d)

**FIGURE 10.15**
Three-phase 180° mode inverter. (a) Line-to-line voltages. (b) Line-to-line voltage harmonic spectrum. (c) Line-to-ground voltage. (d) Line-to-ground voltage harmonic spectrum.

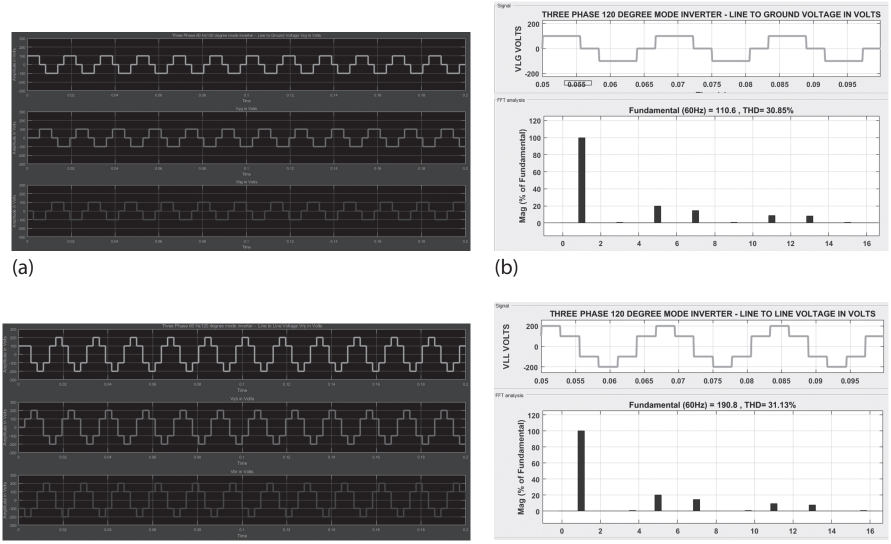
to a star-connected resistive load with isolated neutral. The second one is the three-phase back-to-back connected thyristor AC controller in series with resistive load in delta [2–5,8].

### 10.5.1 Three-Phase Thyristor AC to AC Controller Connected to Resistive Load in Star

The component-level model of the back-to-back connected thyristor AC to AC controller in series with star-connected resistive load is shown in Figure 10.29 [2–5,8]. The interactive blocks of this circuit model and its subsystems are shown in Figures 10.30 and 10.31, respectively. The model parameters are shown in Table 6.1. The model simulation results are shown in Figures 10.32a,b and 10.33a,b for a firing angle α of π/6 and 2π/3 rad. The

**TABLE 10.4**
Three-Phase (a) 180° and (b) 120° Mode Inverter: Simulation Results

| Sl. No. | Frequency (Hz) | DC Link Voltage (V) | THD of $V_{LL}$ (Per Unit) | RMS of $V_{LL}$ (V) | THD of $V_{LG}$ (Per Unit) | RMS of $V_{LG}$ (V) |
|---|---|---|---|---|---|---|
| (a) | | | | | | |
| 1 | 60 | 200 | 0.3115 | 163.3 | 0.45 | 100 |
| (b) | | | | | | |
| 1 | 60 | 200 | 0.3115 | 141.4 | 0.3115 | 81.65 |

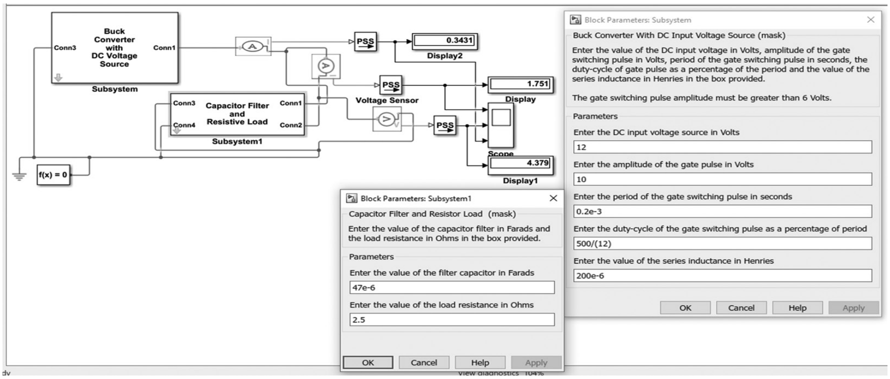


(a) (b) (c) (d)

**FIGURE 10.16**
Three-phase 120° mode inverter. (a) Line-to-ground voltage. (b) Line-to-ground voltage harmonic spectrum. (c) Line-to-line voltage. (d) Line-to-line voltage harmonic spectrum.

**TABLE 10.5**
Buck Converter Simulation Results

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | 4.74 | 0.343 | 3.516 | 1.896 | CCM |
| 2 | 7.112 | 0 | 8.159 | 2.845 | DCM |


Buck Converter with DC Voltage Source
Conn3
Conn1
Subsystem
Capacitor Filter and Resistive Load
Conn3
Conn4
Conn1
Conn2
Subsystem1
f(x) = 0
PSS
0.3431
Display2
Voltage Sensor
1.751
Display
Scope
4.379
Display1
OK
Cancel
Help
Apply

Block Parameters: Subsystem

Buck Converter With DC Input Voltage Source (mask)

Enter the value of the DC input voltage in Volts, amplitude of the gate switching pulse in Volts, period of the gate switching pulse in seconds, the duty-cycle of gate pulse as a percentage of the period and the value of the series inductance in Henries in the box provided.

The gate switching pulse amplitude must be greater than 6 Volts.

Parameters

Enter the DC input voltage source in Volts: 12

Enter the amplitude of the gate pulse in Volts: 10

Enter the period of the gate switching pulse in seconds: 0.2e-3

Enter the duty-cycle of the gate switching pulse as a percentage of period: 500/(12)

Enter the value of the series inductance in Henries: 200e-6

Block Parameters: Subsystem1

Capacitor Filter and Resistor Load (mask)

Enter the value of the capacitor filter in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the value of the filter capacitor in Farads: 47e-6

Enter the value of the load resistance in Ohms: 2.5

**FIGURE 10.17**
Buck converter model.

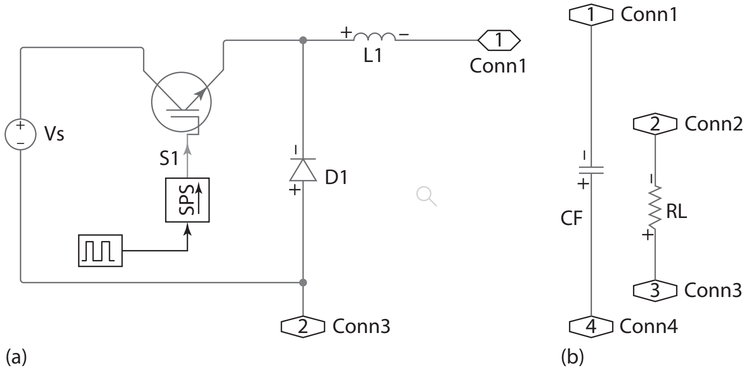

Vs
S1
SPS
D1
L1
1
Conn1
2
Conn3
(a)
1
Conn1
2
Conn2
CF
RL
3
Conn3
4
Conn4
(b)

**FIGURE 10.18**
Buck converter model subsystems. (a) Buck converter. (b) Capacitor filter and resistance load.

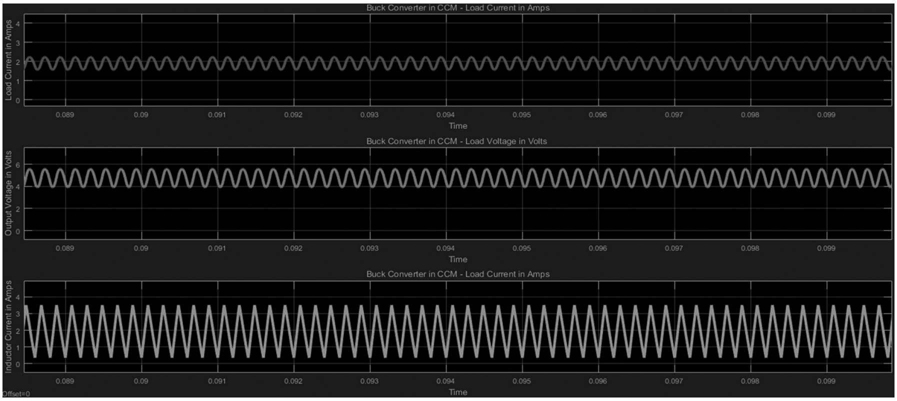


**FIGURE 10.19**
Buck converter in CCM: simulation results.

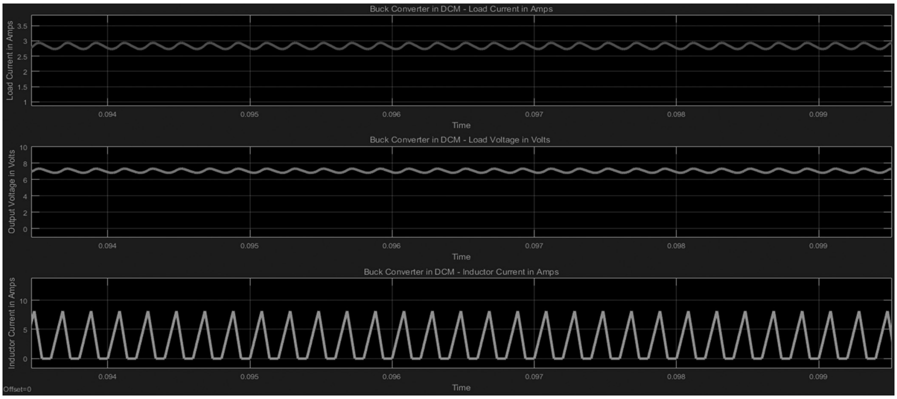
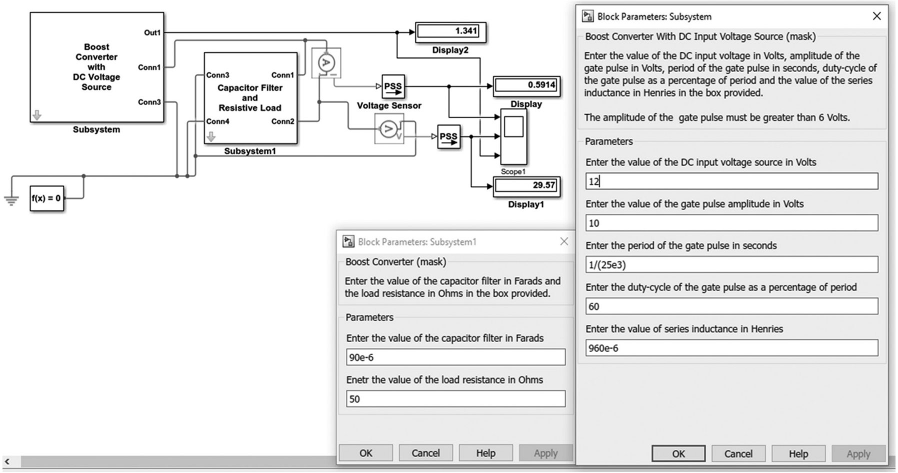


**FIGURE 10.20**
Buck converter in DCM: simulation results.


Boost Converter with DC Voltage Source
Out1
Conn1
Conn3
Subsystem
Conn3
Conn1
Capacitor Filter and Resistive Load
Conn4
Conn2
Subsystem1
f(x) = 0
PSS
Voltage Sensor
PSS
1.341
Display2
0.5914
Display
Scope1
29.57
Display1
OK
Cancel
Help
Apply
OK
Cancel
Help
Apply

Block Parameters: Subsystem1

Boost Converter (mask)

Enter the value of the capacitor filter in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the value of the capacitor filter in Farads

90e-6

Enetr the value of the load resistance in Ohms

50

Block Parameters: Subsystem

Boost Converter With DC Input Voltage Source (mask)

Enter the value of the DC input voltage in Volts, amplitude of the gate pulse in Volts, period of the gate pulse in seconds, duty-cycle of the gate pulse as a percentage of period and the value of the series inductance in Henries in the box provided.

The amplitude of the gate pulse must be greater than 6 Volts.

Parameters

Enter the value of the DC input voltage source in Volts

12

Enter the value of the gate pulse amplitude in Volts

10

Enter the period of the gate pulse in seconds

1/(25e3)

Enter the duty-cycle of the gate pulse as a percentage of period

60

Enter the value of series inductance in Henries

960e-6

**FIGURE 10.21**
Boost converter model.

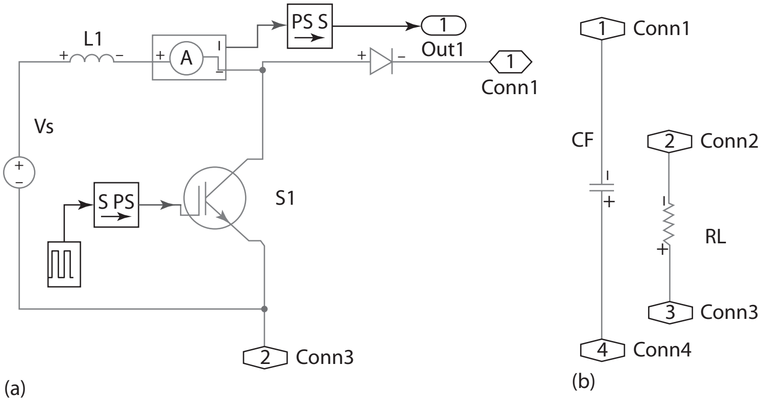

L1
+
−
+
A
PS S
1
Out1
+
−
1
Conn1
Vs
+
−
S PS
S1
2
Conn3
(a)
1
Conn1
CF
+
2
Conn2
RL
+
3
Conn3
4
Conn4
(b)

**FIGURE 10.22**
Boost converter model subsystems.

simulation results are tabulated in Table 10.8 for all values of the firing angle. Comparison of values in Table 10.8 with Tables 6.2 and 6.3 reveals that the error is small for α in the range from π/6 to π/2 rad and is large for 2π/3 rad.

### 10.5.2 Three-Phase Thyristor AC to AC Controller in Series with Resistive Load in Delta

The component-level model of the three-phase thyristor AC to AC controller in series with resistive load in delta is shown in Figure 10.34 [2–5,8]. The interactive blocks of this model and its subsystems are shown in Figures 10.35 and 10.36, respectively. The model parameters are given in Table 6.4. The

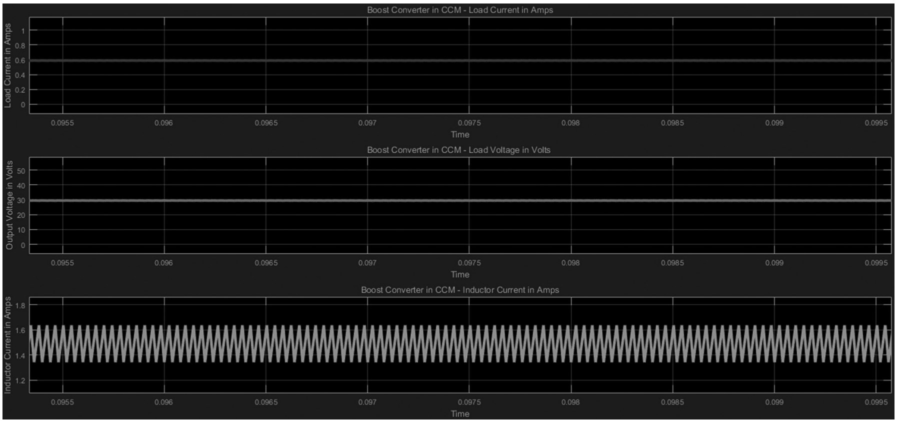


**FIGURE 10.23**
Boost converter in CCM: simulation results.

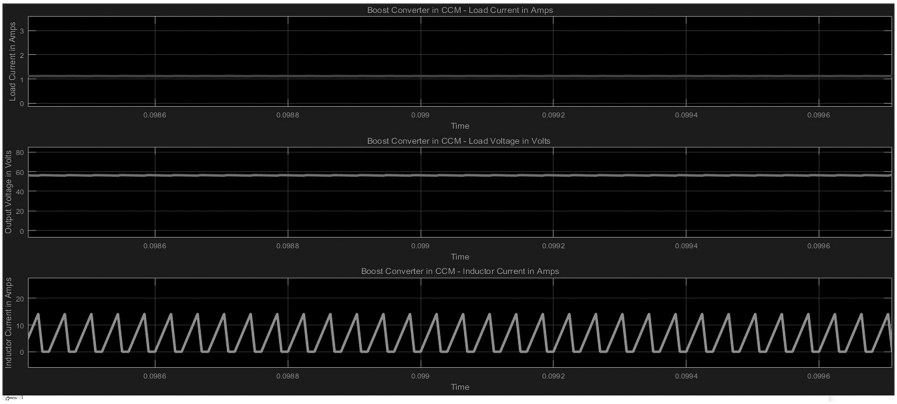
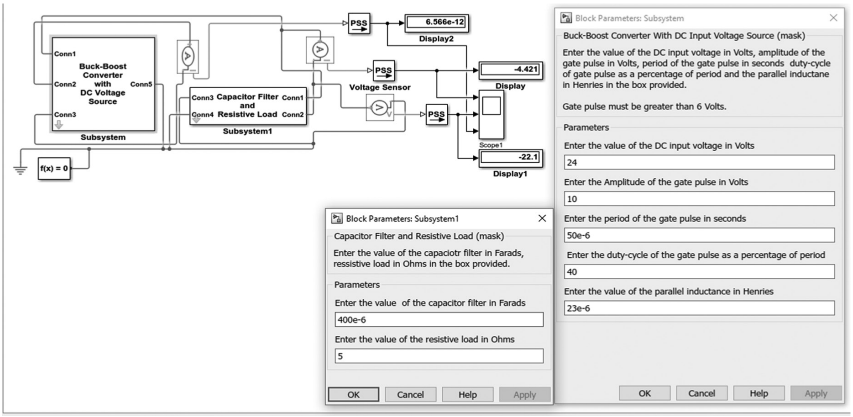


**FIGURE 10.24**
Boost converter in DCM: simulation results.

**TABLE 10.6**

Boost Converter: Simulation Results

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | 29.5 | 1.341 | 1.636 | 0.59 | CCM |
| 2 | 56.3 | 0 | 14.16 | 1.126 | DCM |


Conn1
Buck-Boost Converter with DC Voltage Source
Conn2
Conn5
Conn3
Subsystem
Conn3 Capacitor Filter and Resistive Load Conn1
Conn4 Conn2
Subsystem1
f(x) = 0
PSS
6.566e-12
Display2
PSS
Voltage Sensor
-4.421
Display
PSS
Scope1
-22.1
Display1
OK
Cancel
Help
Apply

Block Parameters: Subsystem

Buck-Boost Converter With DC Input Voltage Source (mask)

Enter the value of the DC input voltage in Volts, amplitude of the gate pulse in Volts, period of the gate pulse in seconds duty-cycle of gate pulse as a percentage of period and the parallel inductane in Henries in the box provided.

Gate pulse must be greater than 6 Volts.

Parameters

Enter the value of the DC input voltage in Volts: 24

Enter the Amplitude of the gate pulse in Volts: 10

Enter the period of the gate pulse in seconds: 50e-6

Enter the duty-cycle of the gate pulse as a percentage of period: 40

Enter the value of the parallel inductance in Henries: 23e-6

Block Parameters: Subsystem1

Capacitor Filter and Resistive Load (mask)

Enter the value of the capaciotr filter in Farads, ressistive load in Ohms in the box provided.

Parameters

Enter the value of the capacitor filter in Farads: 400e-6

Enter the value of the resistive load in Ohms: 5

**FIGURE 10.25**
Buck–boost converter model.

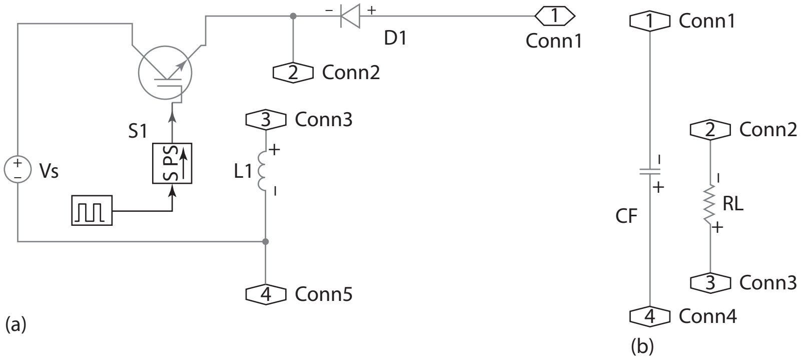

D1
1
Conn1
2
Conn2
S1
3
Conn3
Vs
S PS
L1
4
Conn5
(a)
1
Conn1
2
Conn2
CF
RL
3
Conn3
4
Conn4
(b)

**FIGURE 10.26**
Buck–boost converter model subsystems.

simulation results are given in Figures 10.37 and 10.38, respectively. The simulation results are tabulated in Table 10.9. Comparison of the results in Table 10.9 with Tables 6.5 and 6.6 reveals an error in the circuit model. Compared with the calculated values in Table 6.6, the percentage error for π/6 rad is 9.26%, for π/4 rad it is 14.6% and so on. For π rad, the output voltage is 41 mV, whereas it should be zero. Here, non-ideal semiconductor components are used in the model that have forward voltage and on resistance.

## 10.6 Switched Mode Power Supply Using Buck Converter

The system model and simulation of a switched mode power supply (SMPS) using a buck converter with and without using a proportional–integral (PI) controller is presented in Chapter 7. Here, the component-level model of the

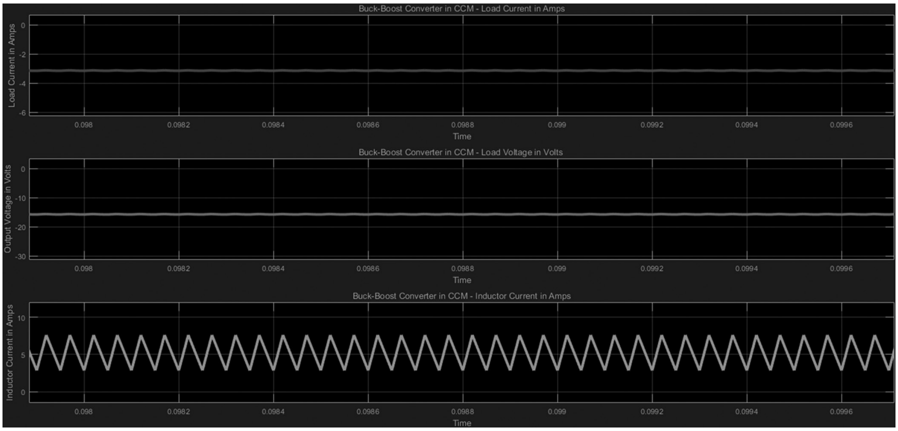


**FIGURE 10.27**
Buck–boost converter in CCM: simulation results.

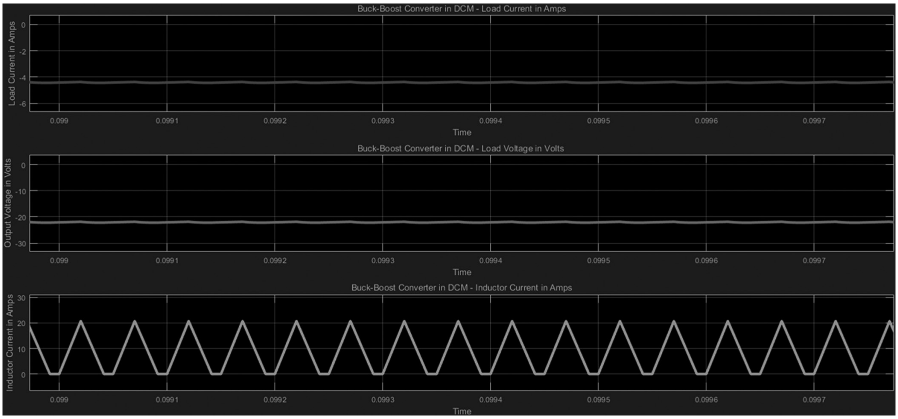


**FIGURE 10.28**
Buck–boost converter in DCM: simulation results.

**TABLE 10.7**
Buck–Boost Converter: Simulation Results

| Sl. No. | Output Voltage $V_O$ (V) | Minimum Inductor Current (A) | Maximum Inductor Current (A) | Load Current (A) | Duty Cycle | Remarks |
|---|---|---|---|---|---|---|
| 1 | −15.65 | 2.853 | 7.613 | 3.13 | 0.4 | CCM |
| 2 | −22.13 | 0 | 20.69 | 4.426 | 0.4 | DCM |

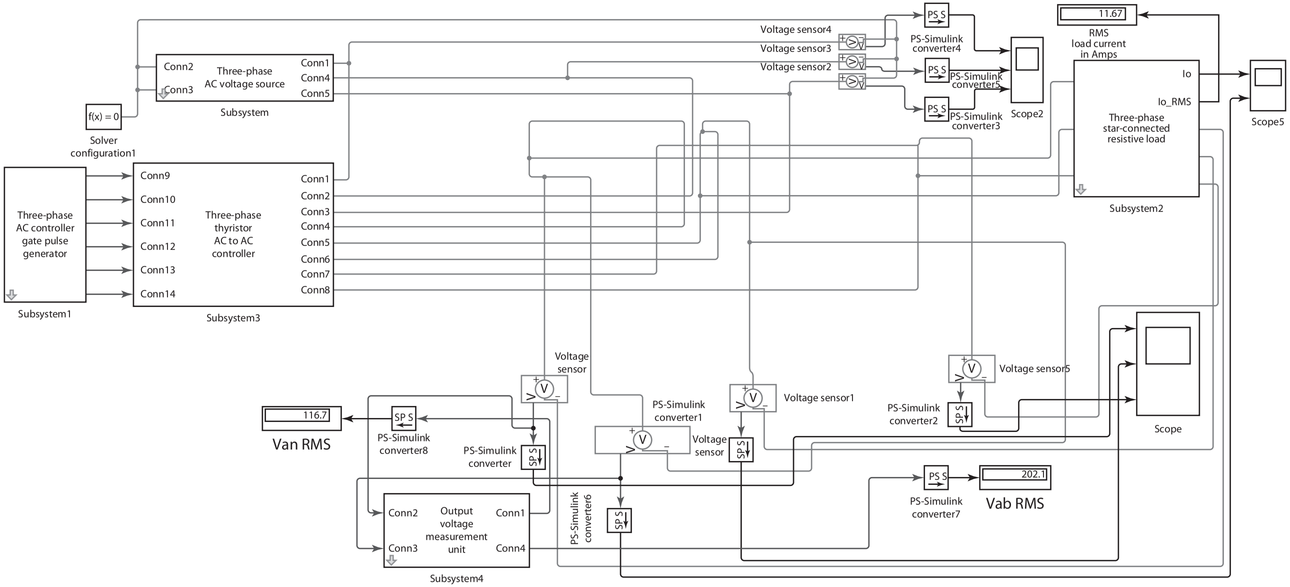
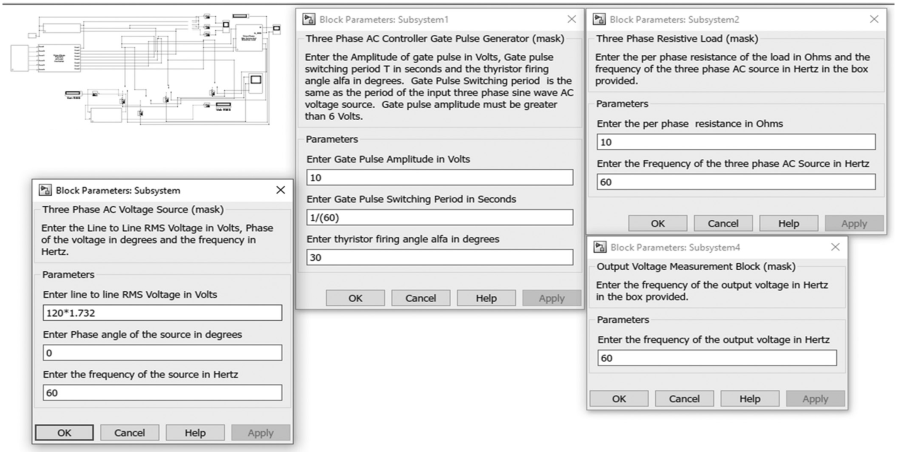

Voltage sensor4
Voltage sensor3
Voltage sensor2
PS S
PS-Simulink converter4
PS-Simulink converter5
PS-Simulink converter3
Scope2
11.67
RMS load current in Amps
Io
Io_RMS
Three-phase star-connected resistive load
Subsystem2
Scope5
Conn2
Conn3
Three-phase AC voltage source
Conn1
Conn4
Conn5
Subsystem
f(x) = 0
Solver configuration1
Three-phase AC controller gate pulse generator
Subsystem1
Conn9
Conn10
Conn11
Conn12
Conn13
Conn14
Three-phase thyristor AC to AC controller
Conn1
Conn2
Conn3
Conn4
Conn5
Conn6
Conn7
Conn8
Subsystem3
Voltage sensor
Voltage sensor1
Voltage sensor5
PS-Simulink converter1
PS-Simulink converter2
Scope
SP S
116.7
Van RMS
PS-Simulink converter8
PS-Simulink converter
Voltage sensor
PS-Simulink converter6
Conn2
Conn3
Output voltage measurement unit
Conn1
Conn4
Subsystem4
PS-Simulink converter7
202.1
Vab RMS

**FIGURE 10.29**
Three-phase thyristor AC to AC controller in series with star-connected resistive load.



Block Parameters: Subsystem

Three Phase AC Voltage Source (mask)

Enter the Line to Line RMS Voltage in Volts, Phase of the voltage in degrees and the frequency in Hertz.

Parameters

Enter line to line RMS Voltage in Volts: 120*1.732

Enter Phase angle of the source in degrees: 0

Enter the frequency of the source in Hertz: 60

Block Parameters: Subsystem1

Three Phase AC Controller Gate Pulse Generator (mask)

Enter the Amplitude of gate pulse in Volts, Gate pulse switching period T in seconds and the thyristor firing angle alfa in degrees. Gate Pulse Switching period is the same as the period of the input three phase sine wave AC voltage source. Gate pulse amplitude must be greater than 6 Volts.

Parameters

Enter Gate Pulse Amplitude in Volts: 10

Enter Gate Pulse Switching Period in Seconds: 1/(60)

Enter thyristor firing angle alfa in degrees: 30

Block Parameters: Subsystem2

Three Phase Resistive Load (mask)

Enter the per phase resistance of the load in Ohms and the frequency of the three phase AC source in Hertz in the box provided.

Parameters

Enter the per phase resistance in Ohms: 10

Enter the Frequency of the three phase AC Source in Hertz: 60

Block Parameters: Subsystem4

Output Voltage Measurement Block (mask)

Enter the frequency of the output voltage in Hertz in the box provided.

Parameters

Enter the frequency of the output voltage in Hertz: 60

**FIGURE 10.30**
Three-phase thyristor AC to AC controller in series with star-connected resistive load with interactive blocks.

same SMPS is developed using semiconductor and passive components; a simulation was carried out and compared with that presented in Section 7.3 [6,7].

This model of the buck converter SMPS with and without PI controller is shown in Figure 10.39. The interactive blocks of this model are shown in Figure 10.40 and subsystems are shown in Figure 10.41.

The relevant data are entered in the box shown in the interactive blocks in Figure 10.40. In Figure 10.41, subsystems A, C and D form the buck converter, capacitor filter and load resistor and the output voltage and current measurement unit. Figure 10.41b is the gate pulse generating unit. The output voltage across the load resistor is multiplied by a potentiometer constant using a gain pot. The output of the gain pot is compared with a reference voltage $v_{ref}$ in an error detector unit that gives the error output voltage $V_{ERR}$. The triangle carrier generator generates a triangle carrier with a positive and negative peak of +1 and –1 V and frequency corresponding to the switching frequency of the SMPS. The triangle carrier is multiplied by a gain multiplier constant *gm* to obtain the triangle carrier with required amplitude. The required amplitude of the triangle carrier is that which gives normal output voltage of 9 V DC with a normal input voltage of 15 V DC. The error output $V_{ERR}$ is compared with the triangle carrier either directly or through the PI controller in a comparator and the resulting output of the comparator is the gate pulse for the SMPS. Switch *SS*1 selects $V_{ERR}$ directly or through the PI controller.

The component model simulation of the buck SMPS is carried out using data given in Table 7.1. The model simulation results are shown in Figure 10.42a–c for the buck SMPS without the PI controller and in Figure 10.43a–c for the

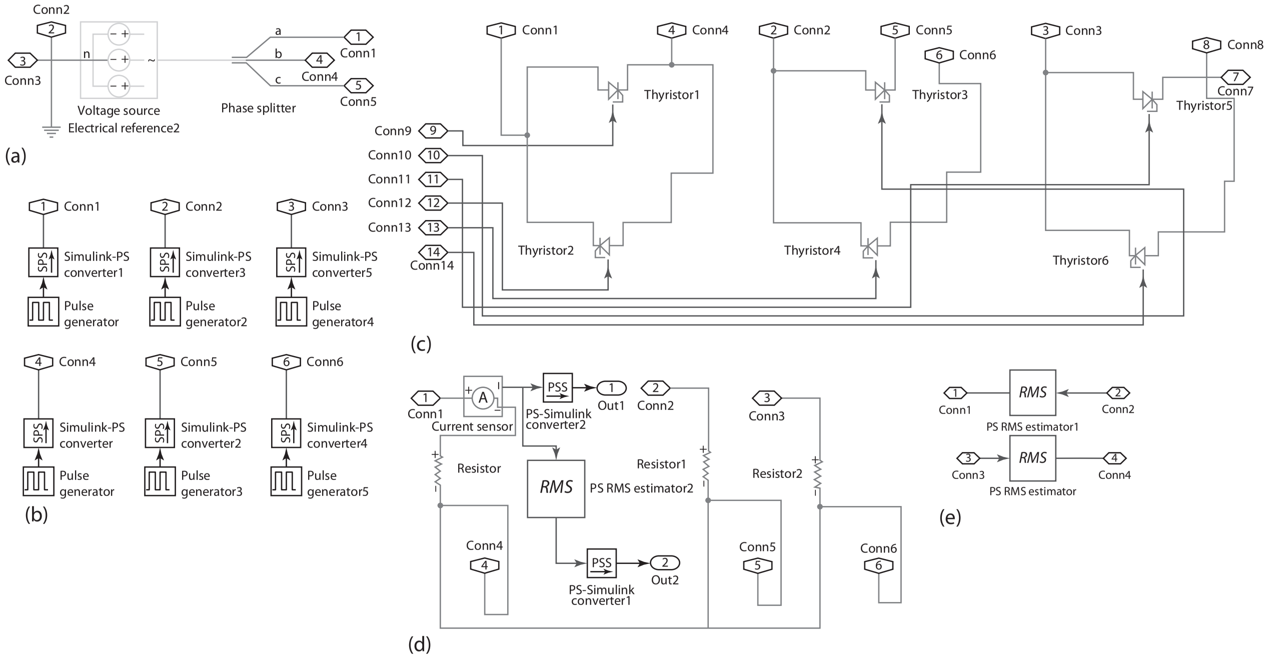
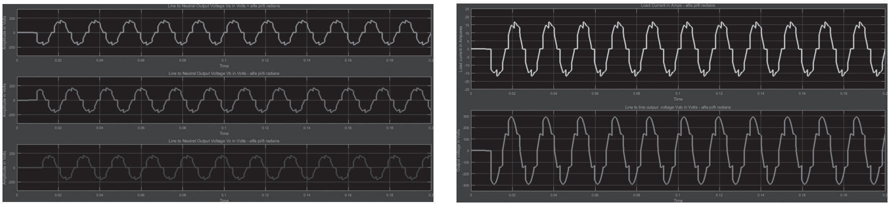
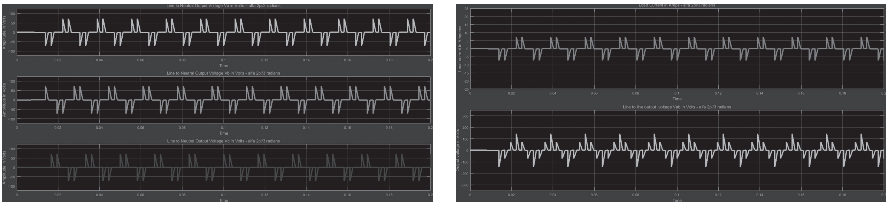

Conn2
2
3
Conn3
n
~
Voltage source
Electrical reference2
a
b
c
Phase splitter
1
Conn1
4
Conn4
5
Conn5
(a)
Conn1
Conn2
Conn3
Simulink-PS converter1
Simulink-PS converter3
Simulink-PS converter5
Pulse generator
Pulse generator2
Pulse generator4
Conn4
Conn5
Conn6
Simulink-PS converter
Simulink-PS converter2
Simulink-PS converter4
Pulse generator
Pulse generator3
Pulse generator5
(b)
Conn9
Conn10
Conn11
Conn12
Conn13
Conn14
Conn1
Conn4
Conn2
Conn5
Conn6
Conn3
Conn8
Conn7
Thyristor1
Thyristor2
Thyristor3
Thyristor4
Thyristor5
Thyristor6
(c)
Conn1
Current sensor
PS-Simulink converter2
Out1
Conn2
Conn3
Resistor
Resistor1
Resistor2
RMS
PS RMS estimator2
PS-Simulink converter1
Out2
Conn4
Conn5
Conn6
(d)
RMS
Conn1
Conn2
PS RMS estimator1
RMS
Conn3
Conn4
PS RMS estimator
(e)

**FIGURE 10.31**
Three-phase thyristor AC to AC controller in series with star-connected resistive load model subsystems.



(a) (b)

**FIGURE 10.32**
Three-phase thyristor AC to AC controller connected to (a) star-connected load and (b) star-connected resistive load: simulation results for α = π/6 rad.



(a) (b)

**FIGURE 10.33**
Three-phase thyristor AC to AC controller connected to (a) star-connected resistive load and (b) star-connected load: simulation results for α = 2π/3 rad.

case with the PI controller. The simulation results for the buck SMPS without the PI controller and those for the case with the PI controller are tabulated in Table 10.10. The conclusions drawn from the results for the buck SMPS are given as follows:

- The change in output voltage for a given change in input voltage or regulation is slightly higher for the case with the PI controller than without the PI controller.

**TABLE 10.8**
Three-Phase Thyristor AC Controller Connected to Resistive Star-Connected Load: Simulation Results

| Sl. No. | Line-to-Neutral Voltage (V) | Frequency (Hz) | Firing Angle α (rad) | Per Phase Load Resistance (Ω) | RMS Line-to-Neutral Load Voltage (V) | RMS Load Current (A) |
|---|---|---|---|---|---|---|
| 1 | 120 | 60 | π/6 | 10 | 116.2 | 11.62 |
| 2 | 120 | 60 | π/4 | 10 | 110.8 | 11.08 |
| 3 | 120 | 60 | π/3 | 10 | 100.8 | 10.08 |
| 4 | 120 | 60 | π/2 | 10 | 64.39 | 6.439 |
| 5 | 120 | 60 | 2π/3 | 10 | 24.55 | 2.455 |

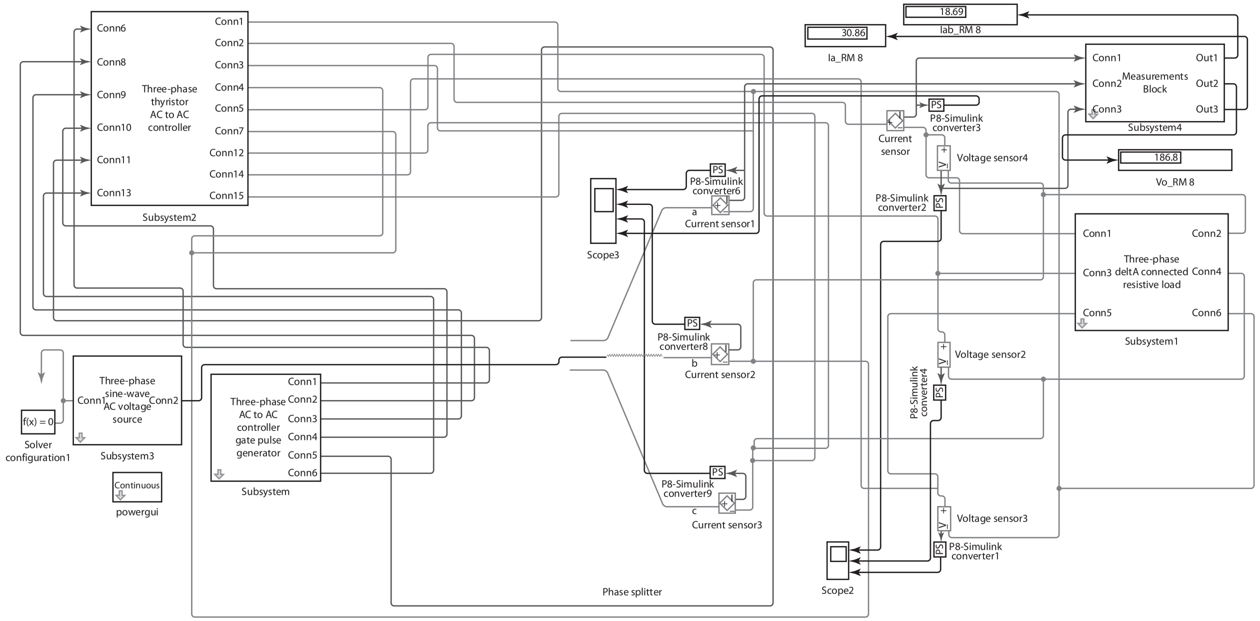

Conn6
Conn8
Conn9
Conn10
Conn11
Conn13
Three-phase thyristor AC to AC controller
Conn1
Conn2
Conn3
Conn4
Conn5
Conn7
Conn12
Conn14
Conn15
Subsystem2
f(x) = 0
Solver configuration1
Three-phase sine-wave AC voltage source
Conn1
Conn2
Subsystem3
Continuous
powergui
Three-phase AC to AC controller gate pulse generator
Conn1
Conn2
Conn3
Conn4
Conn5
Conn6
Subsystem
Scope3
PS
P8-Simulink converter6
a
Current sensor1
PS
P8-Simulink converter8
b
Current sensor2
PS
P8-Simulink converter9
c
Current sensor3
Phase splitter
30.86
Ia_RM 8
18.69
Iab_RM 8
Current sensor
PS
P8-Simulink converter3
Voltage sensor4
P8-Simulink converter2
PS
Conn1
Conn2
Conn3
Measurements Block
Out1
Out2
Out3
Subsystem4
186.8
Vo_RM 8
Conn1
Conn2
Three-phase deltA connected resistive load
Conn3
Conn4
Conn5
Conn6
Subsystem1
Voltage sensor2
P8-Simulink converter4
PS
Voltage sensor3
PS
P8-Simulink converter1
Scope2

**FIGURE 10.34**
Three-phase thyristor AC to AC controller in series with resistive load in delta.

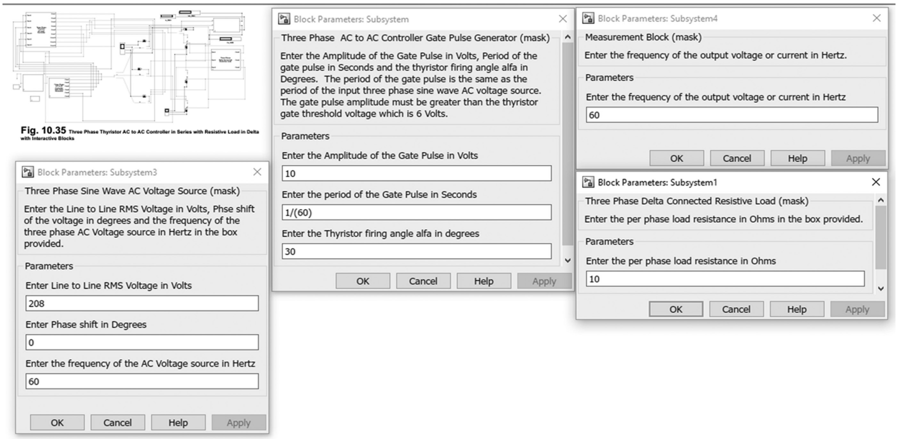


Fig. 10.35 Three Phase Thyristor AC to AC Controller in Series with Resistive Load in Delta with Interactive Blocks

Block Parameters: Subsystem3

Three Phase Sine Wave AC Voltage Source (mask)

Enter the Line to Line RMS Voltage in Volts, Phse shift of the voltage in degrees and the frequency of the three phase AC Voltage source in Hertz in the box provided.

Parameters

Enter Line to Line RMS Voltage in Volts: 208

Enter Phase shift in Degrees: 0

Enter the frequency of the AC Voltage source in Hertz: 60

Block Parameters: Subsystem

Three Phase AC to AC Controller Gate Pulse Generator (mask)

Enter the Amplitude of the Gate Pulse in Volts, Period of the gate pulse in Seconds and the thyristor firing angle alfa in Degrees. The period of the gate pulse is the same as the period of the input three phase sine wave AC voltage source. The gate pulse amplitude must be greater than the thyristor gate threshold voltage which is 6 Volts.

Parameters

Enter the Amplitude of the Gate Pulse in Volts: 10

Enter the period of the Gate Pulse in Seconds: 1/(60)

Enter the Thyristor firing angle alfa in degrees: 30

Block Parameters: Subsystem4

Measurement Block (mask)

Enter the frequency of the output voltage or current in Hertz.

Parameters

Enter the frequency of the output voltage or current in Hertz: 60

Block Parameters: Subsystem1

Three Phase Delta Connected Resistive Load (mask)

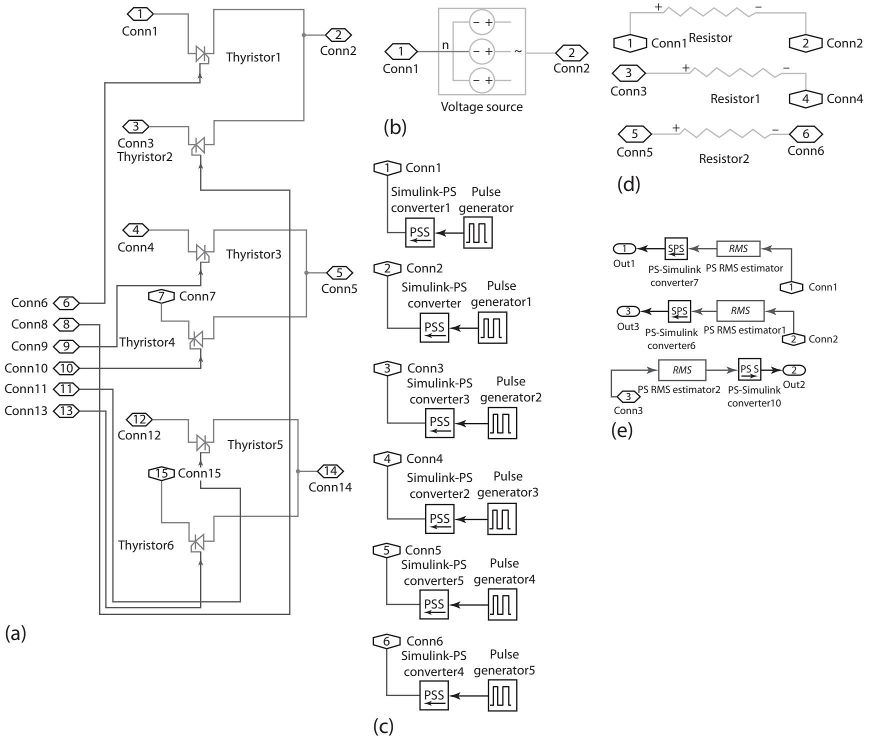
Enter the per phase load resistance in Ohms in the box provided.

Parameters

Enter the per phase load resistance in Ohms: 10

OK
Cancel
Help
Apply

**FIGURE 10.35**
Three-phase thyristor AC to AC controller in series with resistive load in delta with interactive blocks.



1
Conn1
Thyristor1
2
Conn2
3
Conn3
Thyristor2
4
Conn4
Thyristor3
5
Conn5
7
Conn7
Conn6
6
Conn8
8
Conn9
9
Thyristor4
Conn10
10
Conn11
11
Conn13
13
12
Conn12
Thyristor5
15
Conn15
14
Conn14
Thyristor6
(a)
1
Conn1
n
~
2
Conn2
Voltage source
(b)
1
Conn1
Simulink-PS converter1
Pulse generator
PSS
2
Conn2
Simulink-PS converter
Pulse generator1
PSS
3
Conn3
Simulink-PS converter3
Pulse generator2
PSS
4
Conn4
Simulink-PS converter2
Pulse generator3
PSS
5
Conn5
Simulink-PS converter5
Pulse generator4
PSS
6
Conn6
Simulink-PS converter4
Pulse generator5
PSS
(c)
+
−
1
Conn1
Resistor
2
Conn2
3
Conn3
Resistor1
4
Conn4
5
Conn5
Resistor2
6
Conn6
(d)
1
Out1
SPS
PS-Simulink converter7
RMS
PS RMS estimator
1
Conn1
3
Out3
SPS
PS-Simulink converter6
RMS
PS RMS estimator1
2
Conn2
RMS
PS RMS estimator2
PS S
PS-Simulink converter10
2
Out2
3
Conn3
(e)

**FIGURE 10.36**
Three-phase thyristor AC controller in series with resistive load in delta: model subsystems.

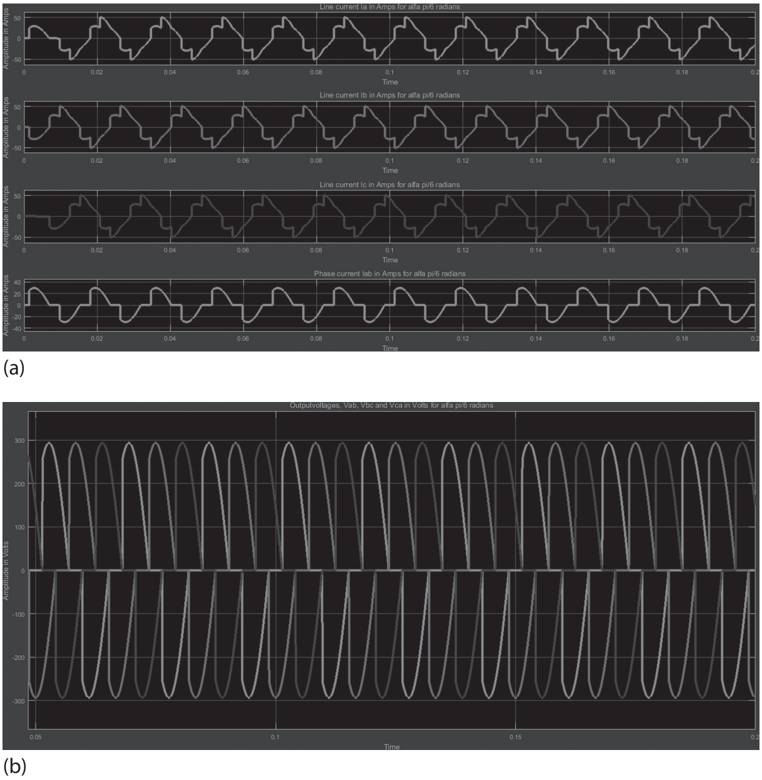
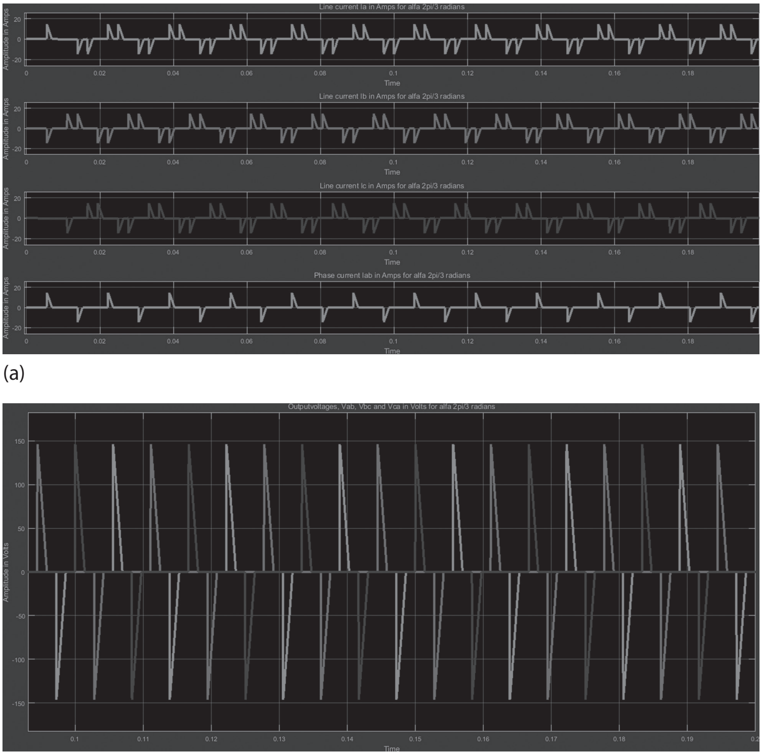


**FIGURE 10.37**
(a and b) Three-phase thyristor AC controller in series with resistive load in delta: simulation results for $\alpha = \pi/6$ rad.

- The output voltage is 9 V when the input voltage is 15 V in both cases.
- The number of initial oscillations for the first 0.01 s is nine without the PI controller and six with the PI controller.
- The initial peak overshoot was 16.25 V without the PI controller and 14.2 V with the PI controller.
- There is a reduction of peak overshoot by 2 V with the PI controller compared with the case without the PI controller.

## 10.7 Fourth-Order DC to DC Converters

The system modelling of selected fourth-order converters such as the single-ended primary inductance converter (SEPIC), quadratic boost and ultra-lift Luo converters are discussed in Chapter 8 for both CCM and DCM. In this



(a)

(b)

**FIGURE 10.38**
(a and b) Three-phase thyristor AC controller in series with resistive load in delta: simulation results for $\alpha = 2\pi/3$ rad.

**TABLE 10.9**
Three-Phase AC Controller in Series with Resistive Load in Delta: Simulation Results

| Sl. No. | RMS Line-to-Line Supply Voltage (V) | Frequency(Hz) | Firing Angle $\alpha$ (rad) | Per Phase Load Resistance (Ω) | RMS Load Voltage $V_O$ (V) | RMS Load Current $I_{ab}$ (A) |
|---|---|---|---|---|---|---|
| 1 | 208 | 60 | $\pi/6$ | 10 | 186.0 | 18.6 |
| 2 | 208 | 60 | $\pi/4$ | 10 | 168.8 | 16.88 |
| 3 | 208 | 60 | $\pi/3$ | 10 | 146.6 | 14.66 |
| 4 | 208 | 60 | $\pi/2$ | 10 | 91.55 | 9.1555 |
| 5 | 208 | 60 | $2\pi/3$ | 10 | 35.03 | 3.503 |
| 6 | 208 | 60 | $\pi$ | 10 | 0.041 | 0.0041 |

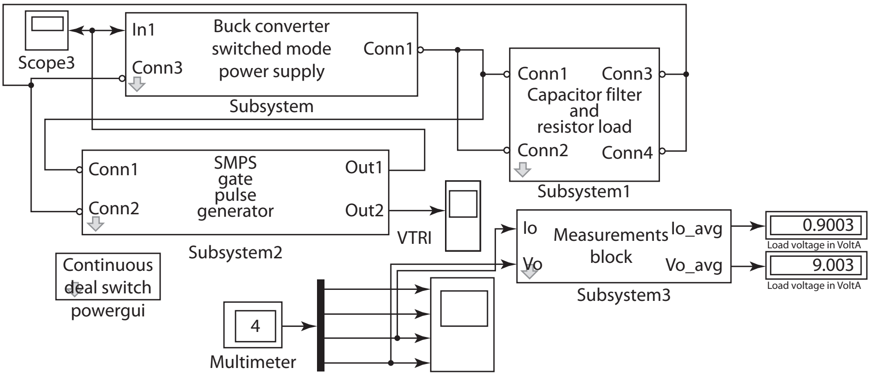
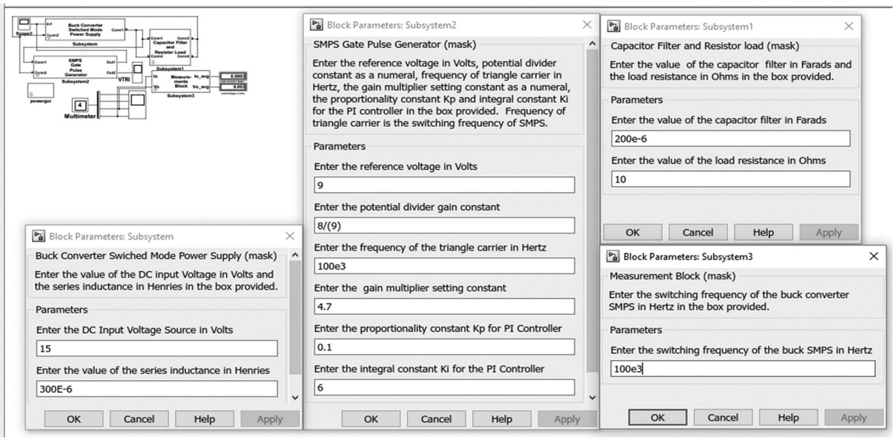

Scope3
In1
Conn3
Buck converter
switched mode
power supply
Conn1
Subsystem
Conn1
Conn3
Capacitor filter
and
resistor load
Conn2
Conn4
Subsystem1
Conn1
Conn2
SMPS
gate
pulse
generator
Out1
Out2
Subsystem2
VTRI
Io
Vo
Measurements block
Io_avg
Vo_avg
Subsystem3
0.9003
Load voltage in VoltA
9.003
Load voltage in VoltA
Continuous
Ideal switch
powergui
4
Multimeter

**FIGURE 10.39**
Model of buck converter SMPS.



Block Parameters: Subsystem2

SMPS Gate Pulse Generator (mask)

Enter the reference voltage in Volts, potential divider constant as a numeral, frequency of triangle carrier in Hertz, the gain multiplier setting constant as a numeral, the proportionality constant Kp and integral constant Ki for the PI controller in the box provided. Frequency of triangle carrier is the switching frequency of SMPS.

Parameters

Enter the reference voltage in Volts
9

Enter the potential divider gain constant
8/(9)

Enter the frequency of the triangle carrier in Hertz
100e3

Enter the gain multiplier setting constant
4.7

Enter the proportionality constant Kp for PI Controller
0.1

Enter the integral constant Ki for the PI Controller
6

Block Parameters: Subsystem1

Capacitor Filter and Resistor load (mask)

Enter the value of the capacitor filter in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the value of the capacitor filter in Farads
200e-6

Enter the value of the load resistance in Ohms
10

Block Parameters: Subsystem

Buck Converter Swiched Mode Power Supply (mask)

Enter the value of the DC input Voltage in Volts and the series inductance in Henries in the box provided.

Parameters

Enter the DC Input Voltage Source in Volts
15

Enter the value of the series inductance in Henries
300E-6

Block Parameters: Subsystem3

Measurement Block (mask)

Enter the switching frequency of the buck converter SMPS in Hertz in the box provided.

Parameters

Enter the switching frequency of the buck SMPS in Hertz
100e3

OK
Cancel
Help
Apply

**FIGURE 10.40**
Model of buck converter SMPS with interactive blocks.

section, component-level models are developed for these three fourth-order converters using semiconductor and passive components, and simulation results for both CCM and DCM operation are presented, tabulated and compared with those given in Chapter 8 [6,7,9].

### 10.7.1 SEPIC Converter

The component-level model of the SEPIC converter is shown in Figure 10.44. The interactive blocks of this model and the subsystems are shown in Figures 10.45 and 10.46, respectively [6,7]. The model simulation results for CCM and DCM are shown in Figures 10.47 and 10.48, respectively.

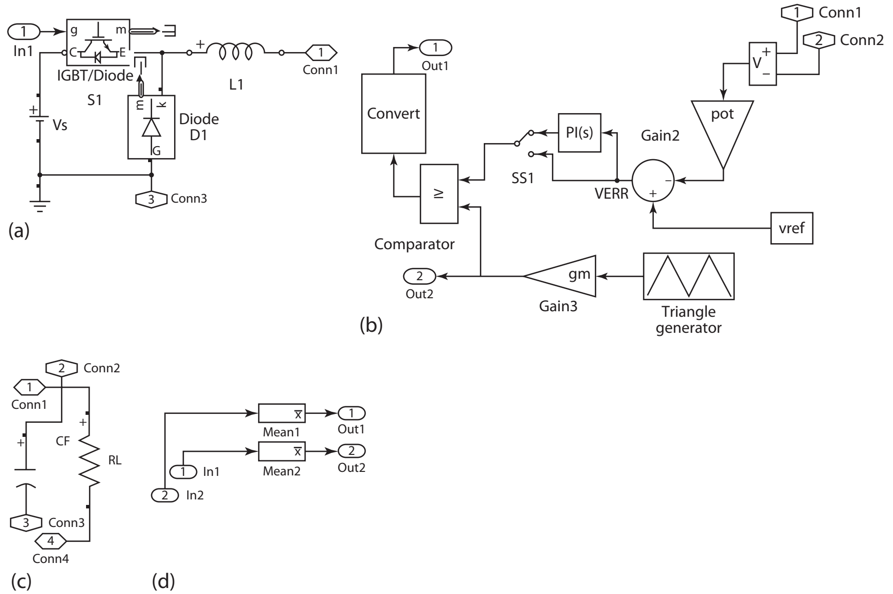

1
In1
g
m
C
E
IGBT/Diode
S1
+
Vs
m
k
Diode
D1
G
L1
1
Conn1
3
Conn3
(a)
1
Out1
Convert
Comparator
≥
2
Out2
SS1
PI(s)
VERR
Gain2
+
−
pot
V
1
Conn1
2
Conn2
vref
gm
Gain3
Triangle generator
(b)
2
Conn2
1
Conn1
CF
RL
3
Conn3
4
Conn4
(c)
Mean1
Mean2
1
Out1
2
Out2
1
In1
2
In2
(d)

**FIGURE 10.41**
Buck converter SMPS model subsystems.

The data shown in Table 8.1 are used for simulation. The simulation results are also tabulated in Table 10.11. Comparison of the simulation results in Table 10.11 with those in Tables 8.2 and 8.3 reveals that the values for CCM almost agree. For the case of DCM, there are some discrepancies with the minimum value for $iL_1$ and maximum value for $iL_2$ when compared with those in Tables 8.2 and 8.3. The polarities of measurement of the $iL_2$ inductor current and $V_{C1}$ voltage are reversed and, hence, a minus and plus sign are, respectively, inserted in Table 10.11.

### 10.7.2 Quadratic Boost Converter

The component-level model of the quadratic boost converter is shown in Figure 10.49 and model subsystems are shown in Figure 10.50 [6,7]. The simulation results are shown in Figure 10.51 for CCM and Figure 10.52 for DCM and tabulated in Table 10.12. Data shown in Table 8.4 are used for simulation. Comparison of simulation results in Table 10.12 with those in Table 8.5 shows that the values agree closely for CCM and for DCM, except for $V_O$. The $V_O$ value has an error of 7.68%.

### 10.7.3 Ultra-Lift Luo Converter

The component-level model of the ultra-lift Luo converter with interactive blocks is shown in Figure 10.53 and the model subsystems are shown in

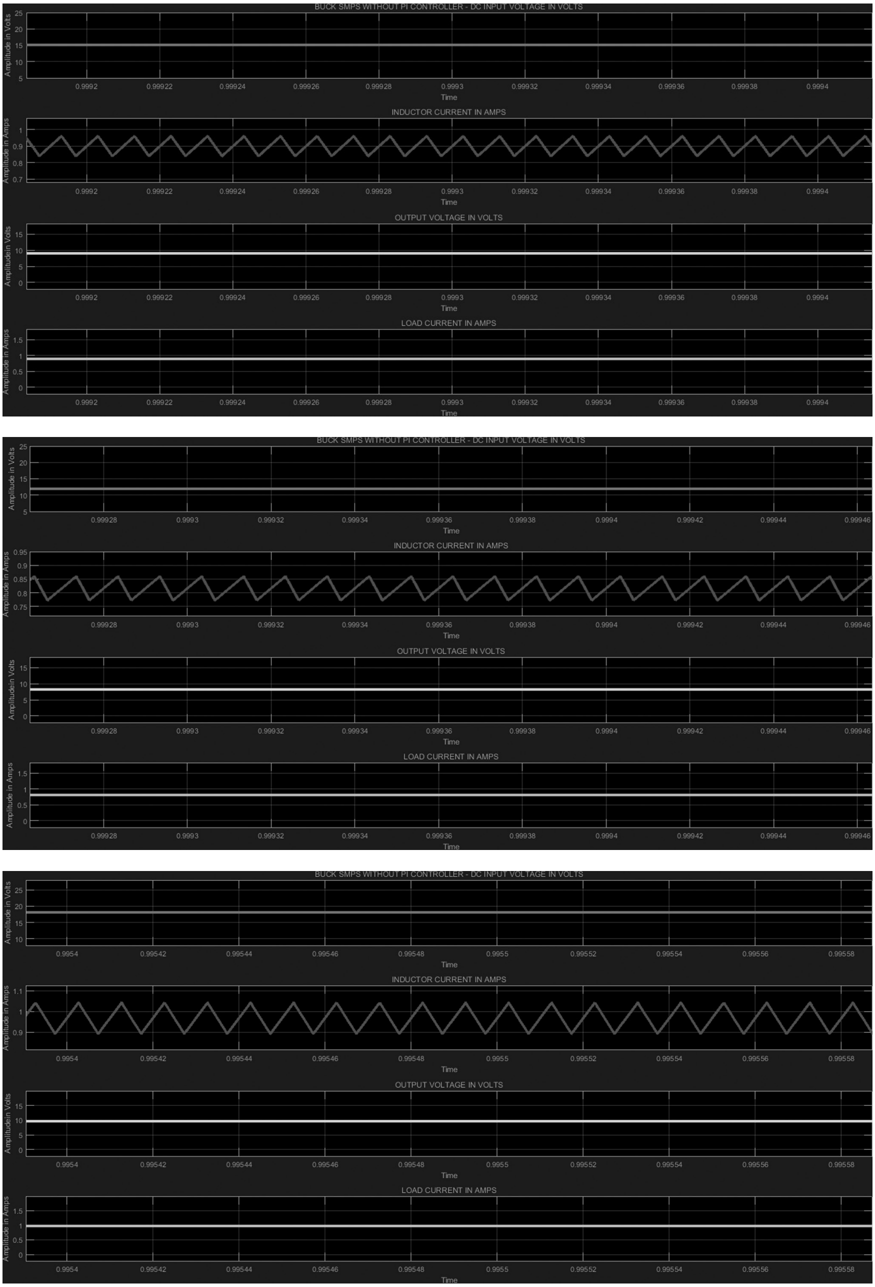


**FIGURE 10.42**
Buck converter SMPS without PI controller for a DC input voltage of (a) 15 V, (b) 12 V and (c) 18 V.

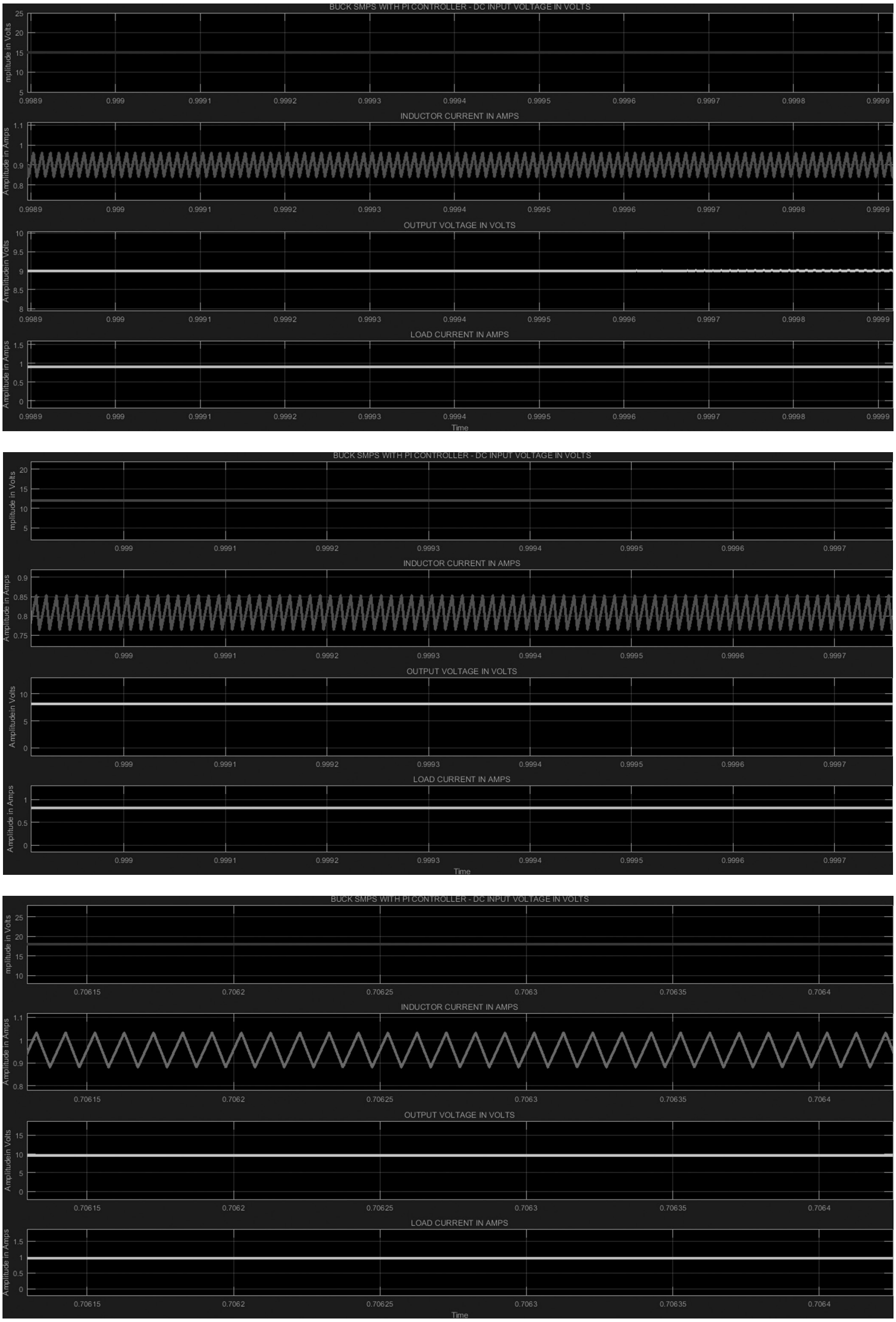
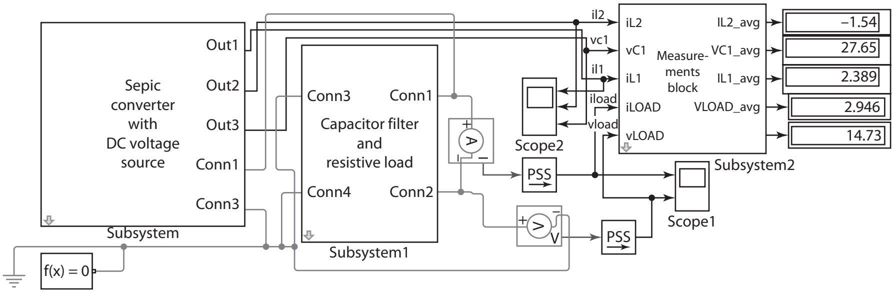


**FIGURE 10.43**
Buck converter SMPS with PI controller for a DC input voltage of (a) 15 V, (b) 12 V and (c) 18 V.

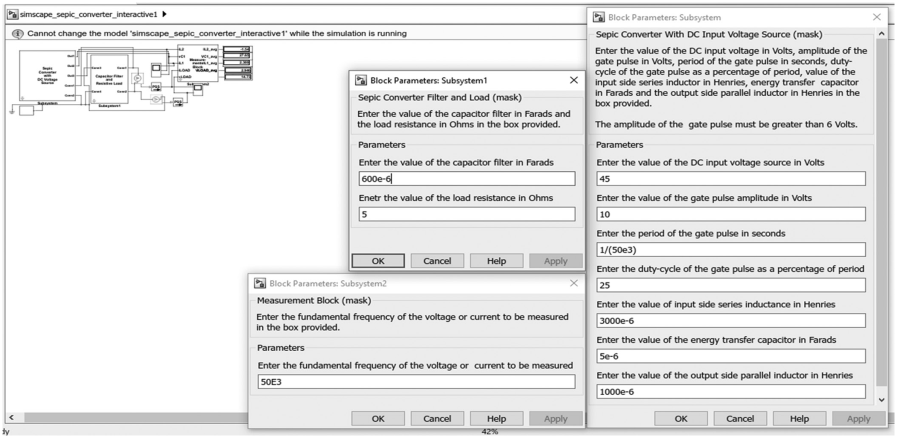
**TABLE 10.10**
Buck Converter SMPS Without PI Controller: Simulation Results

| Sl. No. | PI Controller | DC Input Voltage (V) | DC Output Voltage (V) | Load Current (A) | Remarks |
|---|---|---|---|---|---|
| 1 | NO | 15 | 9.007 | 0.9007 | Normal input voltage |
| 2 | NO | 12 | 8.163 | 0.8163 | Lower input voltage |
| 3 | NO | 18 | 9.674 | 0.9674 | Higher input voltage |
| 4 | YES | 15 | 9.003 | 0.9003 | Normal input voltage |
| 5 | YES | 12 | 8.08 | 0.808 | Lower input voltage |
| 6 | YES | 18 | 9.69 | 0.969 | Higher input voltage |



Sepic converter with DC voltage source
Out1
Out2
Out3
Conn1
Conn3
Subsystem
f(x) = 0
Conn3
Conn1
Capacitor filter and resistive load
Conn4
Conn2
Subsystem1
A
V
PSS
PSS
Scope2
Scope1
il2
vc1
il1
iload
vload
iL2
vC1
iL1
iLOAD
vLOAD
Measure-ments block
IL2_avg
VC1_avg
IL1_avg
VLOAD_avg
Subsystem2
−1.54
27.65
2.389
2.946
14.73

**FIGURE 10.44**
SEPIC converter model.



simscape_sepic_converter_interactive1
OK
Cancel
Help
Apply
42%

Cannot change the model 'simscape_sepic_converter_interactive1' while the simulation is running

Block Parameters: Subsystem1

Sepic Converter Filter and Load (mask)

Enter the value of the capacitor filter in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the value of the capacitor filter in Farads

600e-6

Enetr the value of the load resistance in Ohms

5

Block Parameters: Subsystem2

Measurement Block (mask)

Enter the fundamental frequency of the voltage or current to be measured in the box provided.

Parameters

Enter the fundamental frequency of the voltage or current to be measured

50E3

Block Parameters: Subsystem

Sepic Converter With DC Input Voltage Source (mask)

Enter the value of the DC input voltage in Volts, amplitude of the gate pulse in Volts, period of the gate pulse in seconds, duty-cycle of the gate pulse as a percentage of period, value of the input side series inductor in Henries, energy transfer capacitor in Farads and the output side parallel inductor in Henries in the box provided.

The amplitude of the gate pulse must be greater than 6 Volts.

Parameters

Enter the value of the DC input voltage source in Volts

45

Enter the value of the gate pulse amplitude in Volts

10

Enter the period of the gate pulse in seconds

1/(50e3)

Enter the duty-cycle of the gate pulse as a percentage of period

25

Enter the value of input side series inductance in Henries

3000e-6

Enter the value of the energy transfer capacitor in Farads

5e-6

Enter the value of the output side parallel inductor in Henries

1000e-6

**FIGURE 10.45**
SEPIC converter model with interactive blocks.

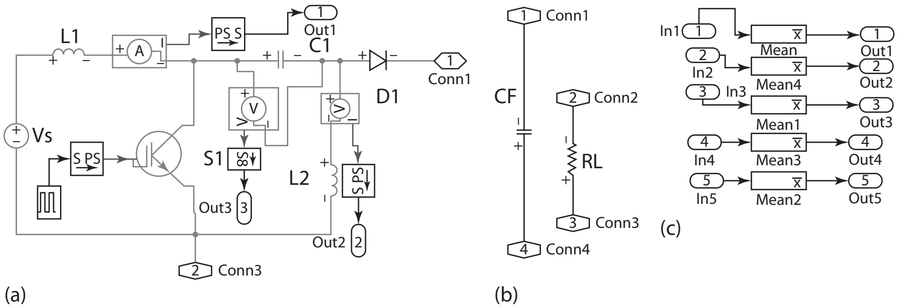

L1
A
PS S
1 Out1
C1
1 Conn1
D1
Vs
S PS
V
S1
V
L2
S PS
Out3 3
Out2 2
2 Conn3
(a)
1 Conn1
CF
2 Conn2
RL
3 Conn3
4 Conn4
(b)
In1 1
Mean
1 Out1
2 In2
Mean4
2 Out2
3 In3
Mean1
3 Out3
4 In4
Mean3
4 Out4
5 In5
Mean2
5 Out5
(c)

**FIGURE 10.46**
SEPIC converter model subsystems.

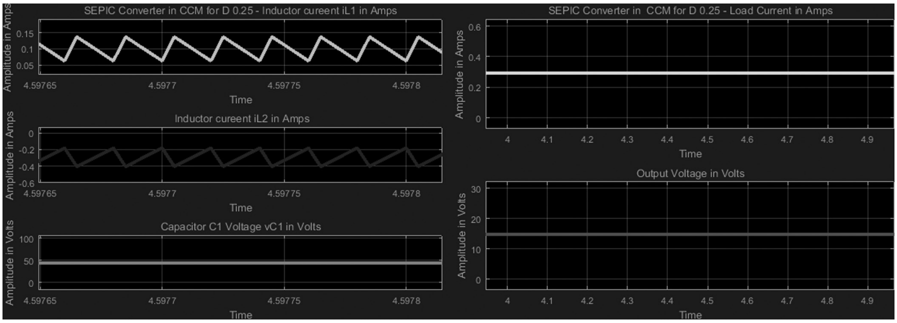


**FIGURE 10.47**
SEPIC converter in CCM for $D = 0.25$: simulation results.

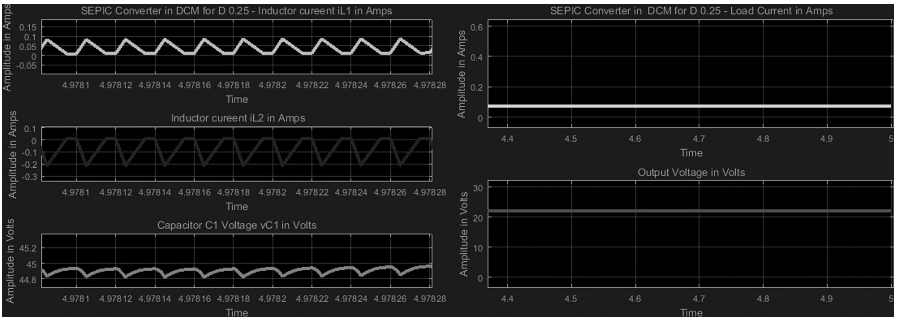
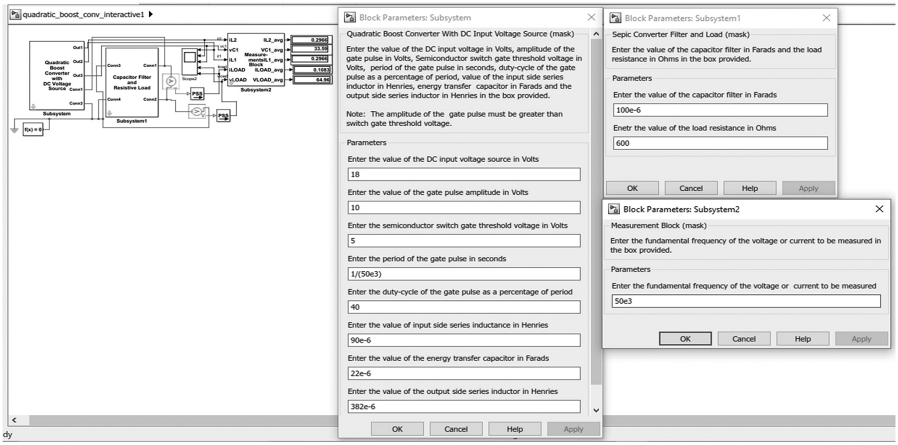


**FIGURE 10.48**
SEPIC converter in DCM for $D = 0.25$: simulation results.

**TABLE 10.11**

SEPIC Converter: Simulation Results

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $VC_1$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.25 | 0.0624 | 0.137 | −0.405 | −0.181 | 44.99 | 14.73 | 0.294 | CCM |
| 2 | 0.25 | 0.0088 | 0.0875 | −0.215 | 0.0132 | 44.92 | 22.19 | 0.0739 | DCM |


quadratic_boost_conv_interactive1
Quadratic Boost Converter with DC Voltage Source
Out1
Out2
Out3
Conn1
Conn3
Subsystem
f(x) = 0
Capacitor Filter and Resistive Load
Conn3
Conn1
Conn4
Conn2
Subsystem1
Scope2
PSS
PSS
iL2
vC1
iL1
iLOAD
vLOAD
Measure-ments Block
IL2_avg
VC1_avg
IL1_avg
ILOAD_avg
VLOAD_avg
Subsystem2
0.2966
33.59
0.2966
0.1083
64.96

Block Parameters: Subsystem

Quadratic Boost Converter With DC Input Voltage Source (mask)

Enter the value of the DC input voltage in Volts, amplitude of the gate pulse in Volts, Semiconductor switch gate threshold voltage in Volts, period of the gate pulse in seconds, duty-cycle of the gate pulse as a percentage of period, value of the input side series inductor in Henries, energy transfer capacitor in Farads and the output side series inductor in Henries in the box provided.

Note: The amplitude of the gate pulse must be greater than switch gate threshold voltage.

Parameters

Enter the value of the DC input voltage source in Volts: 18

Enter the value of the gate pulse amplitude in Volts: 10

Enter the semiconductor switch gate threshold voltage in Volts: 5

Enter the period of the gate pulse in seconds: 1/(50e3)

Enter the duty-cycle of the gate pulse as a percentage of period: 40

Enter the value of input side series inductance in Henries: 90e-6

Enter the value of the energy transfer capacitor in Farads: 22e-6

Enter the value of the output side series inductor in Henries: 382e-6

OK
Cancel
Help
Apply

Block Parameters: Subsystem1

Sepic Converter Filter and Load (mask)

Enter the value of the capacitor filter in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the value of the capacitor filter in Farads: 100e-6

Enetr the value of the load resistance in Ohms: 600

OK
Cancel
Help
Apply

Block Parameters: Subsystem2

Measurement Block (mask)

Enter the fundamental frequency of the voltage or current to be measured in the box provided.

Parameters

Enter the fundamental frequency of the voltage or current to be measured: 50e3

OK
Cancel
Help
Apply
dy

**FIGURE 10.49**
Quadratic boost converter model with interactive blocks.

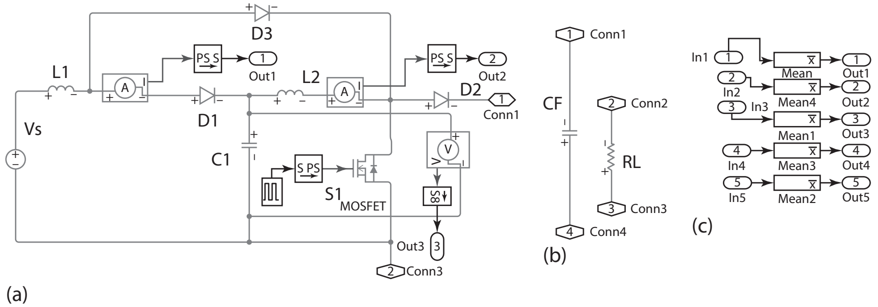

D3
L1
A
PS S
1
Out1
L2
A
PS S
2
Out2
D2
1
Conn1
Vs
D1
C1
S PS
S1
MOSFET
V
Out3
3
2
Conn3
(a)
1
Conn1
CF
2
Conn2
RL
3
Conn3
4
Conn4
(b)
In1
1
Mean
1
Out1
2
In2
Mean4
2
Out2
3
In3
Mean1
3
Out3
4
In4
Mean3
4
Out4
5
In5
Mean2
5
Out5
(c)

**FIGURE 10.50**
Quadratic boost converter model subsystems.

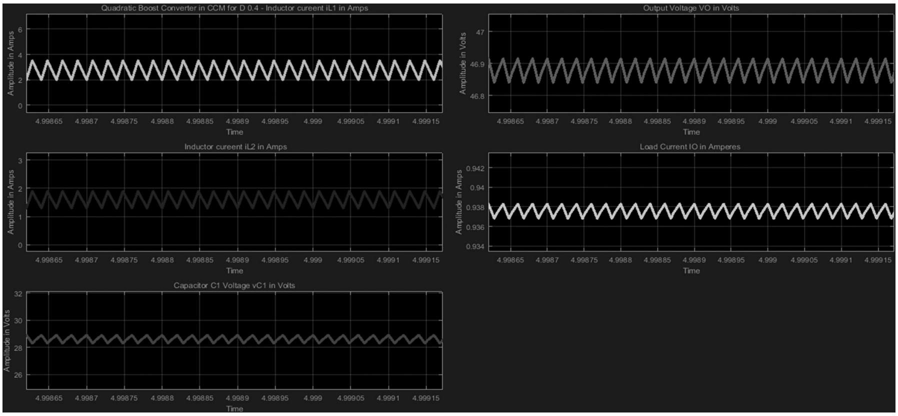


**FIGURE 10.51**
Quadratic boost converter in CCM for $D = 0.4$: simulation results.

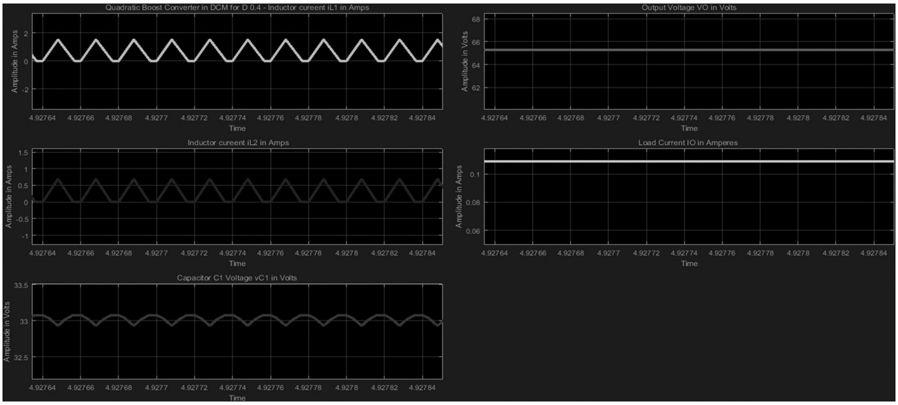


**FIGURE 10.52**
Quadratic boost converter in DCM for $D = 0.4$: simulation results.

Figure 10.54 [6,7]. Simulation of this model was carried out for both CCM and DCM using the data shown in Table 8.7. The simulation results for CCM and DCM are shown in Figures 10.55 and 10.56, respectively.

The simulation results are tabulated in Table 10.13. Comparison of the simulation results in Table 10.13 with those in Tables 8.8 and 8.9 reveals that the maximum and minimum values of the two inductor currents $iL_1$ and $iL_2$ and the load current $I_O$ agree closely. Capacitor voltage $V_{C1}$ for CCM and DCM and output voltage $V_O$ for CCM have some discrepancies. The output voltage $V_O$ for DCM agrees closely with the calculated value in Table 8.9. The current measurement direction for $iL_2$ and $I_O$ is reversed and, hence, a minus sign is inserted in Table 10.13.

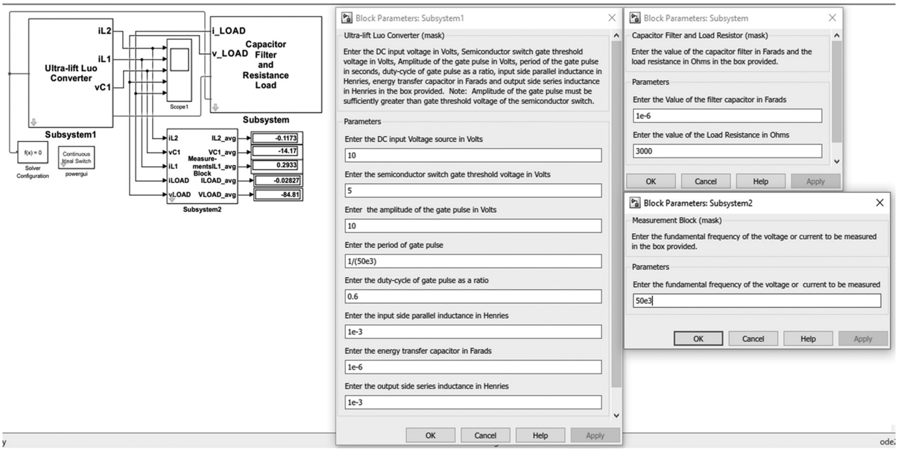
## 10.8 Three-Phase Three-Level Inverters

The system modelling of the three-phase diode-clamped three-level inverter (DCTLI) and the flying-capacitor three-level inverter (FCTLI) are reported in Sections 9.2 and 9.3. These system models are developed using ideal switches and Pulse Generator blocks, which signify the behaviour of three-phase DCTLI and FCTLI. In this chapter, component-level models are developed for three-phase DCTLI and FCTLI, simulation results obtained and compared with those presented in Chapter 9 [10–13]. These models are developed using passive and semiconductor components, which are not ideal switches; that is, these semiconductor components have forward voltage drop and on and off resistance.

**TABLE 10.12**

Quadratic Boost Converter: Simulation Results

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $VC_1$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.4 | 1.985 | 3.51 | 1.296 | 1.894 | 28.6 | 46.88 | 0.9375 | CCM |
| 2 | 0.4 | 0 | 1.53 | 0 | 0.6915 | 33.05 | 65.31 | 0.1088 | DCM |


iL2
iL1
vC1
Ultra-lift Luo Converter
Subsystem1
i_LOAD
v_LOAD
Capacitor Filter and Resistance Load
Subsystem
Scope1
f(x) = 0
Solver Configuration
Continuous Ideal Switch
powergui
iL2
vC1
iL1
iLOAD
vLOAD
IL2_avg
VC1_avg
IL1_avg
ILOAD_avg
VLOAD_avg
Measure-ments Block
Subsystem2
-0.1173
-14.17
0.2933
-0.02827
-84.81
OK
Cancel
Help
Apply

Block Parameters: Subsystem1

Ultra-lift Luo Converter (mask)

Enter the DC input voltage in Volts, Semiconductor switch gate threshold voltage in Volts, Amplitude of the gate pulse in Volts, period of the gate pulse in seconds, duty-cycle of gate pulse as a ratio, input side parallel inductance in Henries, energy transfer capacitor in Farads and output side series inductance in Henries in the box provided. Note: Amplitude of the gate pulse must be sufficiently greater than gate threshold voltage of the semiconductor switch.

Parameters

Enter the DC input Voltage source in Volts
10

Enter the semiconductor switch gate threshold voltage in Volts
5

Enter the amplitude of the gate pulse in Volts
10

Enter the period of gate pulse
1/(50e3)

Enter the duty-cycle of gate pulse as a ratio
0.6

Enter the input side parallel inductance in Henries
1e-3

Enter the energy transfer capacitor in Farads
1e-6

Enter the output side series inductance in Henries
1e-3

Block Parameters: Subsystem

Capacitor Filter and Load Resistor (mask)

Enter the value of the capacitor filter in Farads and the load resistance in Ohms in the box provided.

Parameters

Enter the Value of the filter capacitor in Farads
1e-6

Enter the value of the Load Resistance in Ohms
3000

Block Parameters: Subsystem2

Measurement Block (mask)

Enter the fundamental frequency of the voltage or current to be measured in the box provided.

Parameters

Enter the fundamental frequency of the voltage or current to be measured
50e3

**FIGURE 10.53**
Ultra-lift Luo converter model with interactive blocks.

### 10.8.1 Three-Phase Diode-Clamped Three-Level Inverter

Detailed analysis of the three-phase DCTLI is shown in Section 9.2. The circuit topology is given in Figure 9.1 [10–13]. The component-level model of the three-phase DCTLI is shown in Figure 10.57.

The interactive blocks of this model are shown in Figure 10.58 and the model subsystems are shown in Figure 10.59.

Figure 10.59a–e shows, respectively, semiconductor switches with clamping diodes, the gate pulse generator unit, the DC voltage source with DC link capacitors, three-phase load resistors and the output voltage root mean square (RMS) value and total harmonic distortion (THD) measurement unit.

Simulation results are shown in Figure 10.60.

Simulation results are tabulated in Table 10.14. Comparison of the simulation results in Table 10.14 with the results and derivation in Chapter 9 shows close agreement.

### 10.8.2 Three-Phase Flying-Capacitor Three-Level Inverter

The three-phase FCTLI system model is discussed in Section 9.3. Figure 9.8 shows the circuit topology of the three-phase FCTLI [10–13]. The component-level model using passive and semiconductor components is shown in Figure 10.61.

The interactive blocks of this model are shown in Figure 10.62 and the model subsystems are shown in Figure 10.63.

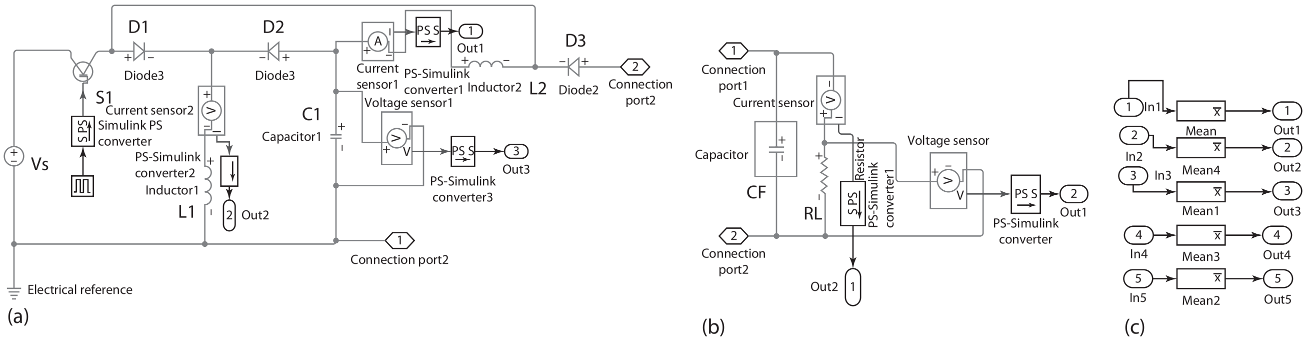

D1
Diode3
D2
Diode3
Current sensor1
PS-Simulink converter1
Out1
Inductor2
L2
D3
Diode2
Connection port2
S1
Current sensor2
Simulink PS converter
Vs
PS-Simulink converter2
Inductor1
L1
Out2
C1
Capacitor1
Voltage sensor1
PS-Simulink converter3
Out3
Connection port2
Electrical reference
(a)
Connection port1
Current sensor
Capacitor
CF
RL
Resistor
PS-Simulink converter1
Voltage sensor
PS-Simulink converter
Out1
Connection port2
Out2
(b)
In1
Mean
Out1
In2
Mean4
Out2
In3
Mean1
Out3
In4
Mean3
Out4
In5
Mean2
Out5
(c)

**FIGURE 10.54**
Ultra-lift Luo converter model subsystems.

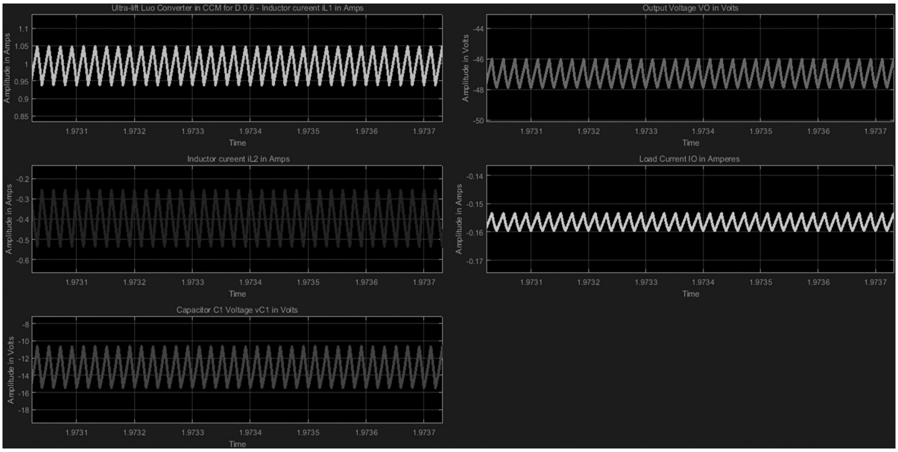


**FIGURE 10.55**
Ultra-lift Luo converter in CCM: simulation results.

Figure 10.63a–e shows, respectively, the three-phase semiconductor switches with flying capacitors, the gate pulse generators, the DC voltage source, the three-phase resistor load and the output voltage RMS and THD measurement unit.

A small resistance of 1 μΩ is connected in series with each DC voltage source for the convergence of simulation. The simulation results are shown in Figure 10.64.

Simulation results are tabulated in Table 10.15. Comparison of the simulation results for the three-phase FCTLI with those in Chapter 9 and also with the derived formula shows that the results in Table 10.15 agree closely.

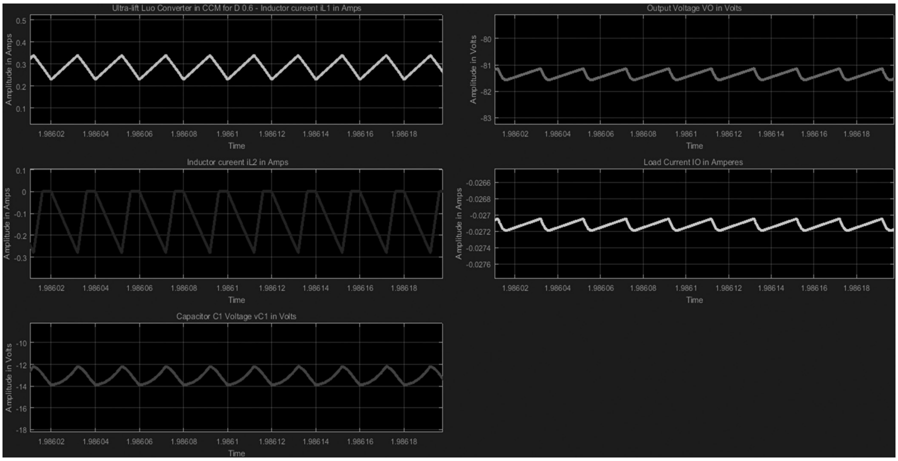


**FIGURE 10.56**
Ultra-lift Luo converter in DCM: simulation results.

**TABLE 10.13**

Ultra-Lift Luo Converter: Simulation Results

| Sl. No. | Duty Ratio | Minimum $L_1$ Inductor Current (A) | Maximum $L_1$ Inductor Current (A) | Minimum $L_2$ Inductor Current (A) | Maximum $L_2$ Inductor Current (A) | Capacitor $C_1$ Voltage $VC_1$ (V) | Output Voltage $V_O$ (V) | Load Current $I_O$ (A) | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.6 | 0.9378 | 1.048 | −0.256 | −0.536 | −13.19 | −47.02 | −0.156 | CCM |
| 2 | 0.6 | 0.2291 | 0.3395 | −0.2795 | 0 | −13.09 | −81.42 | −0.027 | DCM |

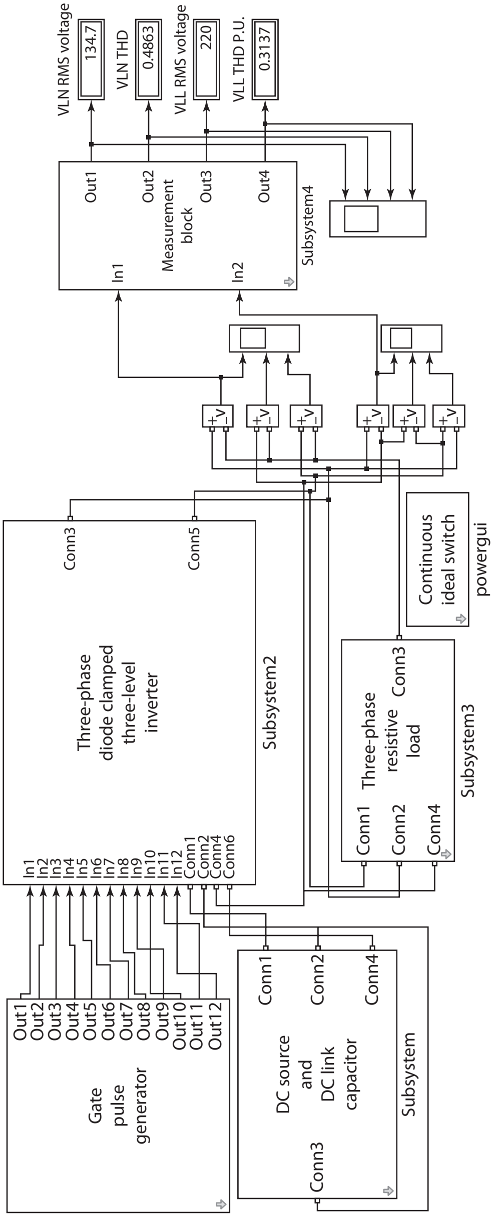
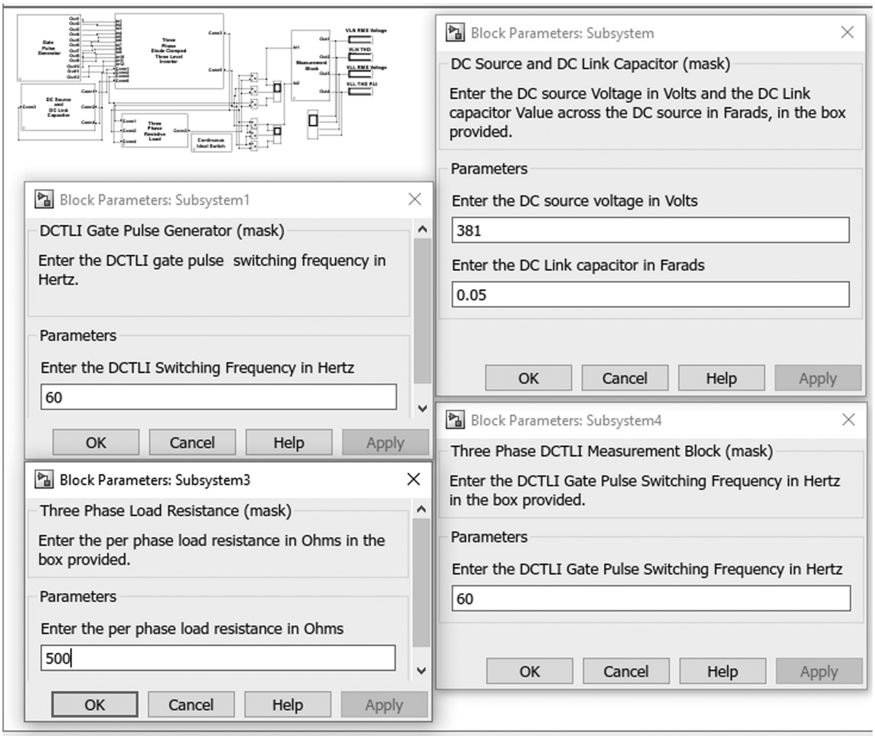

VLN RMS voltage
134.7
VLN THD
0.4863
VLL RMS voltage
220
VLL THD P.U.
0.3137
Out1
Out2
Out3
Out4
Measurement block
In1
In2
Subsystem4
Conn3
Conn5
Three-phase diode clamped three-level inverter
Subsystem2
In1
In2
In3
In4
In5
In6
In7
In8
In9
In10
In11
In12
Conn1
Conn2
Conn4
Conn6
Continuous ideal switch
powergui
Three-phase resistive load
Conn1
Conn2
Conn4
Conn3
Subsystem3
Gate pulse generator
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
DC source and DC link capacitor
Conn1
Conn2
Conn4
Conn3
Subsystem

**FIGURE 10.57**
Three-phase DCTLI model.



Block Parameters: Subsystem

DC Source and DC Link Capacitor (mask)

Enter the DC source Voltage in Volts and the DC Link capacitor Value across the DC source in Farads, in the box provided.

Parameters

Enter the DC source voltage in Volts

381

Enter the DC Link capacitor in Farads

0.05

Block Parameters: Subsystem1

DCTLI Gate Pulse Generator (mask)

Enter the DCTLI gate pulse switching frequency in Hertz.

Parameters

Enter the DCTLI Switching Frequency in Hertz

60

Block Parameters: Subsystem4

Three Phase DCTLI Measurement Block (mask)

Enter the DCTLI Gate Pulse Switching Frequency in Hertz in the box provided.

Parameters

Enter the DCTLI Gate Pulse Switching Frequency in Hertz

60

Block Parameters: Subsystem3

Three Phase Load Resistance (mask)

Enter the per phase load resistance in Ohms in the box provided.

Parameters

Enter the per phase load resistance in Ohms

500

**FIGURE 10.58**
Three-phase DCTLI model with interactive blocks.

## 10.9 Three-Phase Sine PWM Inverter

The method of generating gate pulses for a three-phase inverter by the sine PWM technique is discussed in Section 4.4. The system model of the three-phase sine PWM inverter is presented in Section 4.4.1. In this section, the circuit component-level model of the three-phase sine PWM inverter is developed and the results obtained by simulation are compared with those presented in Chapter 4.

The interactive component-level model of the three-phase sine PWM inverter is shown in Figure 10.65.

The model subsystems are shown in Figure 10.66a–d.

In Figure 10.65, the data entered are for an overmodulation index of 1.1. The DC link voltage is 286 V, the sine-wave modulating signal frequency is 60 Hz, the triangle carrier frequency is 2 kHz and the load resistance is 1 kΩ. The MOSFET gate threshold voltage is 5 V and, therefore, the gain multiplier for the gate pulse amplitude entered is 10, so as to exceed this gate threshold voltage. Two amplitude modulation (A.M.) indices are used for simulation,

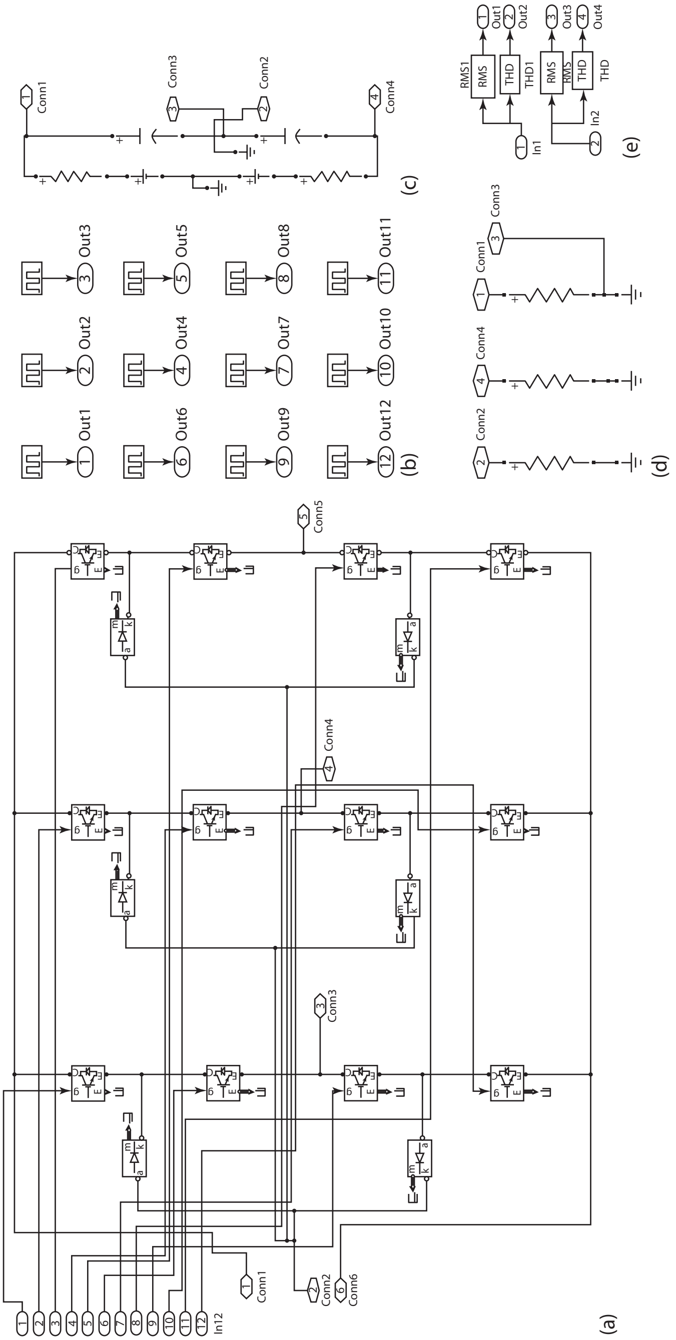

(a)
In12
Conn1
Conn2
Conn3
Conn4
Conn5
Conn6
g
C
E
m
a
k
(b)
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
(c)
Conn1
Conn2
Conn3
Conn4
(d)
Conn1
Conn2
Conn3
Conn4
(e)
In1
In2
RMS1
RMS
THD1
THD
Out1
Out2
Out3
Out4

**FIGURE 10.59**
Three-phase DCTLI model subsystems.

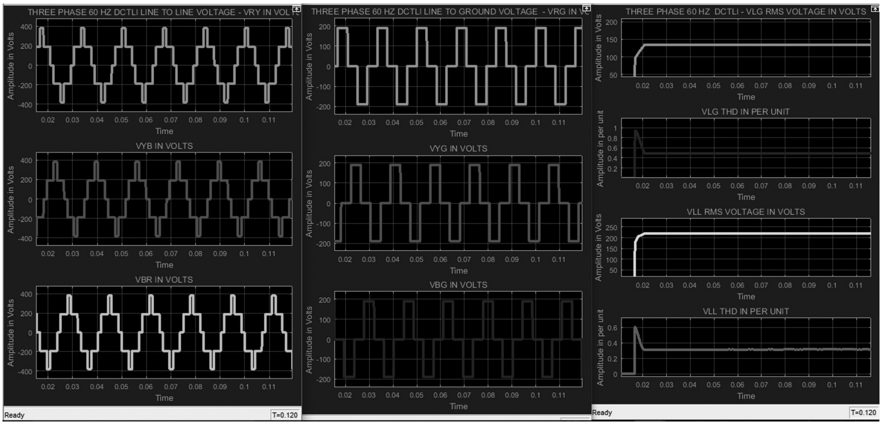

THREE PHASE 60 HZ DCTLI LINE TO LINE VOLTAGE - VRY IN VOL
VYB IN VOLTS
VBR IN VOLTS
THREE PHASE 60 HZ DCTLI LINE TO GROUND VOLTAGE - VRG IN V
VYG IN VOLTS
VBG IN VOLTS
THREE PHASE 60 HZ DCTLI - VLG RMS VOLTAGE IN VOLTS
VLG THD IN PER UNIT
VLL RMS VOLTAGE IN VOLTS
VLL THD IN PER UNIT
Amplitude in Volts
Amplitude in per unit
Time
Ready
T=0.120

**FIGURE 10.60**
Three-phase DCTLI: simulation results.

**TABLE 10.14**
Three-Phase DCTLI: Simulation Results

| Sl. No. | DC Link Voltage (V) | Frequency (Hz) | $V_{LL}$ RMS (V) | $V_{LL}$ THD Per Unit | $V_{LG}$ RMS (V) | $V_{LG}$ THD Per Unit |
|---|---|---|---|---|---|---|
| 1 | 381 | 60 | 220 | 0.3137 | 134.7 | 0.4863 |

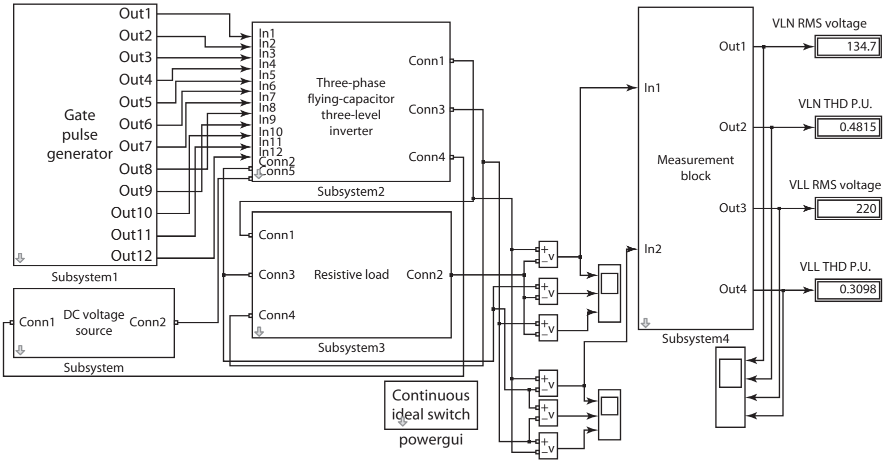
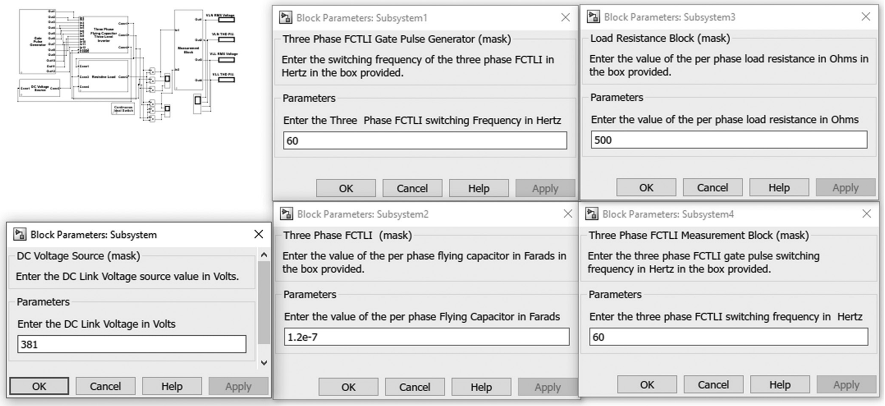

Gate pulse generator
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
Subsystem1
In1
In2
In3
In4
In5
In6
In7
In8
In9
In10
In11
In12
Conn2
Conn5
Three-phase flying-capacitor three-level inverter
Conn1
Conn3
Conn4
Subsystem2
Conn1
Conn3
Conn4
Resistive load
Conn2
Subsystem3
Conn1
DC voltage source
Conn2
Subsystem
Continuous ideal switch
powergui
In1
In2
Measurement block
Out1
Out2
Out3
Out4
Subsystem4
VLN RMS voltage
134.7
VLN THD P.U.
0.4815
VLL RMS voltage
220
VLL THD P.U.
0.3098

**FIGURE 10.61**
Three-phase FCTLI model.



Block Parameters: Subsystem
DC Voltage Source (mask)
Enter the DC Link Voltage source value in Volts.
Parameters
Enter the DC Link Voltage in Volts
381

Block Parameters: Subsystem1
Three Phase FCTLI Gate Pulse Generator (mask)
Enter the switching frequency of the three phase FCTLI in Hertz in the box provided.
Parameters
Enter the Three Phase FCTLI switching Frequency in Hertz
60

Block Parameters: Subsystem2
Three Phase FCTLI (mask)
Enter the value of the per phase flying capacitor in Farads in the box provided.
Parameters
Enter the value of the per phase Flying Capacitor in Farads
1.2e-7

Block Parameters: Subsystem3
Load Resistance Block (mask)
Enter the value of the per phase load resistance in Ohms in the box provided.
Parameters
Enter the value of the per phase load resistance in Ohms
500

Block Parameters: Subsystem4
Three Phase FCTLI Measurement Block (mask)
Enter the three phase FCTLI gate pulse switching frequency in Hertz in the box provided.
Parameters
Enter the three phase FCTLI switching frequency in Hertz
60

**FIGURE 10.62**
Three-phase FCTLI model with interactive blocks.

which is the ratio of the peak of the modulating sine wave to the peak of the triangle carrier wave. The modulating sine-wave amplitude is entered as 1.1 V. The modulating sine wave has an amplitude between 0 and 1 for undermodulation, 1 for normal modulation and above 1 for overmodulation.

Figure 10.66a shows the three-phase sine-triangle carrier PWM generator and Figure 10.66b shows the three-phase MOSFET inverter model subsystems. The three-phase sine-wave modulating signals $V_{an}$, $V_{bn}$ and $V_{cn}$ are compared separately with a triangle carrier having a peak value of 1 V using Relational Operator blocks known as *comparators*, the output of which form the PWM gate pulse for the three upper arm switches S1, S3 and S5, respectively. These three PWM gate pulses are then inverted using NOT gates to generate the PWM gate pulse for the lower arm switches S2, S4 and S6, respectively. Figure 10.66c shows the load current, line-to-neutral and line-to-line output voltage measurement subsystem. The RMS value and THD measurement subsystem for the line-to-neutral and line-to-line output voltages are shown in Figure 10.66d.

The component-level model simulation of the three-phase sine PWM inverter was carried out in Simulink using the ode23t (mod. stiff/trapezoidal) solver for two values of AM indices, 0.9 and 1.1. The simulation results are shown in Figure 10.67a–h for the former and Figure 10.68a–h for the latter AM index.

The results are tabulated in Table 10.16.

## 10.10 Three-Phase Five-Level Cascaded H-Bridge Inverter

The topology and principle of operation of the three-phase five-level cascaded H-bridge inverter (TPFLCHBI) is presented in Section 9.4 and the interactive system model development is presented in Section 9.4.1. Here, the interactive

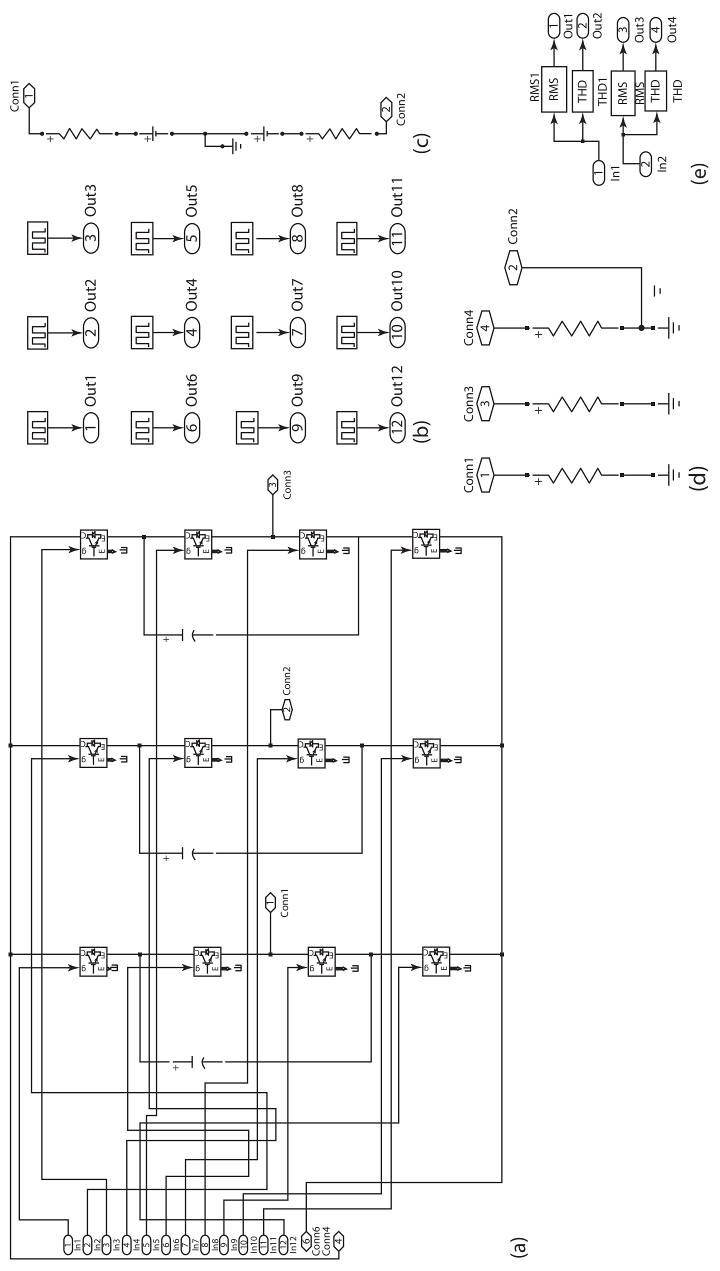

(a)
In1
In2
In3
In4
In5
In6
In7
In8
In9
In10
In11
In12
Conn6
Conn4
Conn1
Conn2
Conn3
g
E
(b)
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Out9
Out10
Out11
Out12
(c)
Conn1
Conn2
(d)
Conn1
Conn3
Conn4
Conn2
(e)
In1
In2
RMS1
RMS
THD1
THD
Out1
Out2
Out3
Out4

**FIGURE 10.63**
Three-phase FCTLI model subsystems.

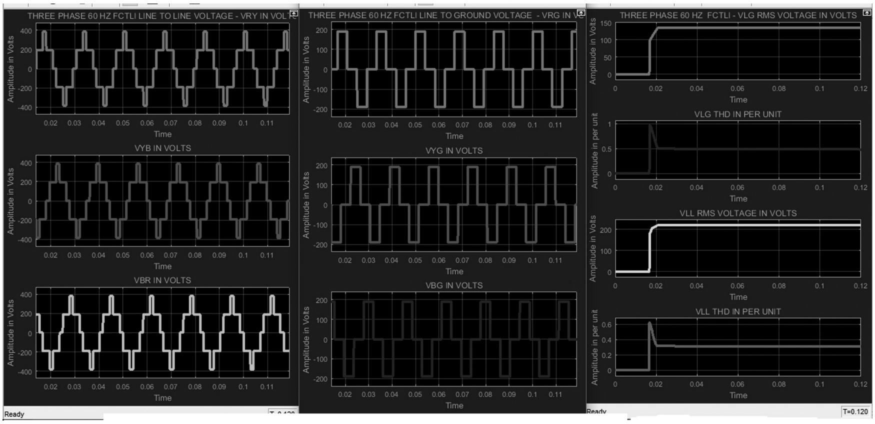
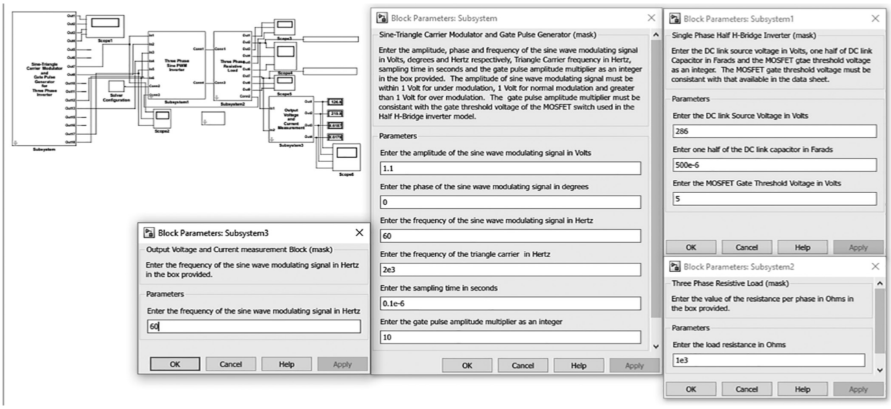


**FIGURE 10.64**
Three-phase FCTLI: simulation results.

## TABLE 10.15

Three-Phase FCTLI: Simulation Results

| Sl. No. | DC Link Voltage (V) | Frequency(Hz) | RMS (V) | THD Per Unit | RMS (V) | THD Per Unit |
|---|---|---|---|---|---|---|
| 1 | 381 | 60 | 220 | 0.3098 | 134.7 | 0.4815 |


Sine-Triangle Carrier Modulator and Gate Pulse Generator for Three Phase Inverter
Subsystem
Scope1
Three Phase Sine PWM Inverter
Subsystem1
Three Phase Resistive Load
Subsystem2
Solver Configuration
Scope2
Output Voltage and Current Measurement
Subsystem3
Scope3
Scope4
Scope5
Scope6
Block Parameters: Subsystem
Block Parameters: Subsystem1
Block Parameters: Subsystem2
Block Parameters: Subsystem3
OK
Cancel
Help
Apply

Block Parameters: Subsystem

Sine-Triangle Carrier Modulator and Gate Pulse Generator (mask)

Enter the amplitude, phase and frequency of the sine wave modulating signal in Volts, degrees and Hertz respectively, Triangle Carrier frequency in Hertz, sampling time in seconds and the gate pulse amplitude multiplier as an integer in the box provided. The amplitude of sine wave modulating signal must be within 1 Volt for under modulation, 1 Volt for normal modulation and greater than 1 Volt for over modulation. The gate pulse amplitude multiplier must be consistant with the gate threshold voltage of the MOSFET switch used in the Half H-Bridge inverter model.

Parameters

Enter the amplitude of the sine wave modulating signal in Volts
1.1

Enter the phase of the sine wave modulating signal in degrees
0

Enter the frequency of the sine wave modulating signal in Hertz
60

Enter the frequency of the triangle carrier in Hertz
2e3

Enter the sampling time in seconds
0.1e-6

Enter the gate pulse amplitude multiplier as an integer
10

Block Parameters: Subsystem1

Single Phase Half H-Bridge Inverter (mask)

Enter the DC link source voltage in Volts, one half of DC link Capacitor in Farads and the MOSFET gtae threshold voltage as an integer. The MOSFET gate threshold voltage must be consistant with that available in the data sheet.

Parameters

Enter the DC link Source Voltage in Volts
286

Enter one half of the DC link capacitor in Farads
500e-6

Enter the MOSFET Gate Threshold Voltage in Volts
5

Block Parameters: Subsystem2

Three Phase Resistive Load (mask)

Enter the value of the resistance per phase in Ohms in the box provided.

Parameters

Enter the load resistance in Ohms
1e3

Block Parameters: Subsystem3

Output Voltage and Current measurement Block (mask)

Enter the frequency of the sine wave modulating signal in Hertz in the box provided.

Parameters

Enter the frequency of the sine wave modulating signal in Hertz
60

**FIGURE 10.65**
Three-phase sine PWM inverter with interactive blocks.

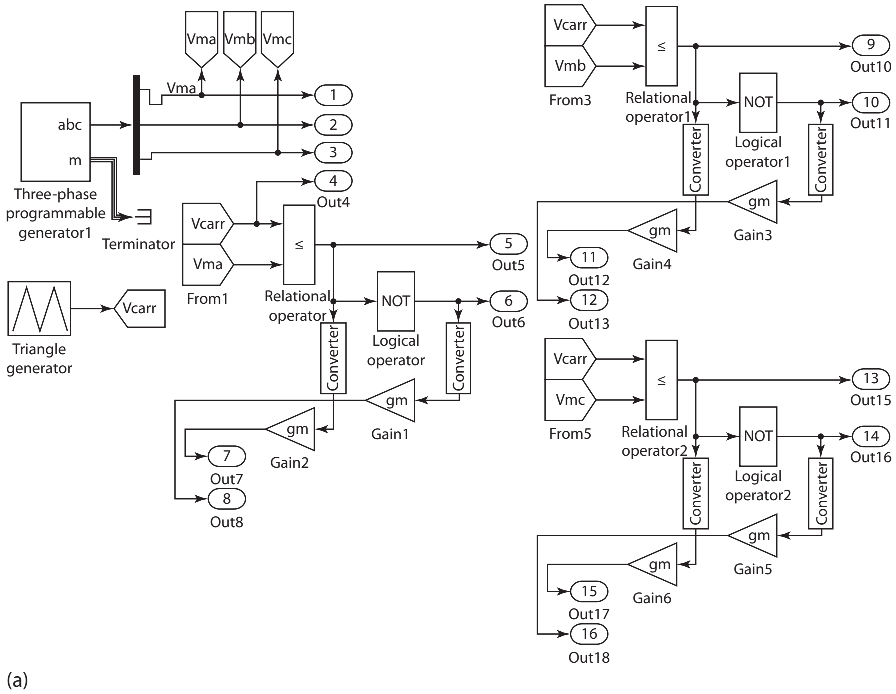

Vma
Vmb
Vmc
Vma
abc
m
Three-phase programmable generator1
Terminator
1
2
3
4
Out4
Vcarr
Vma
From1
≤
Relational operator
5
Out5
NOT
Logical operator
6
Out6
Converter
Converter
gm
Gain1
gm
Gain2
7
Out7
8
Out8
Vcarr
Triangle generator
Vcarr
Vmb
From3
≤
Relational operator1
9
Out10
NOT
Logical operator1
10
Out11
Converter
Converter
gm
Gain3
gm
Gain4
11
Out12
12
Out13
Vcarr
Vmc
From5
≤
Relational operator2
13
Out15
NOT
Logical operator2
14
Out16
Converter
Converter
gm
Gain5
gm
Gain6
15
Out17
16
Out18
(a)

**FIGURE 10.66**
Three-phase sine PWM inverter model subsystems. (a) Three-phase sine-triangle carrier PWM generator.

component-level model of this converter is presented. Model simulation results were obtained and are presented and compared with those given in Chapter 9.

The component-level model of the TPFLCHBI is shown in Figure 10.69 [14,15]. This model, with an interactive dialogue box, is shown in Figure 10.70.

The internal subsystems of this model are shown in Figure 10.71a–d. In this model, MOSFET semiconductor switches are used. In the dialogue box in Figure 10.70, the upper and lower H-bridge DC voltage source, amplitude of the gate pulse, gate pulse switching period, load resistance, load inductance, switching frequency and MOSFET gate threshold voltage are entered in the appropriate box. In Figure 10.71a–d, the voltage source for the upper and lower H-bridge, gate pulse generator for the MOSFET switches, MOSFET switch arrangement for the TPFLCHBI and the R–L load with measurement blocks are shown.

Here, the MOSFET gate threshold voltage is entered as 5 V and, hence, a gate pulse amplitude of 10 V is used. The pulse generator shown in Figure 10.71b is the same as that shown in Figure 9.18a. Here, the pulse amplitude $A$ is 10 V and the period $T$ is 1/(50) s. The method of calculating the duty cycle and phase delay for various switches is the same as explained in Section 9.4.1 and in Table 9.8. The R–L load component values are 50 Ω and 0.5 H.

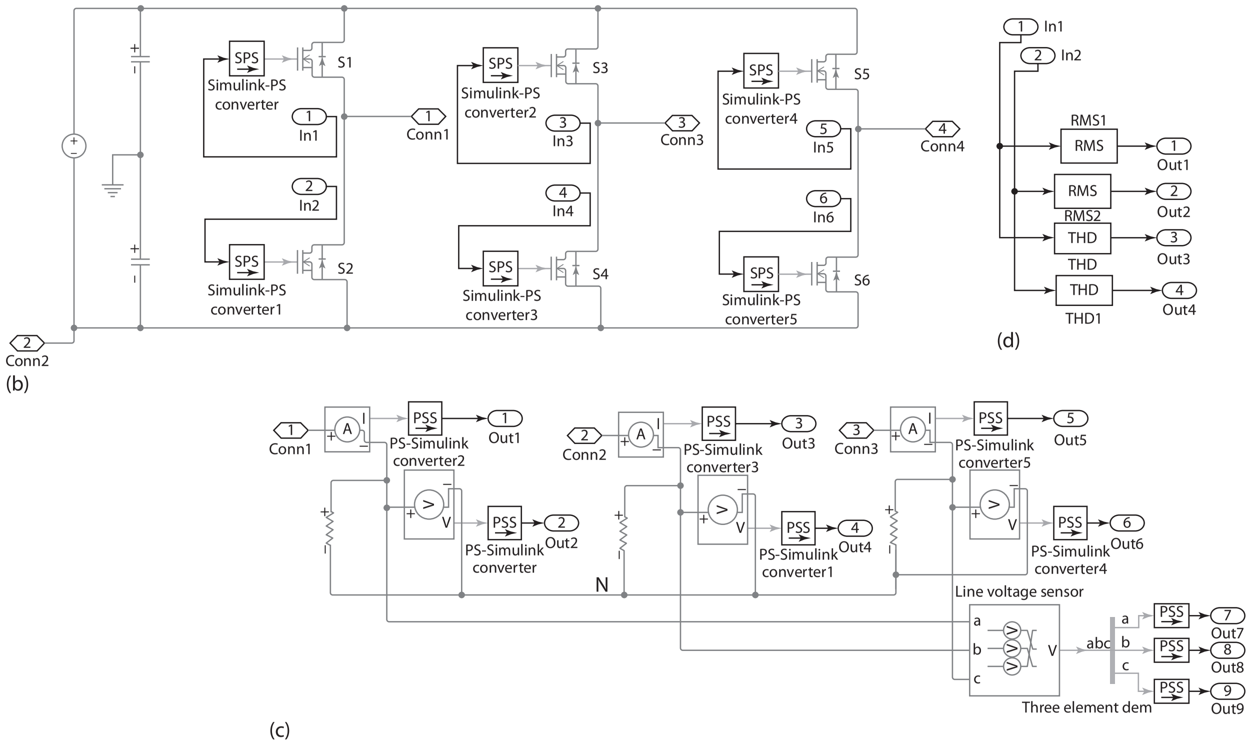

SPS
Simulink-PS converter
S1
1 In1
1 Conn1
2 In2
Simulink-PS converter1
S2
Simulink-PS converter2
S3
3 In3
3 Conn3
4 In4
Simulink-PS converter3
S4
Simulink-PS converter4
S5
5 In5
4 Conn4
6 In6
Simulink-PS converter5
S6
2 Conn2
(b)
1 In1
2 In2
RMS1
RMS
1 Out1
RMS
RMS2
2 Out2
THD
THD
3 Out3
THD
THD1
4 Out4
(d)
1 Conn1
A
PSS
PS-Simulink converter2
1 Out1
PS-Simulink converter
2 Out2
2 Conn2
PS-Simulink converter3
3 Out3
PS-Simulink converter1
4 Out4
3 Conn3
PS-Simulink converter5
5 Out5
PS-Simulink converter4
6 Out6
N
Line voltage sensor
a
b
c
V
abc
Three element dem
7 Out7
8 Out8
9 Out9
(c)

**FIGURE 10.66**
Three-phase sine PWM inverter model subsystems. (b) Three-phase MOSFET inverter. (c) Output voltage and current measurement unit. (d) Resistive load.

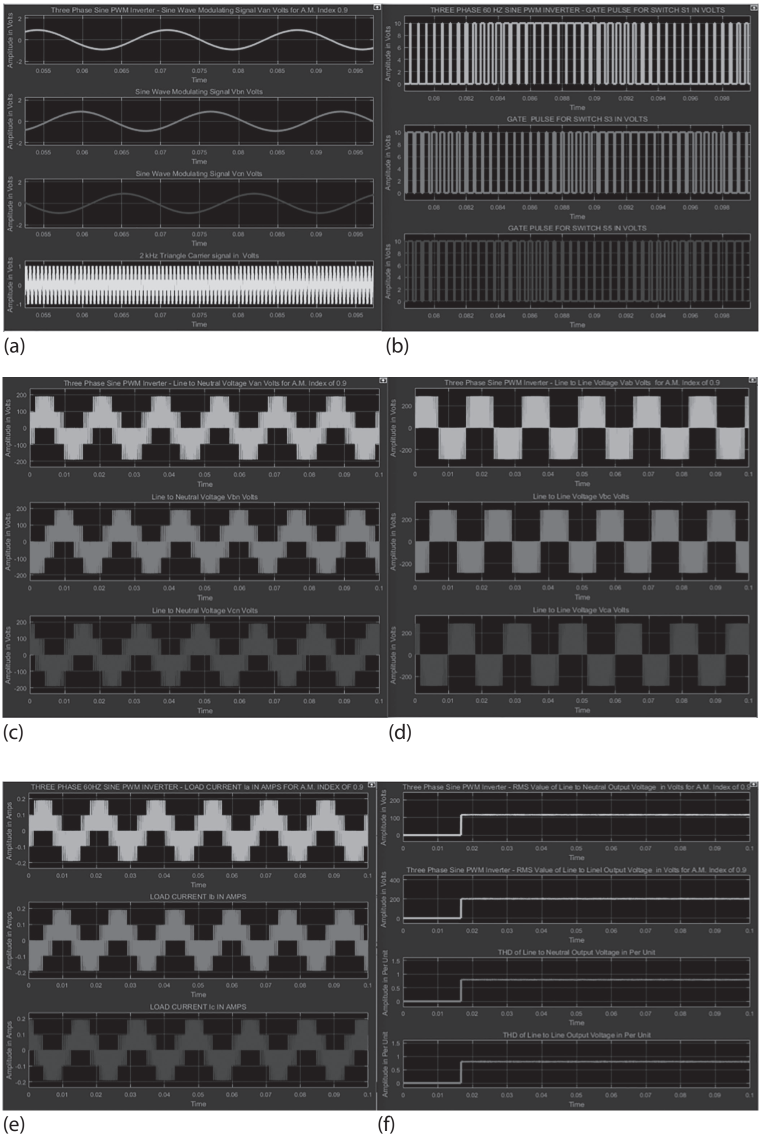


**FIGURE 10.67**
Three-phase sine PWM inverter component-level simulation. (a) Three-phase sine-wave modulating signal and triangle carrier (left). (b) Three-phase PWM gate pulse for upper arm switches of inverter (right). (c) Three-phase line-to-neutral output voltage (left). (d) Three-phase line-to-line output voltage (right). (e) Three-phase load current (left). (f) RMS value and THD of line-to-neutral and line-to line output voltage (right).

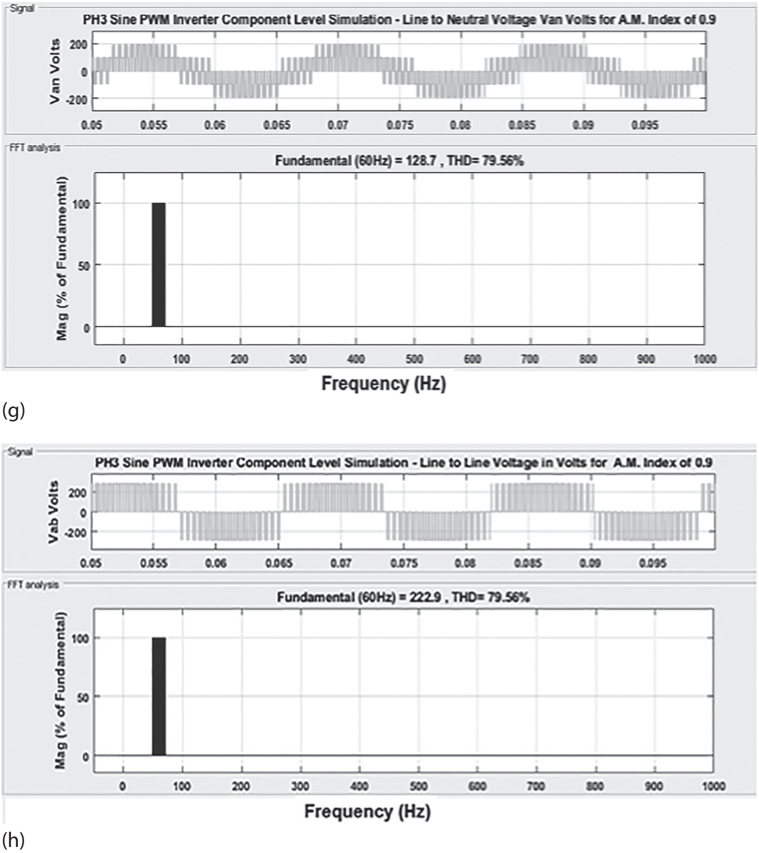


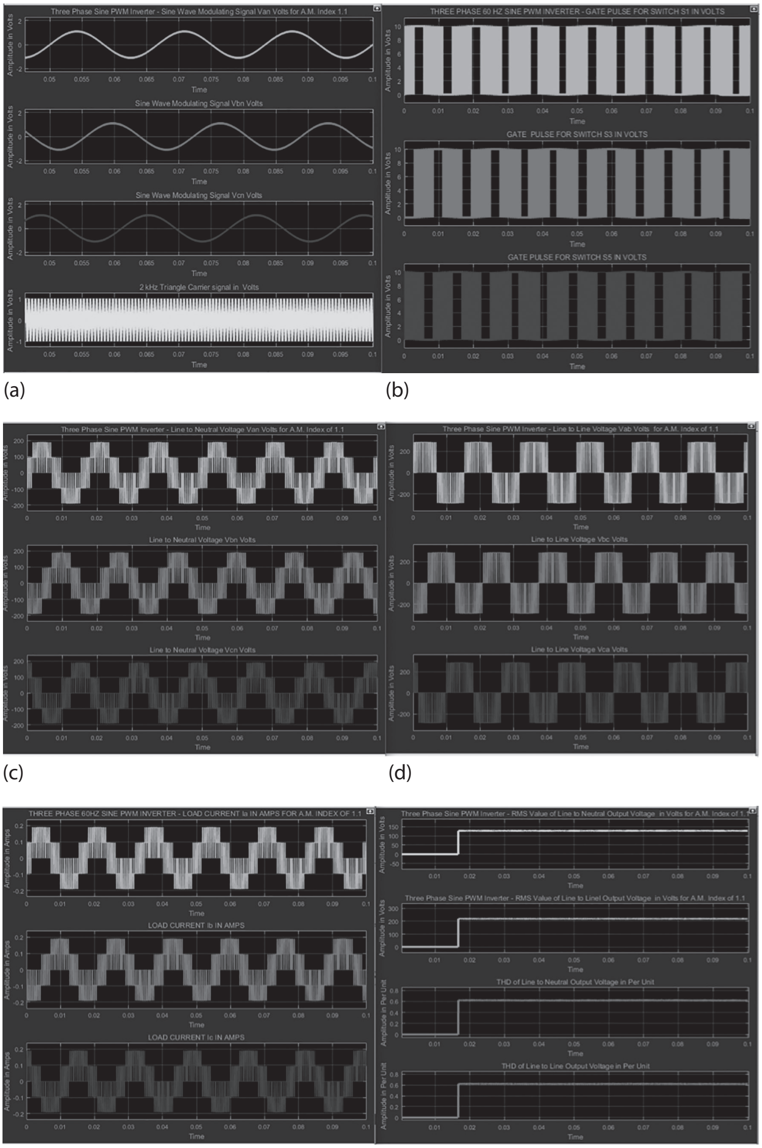
**FIGURE 10.67 (CONTINUED)**
(g) Harmonic spectrum of line-to-neutral voltage and (h) harmonic spectrum of line-to-line voltage.

The simulation for the component-level model of TPFLCHBI was carried out using the ode23t (mod. Stiff/Trapezoidal) solver [1]. The data used are the same as shown in Table 9.9. Simulation results for the three phase-to-ground voltages, load currents, RMS value and THD of phase-to-ground voltage are shown in Figure 10.72.

The harmonic spectrum of the phase-to-ground voltage is shown in Figure 10.73.

Simulation results are tabulated in Table 10.17.

Simulation results in Table 10.17 agree well with those shown in Table 9.9 and the derivation in Section 9.6.



(a) (b)

(c) (d)

(e) (f)

**FIGURE 10.68**
(a–f) Three-phase sine PWM inverter component-level simulation. (a) Three-phase sine modulating signal and triangle carrier (left). (b) Three-phase PWM gate pulse for upper arm switches of inverter (right). (c) Three-phase line-to-neutral output voltage (left). (d) Three-phase line-to-line output voltage (right). (e) Three-phase load current (left). (f) RMS value and THD of line-to-neutral and line-to-line output voltages (right).

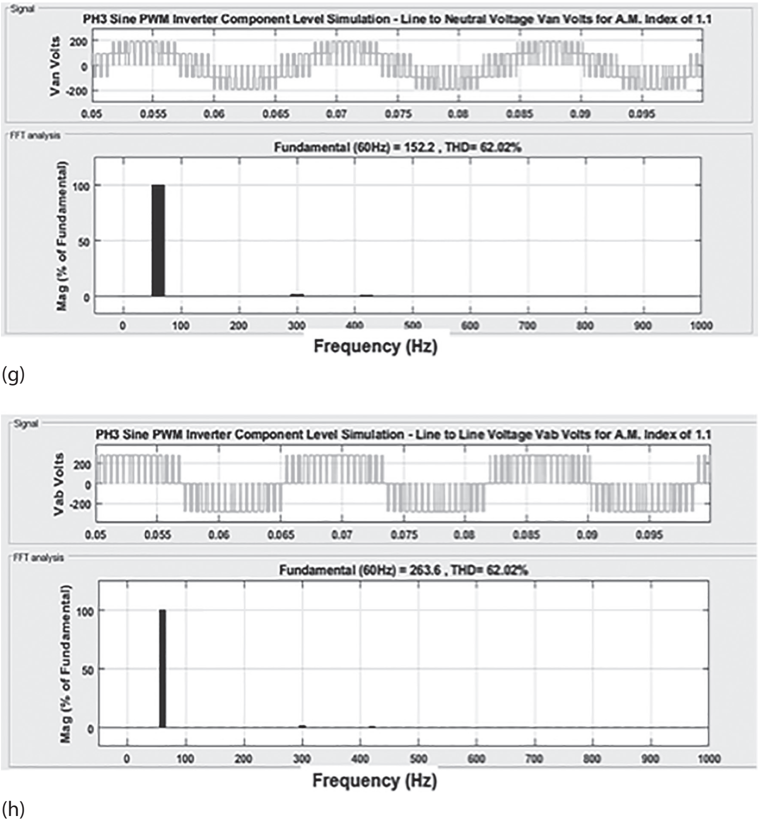


**FIGURE 10.68 (CONTINUED)**
(g, h) Three-phase sine PWM VSI component-level simulation: harmonic spectrum of (g) $V_{an}$ and (h) $V_{ab}$ for AM index of 1.1.

**TABLE 10.16**

Three-Phase Sine PWM Inverter: Component-Level Simulation Results

| Sl. No. | DC Link Voltage (V) | AM Index | RMS $V_{ab}$ (V) | THD $V_{ab}$ Per Unit | RMS $V_{an}$ (V) | THD $V_{an}$ Per Unit |
|---|---|---|---|---|---|---|
| 1 | 286 | 0.9 | 201.8 | 0.7923 | 116.3 | 0.7944 |
| 2 | 286 | 1.1 | 219.8 | 0.6178 | 126.6 | 0.6187 |

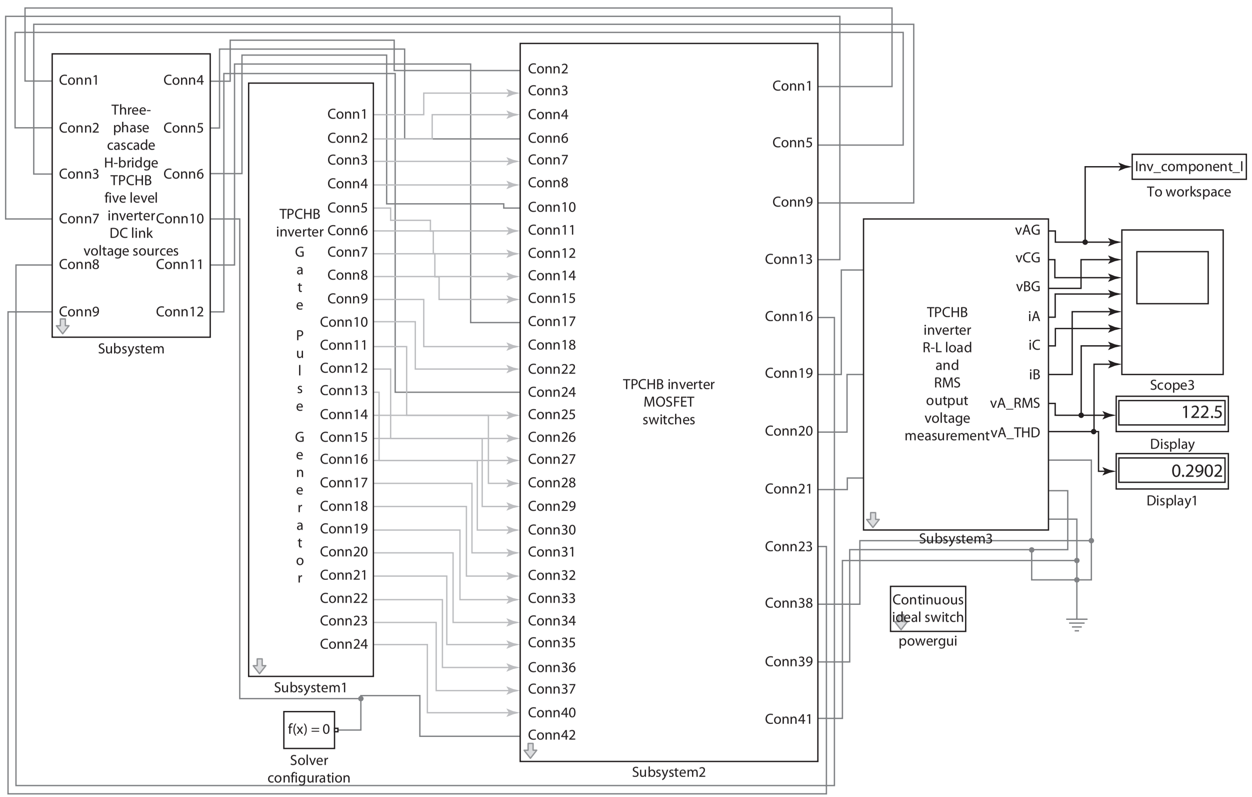
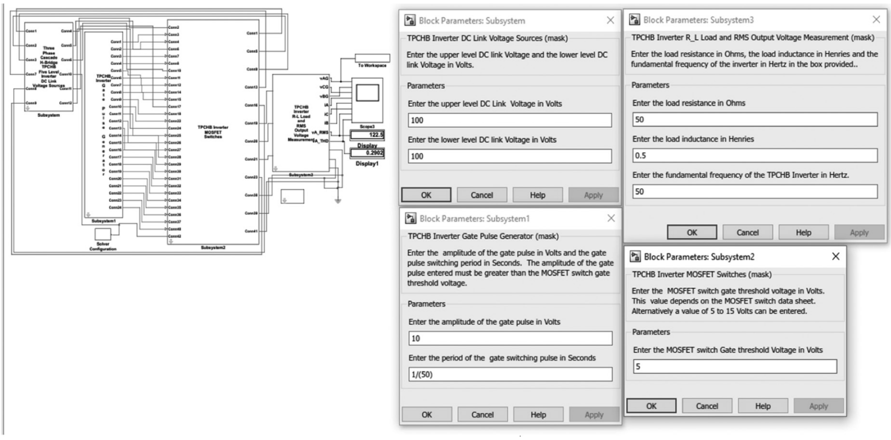

Conn1
Conn2
Conn3
Conn7
Conn8
Conn9
Three-
phase
cascade
H-bridge
TPCHB
five level
inverter
DC link
voltage sources
Conn4
Conn5
Conn6
Conn10
Conn11
Conn12
Subsystem
TPCHB
inverter
Gate Pulse Generator
Conn1
Conn2
Conn3
Conn4
Conn5
Conn6
Conn7
Conn8
Conn9
Conn10
Conn11
Conn12
Conn13
Conn14
Conn15
Conn16
Conn17
Conn18
Conn19
Conn20
Conn21
Conn22
Conn23
Conn24
Subsystem1
f(x) = 0
Solver
configuration
Conn2
Conn3
Conn4
Conn6
Conn7
Conn8
Conn10
Conn11
Conn12
Conn14
Conn15
Conn17
Conn18
Conn22
Conn24
Conn25
Conn26
Conn27
Conn28
Conn29
Conn30
Conn31
Conn32
Conn33
Conn34
Conn35
Conn36
Conn37
Conn40
Conn42
TPCHB inverter
MOSFET
switches
Conn1
Conn5
Conn9
Conn13
Conn16
Conn19
Conn20
Conn21
Conn23
Conn38
Conn39
Conn41
Subsystem2
TPCHB
inverter
R-L load
and
RMS
output
voltage
measurement
vAG
vCG
vBG
iA
iC
iB
vA_RMS
vA_THD
Subsystem3
Continuous
ideal switch
powergui
Inv_component_I
To workspace
Scope3
122.5
Display
0.2902
Display1

**FIGURE 10.69**
TPFLCHBI model.


Three Phase Cascade H-Bridge TPCHB Five Level Inverter DC Link Voltage Sources
Subsystem
TPCHB Inverter Gate Pulse Generator
Subsystem1
Solver Configuration
TPCHB Inverter MOSFET Switches
Subsystem2
TPCHB Inverter R-L Load and RMS Output Voltage Measurement
vAG
vCG
vBG
iA
iC
iB
vA_RMS
vA_THD
Subsystem3
To Workspace
Scope3
122.5
Display
0.2902
Display1

Block Parameters: Subsystem

TPCHB Inverter DC Link Voltage Sources (mask)

Enter the upper level DC link Voltage and the lower level DC link Voltage in Volts.

Parameters

Enter the upper level DC Link Voltage in Volts: 100

Enter the lower level DC link Voltage in Volts: 100

Block Parameters: Subsystem3

TPCHB Inverter R_L Load and RMS Output Voltage Measurement (mask)

Enter the load resistance in Ohms, the load inductance in Henries and the fundamental frequency of the inverter in Hertz in the box provided..

Parameters

Enter the load resistance in Ohms: 50

Enter the load inductance in Henries: 0.5

Enter the fundamental frequency of the TPCHB Inverter in Hertz.: 50

Block Parameters: Subsystem1

TPCHB Inverter Gate Pulse Generator (mask)

Enter the amplitude of the gate pulse in Volts and the gate pulse switching period in Seconds. The amplitude of the gate pulse entered must be greater than the MOSFET switch gate threshold voltage.

Parameters

Enter the amplitude of the gate pulse in Volts: 10

Enter the period of the gate switching pulse in Seconds: 1/(50)

Block Parameters: Subsystem2

TPCHB Inverter MOSFET Switches (mask)

Enter the MOSFET switch gate threshold voltage in Volts. This value depends on the MOSFET switch data sheet. Alternatively a value of 5 to 15 Volts can be entered.

Parameters

Enter the MOSFET switch Gate threshold Voltage in Volts: 5

OK
Cancel
Help
Apply

**FIGURE 10.70**
TPFLCHBI model with interactive blocks.

## 10.11 Pulse Width Modulation Methods for Multilevel Converters

Multi-carrier-based sine PWM techniques are classified as multi-carrier sine phase-shift PWM (MSPSPWM) and multi-carrier sine level shift PWM (MSLSPWM). These two PWM techniques for multilevel converters have already been presented in Section 9.7. In this section, details regarding the interactive component-level model development for these two PWM techniques are presented with model simulation results.

### 10.11.1 Multi-Carrier Sine Phase-Shift PWM

The system model of MSPSPWM is explained in Section 9.7.1. Here, the component-level model of MSPSPWM is presented. Figure 10.74 presents the component-level model of the MSPSPWM with an interactive dialogue box.

Figure 10.75 shows the internal subsystem with a dialogue box. In the dialogue box in Figure 10.74, the numerical data relating to triangle carrier frequency, angular phase-shift between four carriers, modulating signal amplitude and frequency in hertz and phase difference between three-phase sine-wave modulating signal are entered. The triangle carrier has a peak value of +1 V/–1 V.

In the model subsystem in Figure 10.75, for 'Triangle Generator' to 'Triangle Generator4', the frequency 'ftri', and phases 'phi*0' to 'phi*4' are entered. In the sine-wave generators marked 'Sine Wave1' to 'Sine Wave3', the amplitude is entered as 'A', the frequency is '2*pi*fm' rad/s and the phases 'theta*0*pi/180', 'theta*(–1)*pi/180' and 'theta*(–2)*pi/180' rad are entered. Phase shift 'phi' 90° creates four triangle carriers with a phase difference of 90° and peak

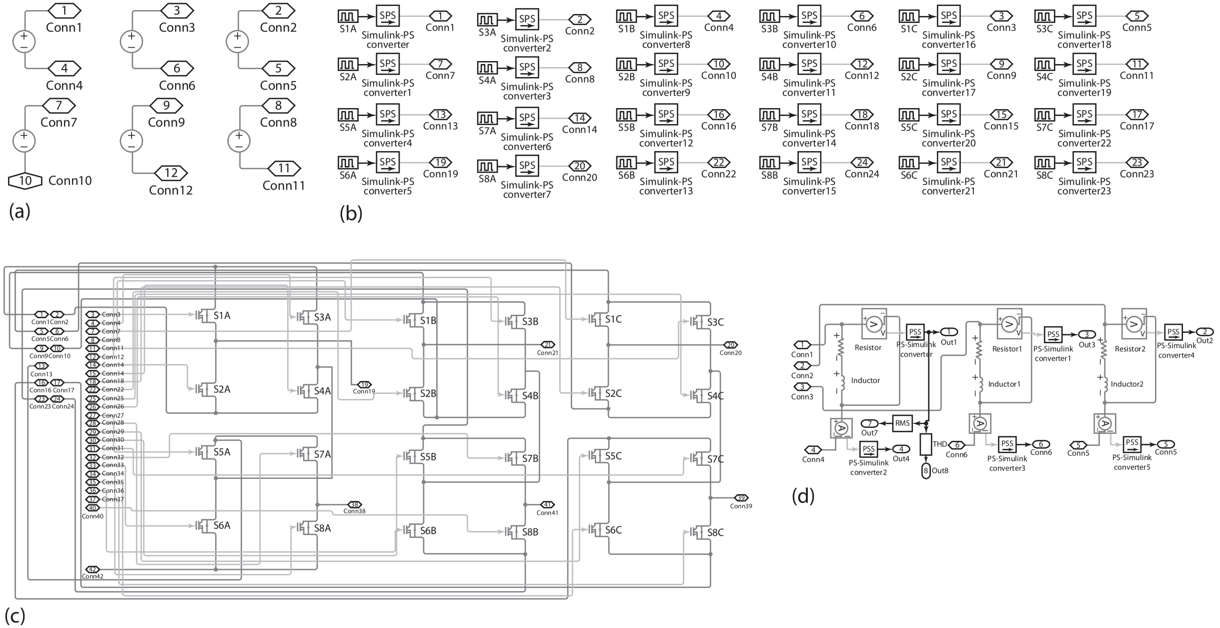

Conn1
Conn4
Conn7
Conn10
Conn3
Conn6
Conn9
Conn12
Conn2
Conn5
Conn8
Conn11
(a)
S1A Simulink-PS converter Conn1
S2A Simulink-PS converter1 Conn7
S5A Simulink-PS converter4 Conn13
S6A Simulink-PS converter5 Conn19
S3A Simulink-PS converter2 Conn2
S4A Simulink-PS converter3 Conn8
S7A Simulink-PS converter6 Conn14
S8A Simulink-PS converter7 Conn20
S1B Simulink-PS converter8 Conn4
S2B Simulink-PS converter9 Conn10
S5B Simulink-PS converter12 Conn16
S6B Simulink-PS converter13 Conn22
S3B Simulink-PS converter10 Conn6
S4B Simulink-PS converter11 Conn12
S7B Simulink-PS converter14 Conn18
S8B Simulink-PS converter15 Conn24
S1C Simulink-PS converter16 Conn3
S2C Simulink-PS converter17 Conn9
S5C Simulink-PS converter20 Conn15
S6C Simulink-PS converter21 Conn21
S3C Simulink-PS converter18 Conn5
S4C Simulink-PS converter19 Conn11
S7C Simulink-PS converter22 Conn17
S8C Simulink-PS converter23 Conn23
SPS
(b)
S1A
S2A
S5A
S6A
S3A
S4A
S7A
S8A
S1B
S2B
S5B
S6B
S3B
S4B
S7B
S8B
S1C
S2C
S5C
S6C
S3C
S4C
S7C
S8C
Conn19
Conn21
Conn20
Conn38
Conn41
Conn39
Conn40
Conn42
(c)
Conn1
Conn2
Conn3
Conn4
Resistor
Inductor
PS-Simulink converter
Out1
RMS
Out7
THD
Out8
PS-Simulink converter2
Out4
Resistor1
Inductor1
PS-Simulink converter1
Out3
PS-Simulink converter3
Conn6
Resistor2
Inductor2
PS-Simulink converter4
Out2
PS-Simulink converter5
Conn5
PSS
(d)

**FIGURE 10.71**
(a–d) TPFLCHBI model subsystems. (a) Voltage sources. (b) TPFLCHBI gate pulse generator. (c) TPFLCHBI MOSFET switches. (d) TPFLCHBI R–L load.

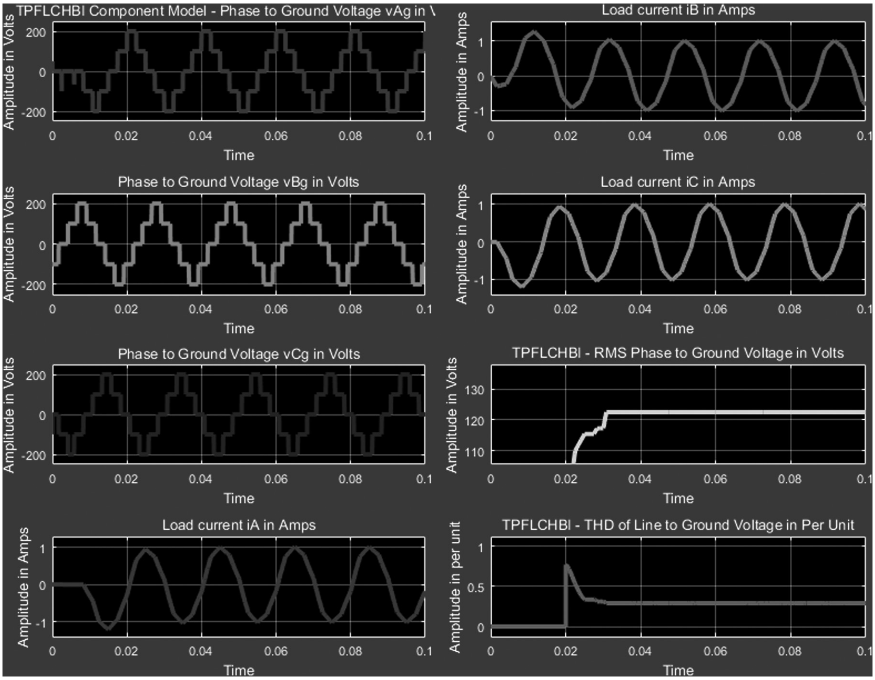


**FIGURE 10.72**
TPFLCHBI component-level model: simulation results.

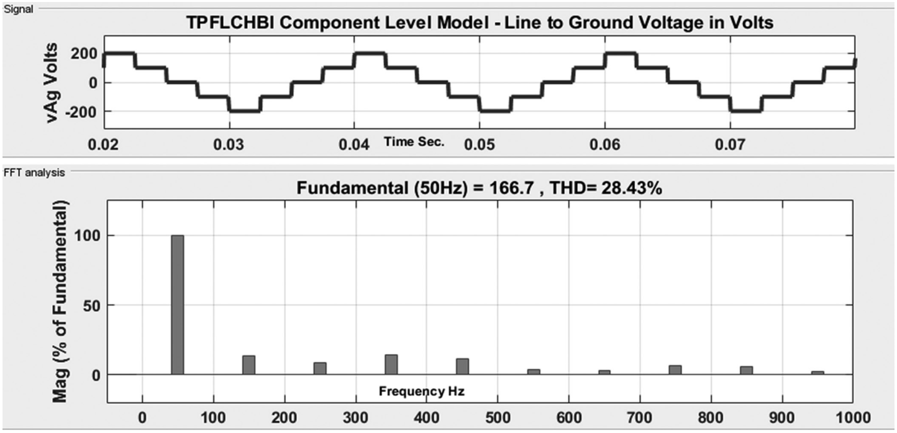


**FIGURE 10.73**
TPFLCHBI component-level model: harmonic spectrum of line-to-ground voltage.

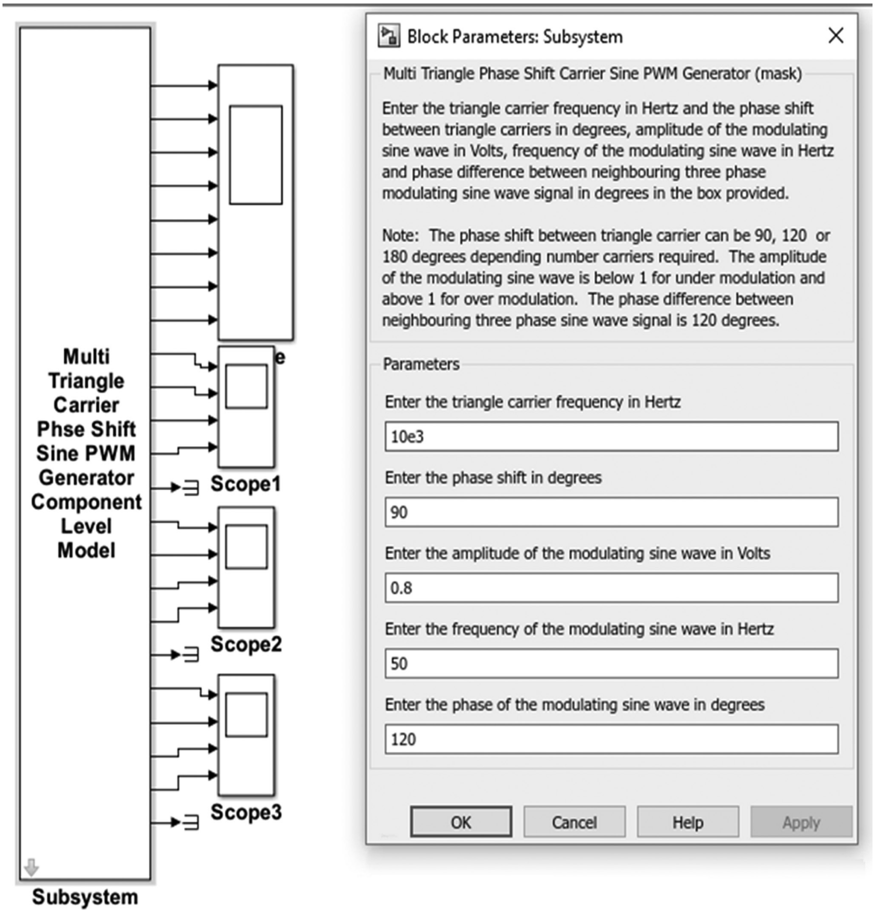
**TABLE 10.17**

TPFLCHBI: Component-Level Simulation Results

| Sl. No. | Symmetrical DC Link Voltage Source (V) | Frequency (Hz) | $V_{Ag}$ RMS (V) | $V_{Ag}$ THD (%) |
|---|---|---|---|---|
| 1 | 100 | 50 | 122.5 | 29.02 |

value +1 V/–1 V. The ftri value is 10 kHz, which is the triangle carrier frequency in hertz. For the sine-wave modulating signal, amplitude 'A' corresponds to 0.8 V, frequency 'fm' corresponds to 50 Hz, and 'theta' corresponds to 120°.

The output of each triangle generator is compared with the three-phase sine-wave modulating signal using Relational Operator blocks, as shown in Figure 10.75. As the op-amp model is *not* functioning, Relational Operator


Multi Triangle Carrier Phse Shift Sine PWM Generator Component Level Model
Subsystem
e
Scope1
Scope2
Scope3
OK
Cancel
Help
Apply

Block Parameters: Subsystem

Multi Triangle Phase Shift Carrier Sine PWM Generator (mask)

Enter the triangle carrier frequency in Hertz and the phase shift between triangle carriers in degrees, amplitude of the modulating sine wave in Volts, frequency of the modulating sine wave in Hertz and phase difference between neighbouring three phase modulating sine wave signal in degrees in the box provided.

Note: The phase shift between triangle carrier can be 90, 120 or 180 degrees depending number carriers required. The amplitude of the modulating sine wave is below 1 for under modulation and above 1 for over modulation. The phase difference between neighbouring three phase sine wave signal is 120 degrees.

Parameters

Enter the triangle carrier frequency in Hertz: 10e3

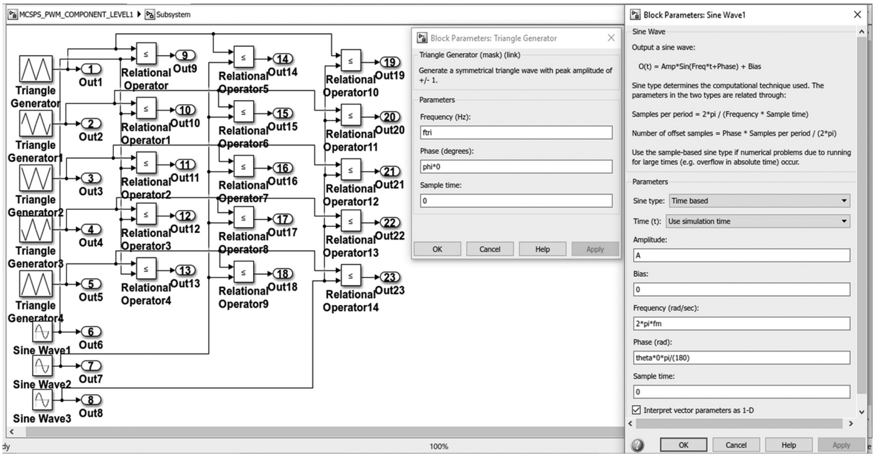
Enter the phase shift in degrees: 90

Enter the amplitude of the modulating sine wave in Volts: 0.8

Enter the frequency of the modulating sine wave in Hertz: 50

Enter the phase of the modulating sine wave in degrees: 120

**FIGURE 10.74**
Component-level model of MSPSPWM with interactive block.



Block Parameters: Triangle Generator

Triangle Generator (mask) (link)

Generate a symmetrical triangle wave with peak amplitude of +/- 1.

Parameters

Frequency (Hz): ftri

Phase (degrees): phi*0

Sample time: 0

Block Parameters: Sine Wave1

Sine Wave

Output a sine wave:

O(t) = Amp*Sin(Freq*t+Phase) + Bias

Sine type determines the computational technique used. The parameters in the two types are related through:

Samples per period = 2*pi / (Frequency * Sample time)

Number of offset samples = Phase * Samples per period / (2*pi)

Use the sample-based sine type if numerical problems due to running for large times (e.g. overflow in absolute time) occur.

Parameters

Sine type: Time based

Time (t): Use simulation time

Amplitude: A

Bias: 0

Frequency (rad/sec): 2*pi*fm

Phase (rad): theta*0*pi/(180)

Sample time: 0

☑ Interpret vector parameters as 1-D

MCSPS_PWM_COMPONENT_LEVEL1 ▸ Subsystem
Triangle Generator
Triangle Generator1
Triangle Generator2
Triangle Generator3
Triangle Generator4
Sine Wave1
Sine Wave2
Sine Wave3
Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out8
Relational Operator
Relational Operator1
Relational Operator2
Relational Operator3
Relational Operator4
Relational Operator5
Relational Operator6
Relational Operator7
Relational Operator8
Relational Operator9
Relational Operator10
Relational Operator11
Relational Operator12
Relational Operator13
Relational Operator14
Out9
Out10
Out11
Out12
Out13
Out14
Out15
Out16
Out17
Out18
Out19
Out20
Out21
Out22
Out23
100%
OK
Cancel
Help
Apply

**FIGURE 10.75**
Subsystem of MSPSPWM component-level model.

blocks are used. Strictly, in a component-level model, the triangular carrier output and the sine-wave modulating signal output are passed to the inverting and non-inverting pin of an Op-Amp Comparator block. The resulting output of the Relational Operator/Op-Amp comparator is the PWM gate pulse for the multilevel converter.

Simulation of the MSPSPWM component-level model was carried out using the ode23t (mod. stiff/trapezoidal) solver [1]. The simulation results for the four triangle carriers and three-phase modulating signals are shown in

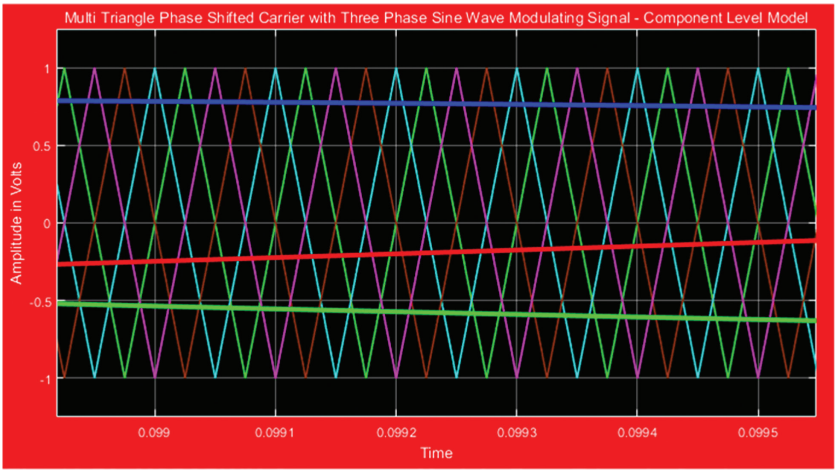


**FIGURE 10.76**
MSPSPWM component model: four triangle carriers and three-phase sine-wave modulating signal.

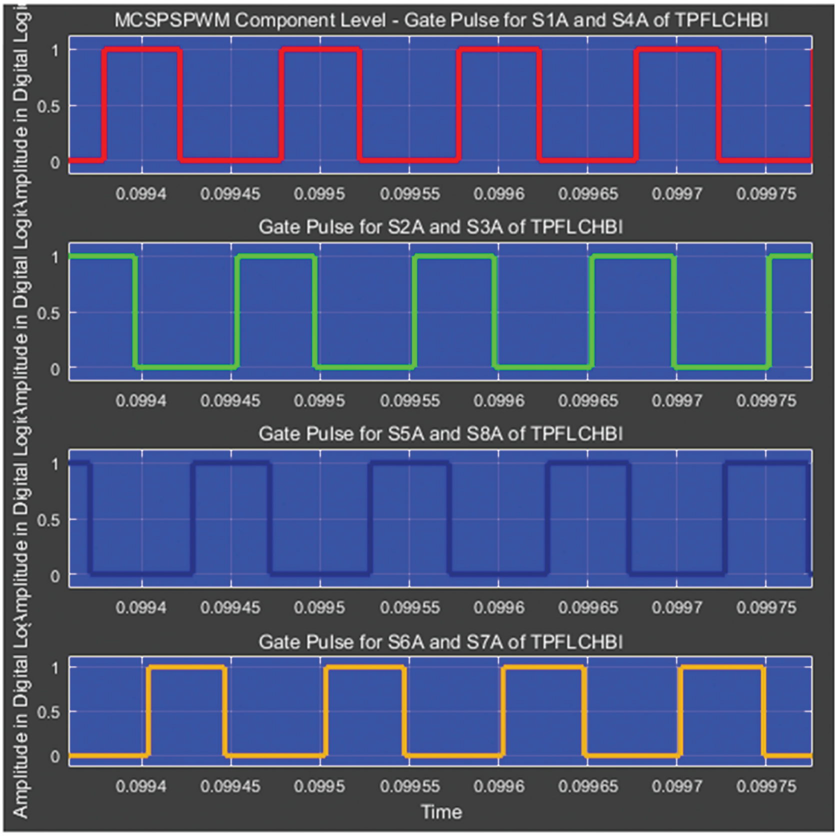


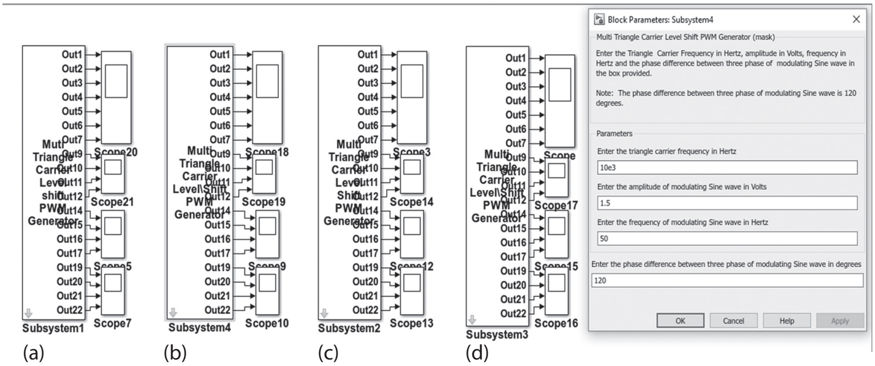
**FIGURE 10.77**
MSPSPWM component model: gate pulses for Phase A of TPFLCHBI.

Figure 10.76 and the gate pulses for Phase A of the TPFLCHBI are shown in Figure 10.77.

### 10.11.2 Multi-Carrier Sine Level Shift PWM

The details regarding the operation of the MSLSPWM method are explained in Section 9.7.3. In this section, details regarding the interactive component-level model of MSLSPWM are presented.

The model of the MSLSPWM generator is shown in Figure 10.78a–d with a dialogue box. Each model generates four different triangle carrier patterns. The internal subsystem of the model is shown in Figure 10.79 with a dialogue box, which corresponds to Figure 10.78b. In the dialogue box in Figure 10.78, the values entered are 10 kHz for the triangle carrier frequency, 1.5 V and 50 Hz for the sine-wave modulating signal amplitude and frequency, and 120° for the phase difference between three-phase sine-wave modulating signals.


Out1
Out2
Out3
Out4
Out5
Out6
Out7
Out9
Out10
Out11
Out12
Out14
Out15
Out16
Out17
Out19
Out20
Out21
Out22
Multi Triangle Carrier Level Shift PWM Generator
Scope20
Scope21
Scope5
Scope7
Subsystem1
Scope18
Scope19
Scope9
Scope10
Subsystem4
Scope3
Scope14
Scope12
Scope13
Subsystem2
Scope
Scope17
Scope15
Scope16
Subsystem3
(a)
(b)
(c)
(d)
OK
Cancel
Help
Apply

Block Parameters: Subsystem4

Multi Triangle Carrier Level Shift PWM Generator (mask)

Enter the Triangle Carrier Frequency in Hertz, amplitude in Volts, frequency in Hertz and the phase difference between three phase of modulating Sine wave in the box provided.

Note: The phase difference between three phase of modulating Sine wave is 120 degrees.

Parameters

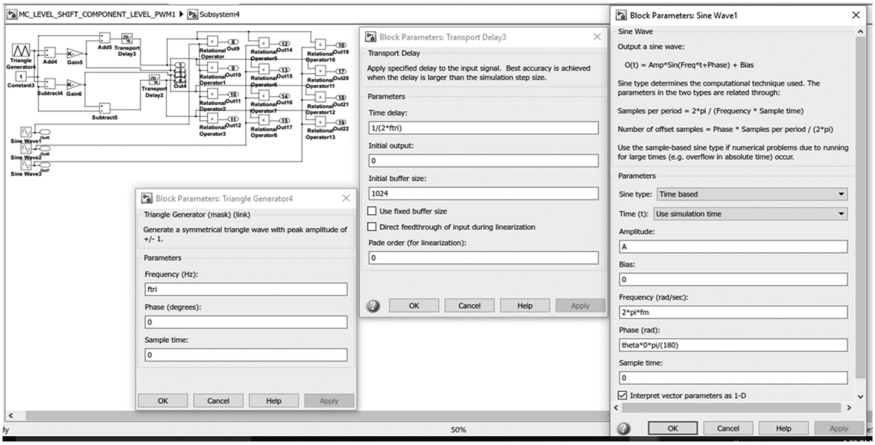
Enter the triangle carrier frequency in Hertz: 10e3

Enter the amplitude of modulating Sine wave in Volts: 1.5

Enter the frequency of modulating Sine wave in Hertz: 50

Enter the phase difference between three phase of modulating Sine wave in degrees: 120

**FIGURE 10.78**
Multi-carrier level-shift PWM generator with interactive block.


MC_LEVEL_SHIFT_COMPONENT_LEVEL_PWM1 ▸ Subsystem4
Triangle Generator4
Constant3
Add4
Gain5
Subtract4
Gain6
Add5
Transport Delay3
Transport Delay2
Subtract5
Relational Operator
Relational Operator1
Relational Operator2
Relational Operator3
Relational Operator5
Relational Operator6
Relational Operator7
Relational Operator8
Relational Operator10
Relational Operator11
Relational Operator12
Relational Operator13
Out9
Out10
Out11
Out12
Out14
Out15
Out16
Out17
Out19
Out20
Out21
Out22
Sine Wave1
Sine Wave2
Sine Wave3
50%
OK
Cancel
Help
Apply

Block Parameters: Transport Delay3

Transport Delay

Apply specified delay to the input signal. Best accuracy is achieved when the delay is larger than the simulation step size.

Parameters

Time delay: 1/(2*ftri)

Initial output: 0

Initial buffer size: 1024

☐ Use fixed buffer size

☐ Direct feedthrough of input during linearization

Pade order (for linearization): 0

Block Parameters: Triangle Generator4

Triangle Generator (mask) (link)

Generate a symmetrical triangle wave with peak amplitude of +/- 1.

Parameters

Frequency (Hz): ftri

Phase (degrees): 0

Sample time: 0

Block Parameters: Sine Wave1

Sine Wave

Output a sine wave:

O(t) = Amp*Sin(Freq*t+Phase) + Bias

Sine type determines the computational technique used. The parameters in the two types are related through:

Samples per period = 2*pi / (Frequency * Sample time)

Number of offset samples = Phase * Samples per period / (2*pi)

Use the sample-based sine type if numerical problems due to running for large times (e.g. overflow in absolute time) occur.

Parameters

Sine type: Time based

Time (t): Use simulation time

Amplitude: A

Bias: 0

Frequency (rad/sec): 2*pi*fm

Phase (rad): theta*0*pi/(180)

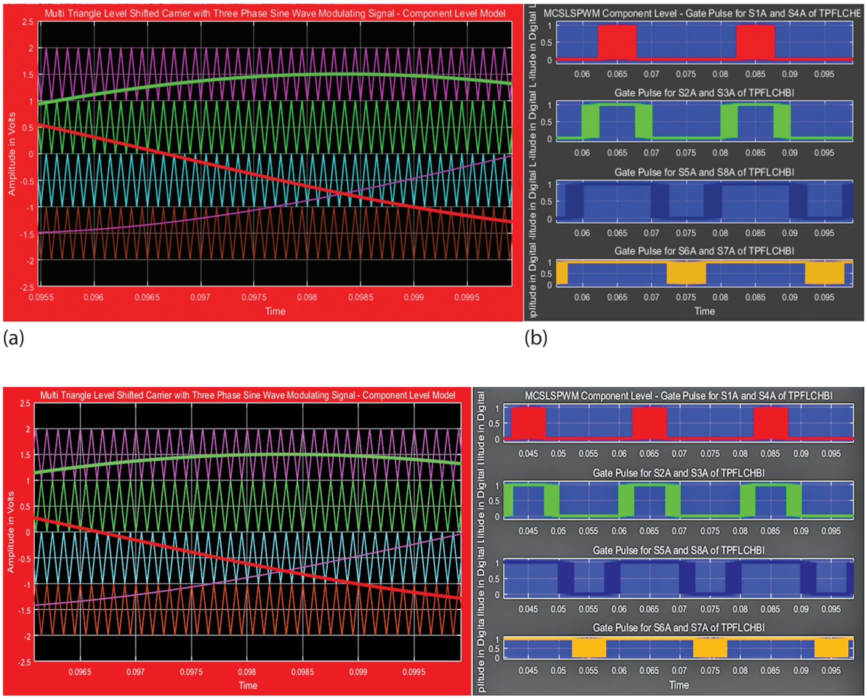
Sample time: 0

☑ Interpret vector parameters as 1-D

**FIGURE 10.79**
MSLSPWM generator subsystem.

Similarly, in Figure 10.79, in the dialogue box for ‘Triangle Generator4’, the frequency in hertz is entered as ‘ftri’. The time delay in the ‘Transport Delay2’ and ‘Transport Delay3’ dialogue boxes is entered as ‘1/(2*ftri)’. The amplitude, frequency and phase are entered in the ‘Sine Wave1’ generator as ‘A’, ‘2*pi*fm’ and ‘theta*0*pi/(180)’. For Sine Wave2 and 3, the phases entered are ‘theta*(–1)*pi/(180)’ and ‘theta*(–2)*pi/(180)’ with amplitude and frequency values the same as for Sine Wave1. When ‘ftri’ is entered as 10 kHz, the triangle generator generates a triangle carrier with frequency of 10 kHz and amplitude of +1 V/–1 V. Transport Delay2 and 3 provide a time delay of ‘1/(2*10e3)’ s. Sine Wave1, 2 and 3 output a three-phase sine wave with amplitude 1.5 V, frequency ‘fm’ corresponding to 50 Hz and phase ‘theta’ corresponding to zero, –120° and –240°, respectively. To obtain a triangle carrier with +1 V peak value and zero minimum value, the Triangle Generator4 output is added to 1 with a constant block, and this output is multiplied by 0.5 using the Gain block. To obtain a triangle carrier with –1 V peak and zero maximum value, the Triangle Generator4 output is subtracted from 1 in a constant block and multiplied by 0.5 using the Gain block. The triangle carrier with +1 V peak and zero minimum value is again added to 1 from a constant block and delayed in time by '1/(2*ftri)' to obtain the next higher level triangle carrier. Similarly, the triangle carrier with –1 V peak and maximum value zero is subtracted from 1 in a constant block and delayed in time by '1/(2*ftri)' to obtain the next lower level triangle carrier. This generates four triangle carriers with Pattern B in Figure 10.78. To obtain Pattern A for the triangle carrier, the two transport delays are removed. To obtain Pattern C for the triangle carrier, Transport Delay2 is connected to the output of the Gain6 block and for Pattern D, Transport Delay3 is connected to the output of the Gain6 block in Figure 10.79.

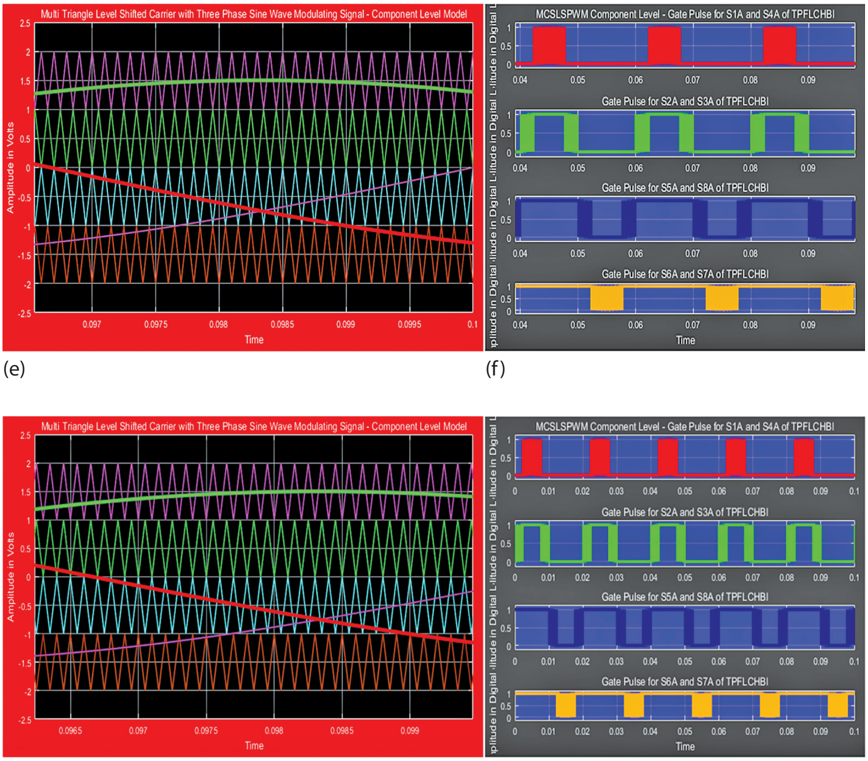
The four triangle carrier outputs are compared with modulating sine waves in each phase using Relational Operator blocks. As the op-amp module



(a) (b)

(c) (d)

**FIGURE 10.80**
MSLSPWM component level model. (a) Four triangle carriers in Pattern A with three-phase sine-wave modulating signal and (b) gate pulse for Phase A switches of TPFLCHBI. (c) Four Triangle carrier in Pattern B with three-phase wave modulating saignal. (d) Gate pulse for Phase A of TPFLCHBI.



(e) (f)

(g) (h)

**FIGURE 10.80 (CONTINUED)**
MSLSPWM component level model. (e) Four triangle carrier in Pattern C with three-phase since wave mudulating signal. (d) Gate pulse for Phase A switches of TPFLCHBI. (g) Four triangle carriers in Patteren D with three phase since wave modulating signal. (h) Gate pulse for Phase A switches of TPFLCHBI.

is *not* functioning, Relational Operator blocks are used in this component model. The output of the Relational Operator blocks are the gate pulses to the switches in each phase of the multilevel converter.

The simulation of the MSLSPWM generator component-level model was carried out using the ode23t (mod. stiff/trapezoidal) solver [1]. The simulation results for Patterns A to D in Figure 10.78 are shown in Figure 10.80a–h.

## 10.12 Conclusions

This chapter is exclusively dedicated to developing interactive component-level models for the power electronic converters such as AC to DC, DC to AC, DC to DC, AC to AC, buck SMPS, fourth-order DC to DC converters and three-phase DCTLI, FCTLI, TPFLCHBI, sine PWM, MSPSPWM and MSLSPWM, whose system models are presented and discussed in Chapters 3 to 9. The system models use ideal switches, whereas component-level models use semiconductor switches and components that are non-ideal. The results obtained by simulation of the component-level model for each power electronic converter are compared with those of their respective system model. The possible causes of discrepancies in the simulation results between these two types of model are presented.

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# 11

# *Interactive Model for and Real-Time Simulation of a Single-Phase Half H-Bridge Sine PWM Inverter*

## 11.1 Introduction

This chapter describes how Texas Instruments (TI) digital signal processor (DSP) TMS320F2812 can be used to generate pulse width modulation (PWM) gate drive output for the single-phase half H-bridge (SPHHB) inverter. This DSP has four main units: (1) internal and external bus; (2) central processing unit (CPU); (3) memory; and (4) peripherals [1]. The control algorithm is developed in MATLAB®/Simulink® using the Embedded coder block set; code generated using Real-Time Workshop (RTW) is compiled, debugged and transferred to the DSP board using Code Composer Studio (CCS) software.

CCS is an integrated design environment (IDE) that provides an environment for project development with all tools for real-time applications using only TI DSP. The program can be written either in Assembler or in C.

Experimental investigation of the gate drive, output voltage and current waveforms for an SPHHB inverter were studied using a Simulink model of the gate drive developed using Simulink and the Embedded coder block set interfaced to TI DSP TMS320F2812. Real-time simulation, known as a *software in the loop (SIL) simulation*, was conducted and the results are presented.

The experimental set-up consists of an eZdsp F2812 board, an SPHHB inverter and its gate drive modules. Here, the method of generating the PWM gate drive using a sine-triangle carrier is explained. This inverter was developed using silicon carbide (SiC) power MOSFETs.

## 11.2 Interactive Model of Single-Phase Half H-Bridge Sine PWM Inverter

The model of the SPHHB sine PWM inverter with interactive blocks developed using Simulink software is shown in Figure 11.1 [1–5]. These model subsystems are shown in Figure 11.2. Figure 11.2a–d are, respectively, sine-triangle carrier pulse width modulator, SPHHB MOSFET inverter, resistor and coupled coil inductor load, and output voltage and current measurement unit. In Figure 11.2a, the reference phase of the sine-wave modulating signal with frequency 400 Hz and peak value 0.5 V and a triangle carrier with frequency 20 kHz are compared in a relational operator block to generate gate pulses for the top switch S1 in Figure 11.2b. This output of the relational operator block is inverted using a NOT gate to generate gate pulses for the bottom switch S2 in Figure 11.2b. The DC link voltage is 60 V. The resistor, with value 15 Ω, and two coupled coil mutual inductors, each with 1 mH self-inductance and 0.9 coupling coefficient, shown in Figure 11.2c, form the load in series. Figure 11.2d shows the root mean square (RMS) output voltage and current measurement unit.

### 11.2.1 Simulation Results

Simulation of the model was carried out using the ode23t (mod. stiff/trapezoidal) solver [5]. The model simulation results are shown in Figure 11.3a–e, respectively.

## 11.3 Real-Time Software in the Loop Simulation

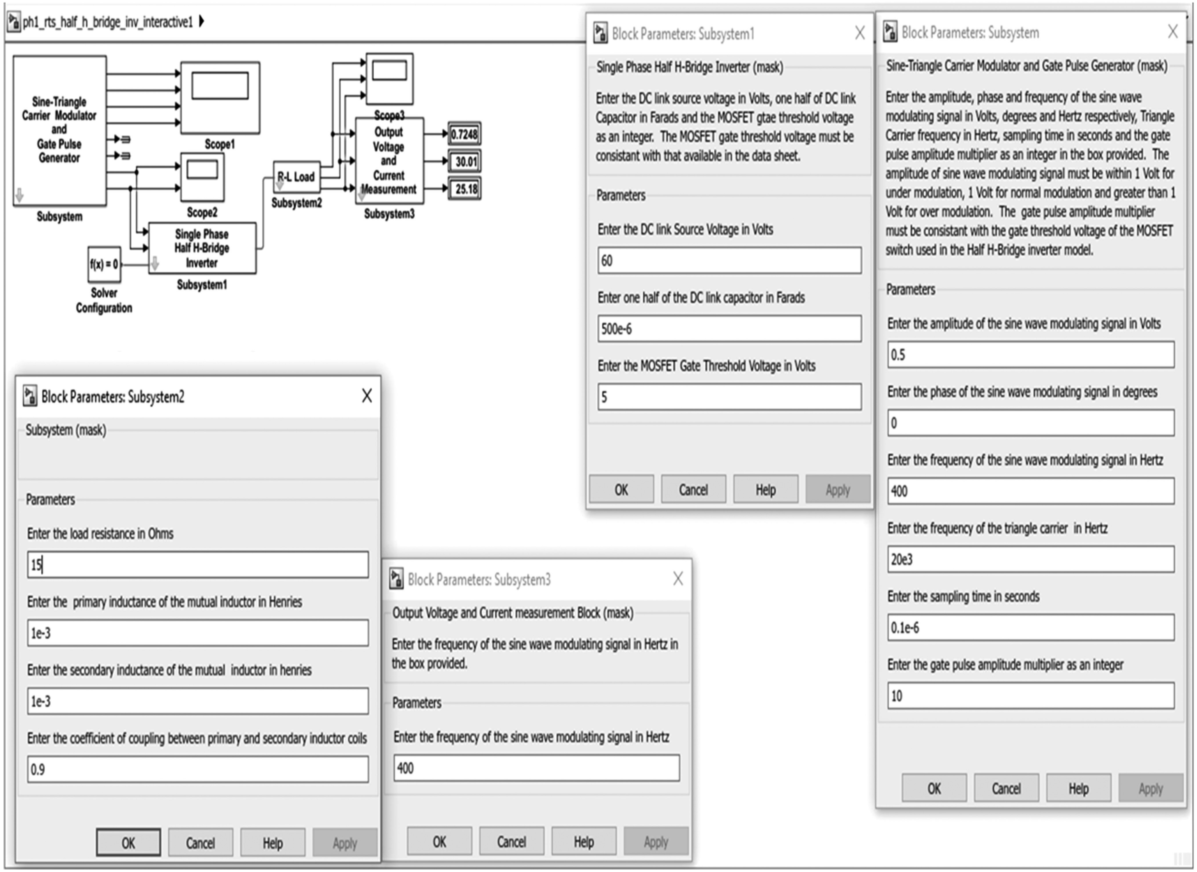
The real-time SIL simulation of the SPHHB sine PWM inverter was carried out using the model of the gate drive developed using the Simulink Sources and Embedded coder block set. The model build was carried out and the source code generated was compiled using CCS software. After compilation, the output file was downloaded to the memory of TI DSP TMS320F2812, which was interfaced using JTAG* to the computer in which the model was developed. The details of the TI DSP, CCS and the procedure used to generate the gate pulse, output voltage and current waveforms are explained in the following sections.

### 11.3.1 Digital Signal Processor

The DSP used was the one by Texas Instruments TI TMS320F2812 [6, 7]. This has four main units: (1) internal and external bus system; (2) CPU; (3) memory; (4) peripherals. The block diagram is shown in Figure 11.4a and the photograph in Figure 11.4b.

---

* JTAG is the cable used to communicate between the computer and the digital signal processor (DSP).


ph1_rts_half_h_bridge_inv_interactive1
Sine-Triangle Carrier Modulator and Gate Pulse Generator
Subsystem
Scope1
Scope2
Single Phase Half H-Bridge Inverter
Subsystem1
f(x) = 0
Solver Configuration
R-L Load
Subsystem2
Scope3
Output Voltage and Current Measurement
Subsystem3
0.7248
30.01
25.18
OK
Cancel
Help
Apply

Block Parameters: Subsystem2

Subsystem (mask)

Parameters

Enter the load resistance in Ohms

15

Enter the primary inductance of the mutual inductor in Henries

1e-3

Enter the secondary inductance of the mutual inductor in henries

1e-3

Enter the coefficient of coupling between primary and secondary inductor coils

0.9

Block Parameters: Subsystem3

Output Voltage and Current measurement Block (mask)

Enter the frequency of the sine wave modulating signal in Hertz in the box provided.

Parameters

Enter the frequency of the sine wave modulating signal in Hertz

400

Block Parameters: Subsystem1

Single Phase Half H-Bridge Inverter (mask)

Enter the DC link source voltage in Volts, one half of DC link Capacitor in Farads and the MOSFET gtae threshold voltage as an integer. The MOSFET gate threshold voltage must be consistant with that available in the data sheet.

Parameters

Enter the DC link Source Voltage in Volts

60

Enter one half of the DC link capacitor in Farads

500e-6

Enter the MOSFET Gate Threshold Voltage in Volts

5

Block Parameters: Subsystem

Sine-Triangle Carrier Modulator and Gate Pulse Generator (mask)

Enter the amplitude, phase and frequency of the sine wave modulating signal in Volts, degrees and Hertz respectively, Triangle Carrier frequency in Hertz, sampling time in seconds and the gate pulse amplitude multiplier as an integer in the box provided. The amplitude of sine wave modulating signal must be within 1 Volt for under modulation, 1 Volt for normal modulation and greater than 1 Volt for over modulation. The gate pulse amplitude multiplier must be consistant with the gate threshold voltage of the MOSFET switch used in the Half H-Bridge inverter model.

Parameters

Enter the amplitude of the sine wave modulating signal in Volts

0.5

Enter the phase of the sine wave modulating signal in degrees

0

Enter the frequency of the sine wave modulating signal in Hertz

400

Enter the frequency of the triangle carrier in Hertz

20e3

Enter the sampling time in seconds

0.1e-6

Enter the gate pulse amplitude multiplier as an integer

10

**FIGURE 11.1**
SPHHB PWM inverter with interactive blocks.

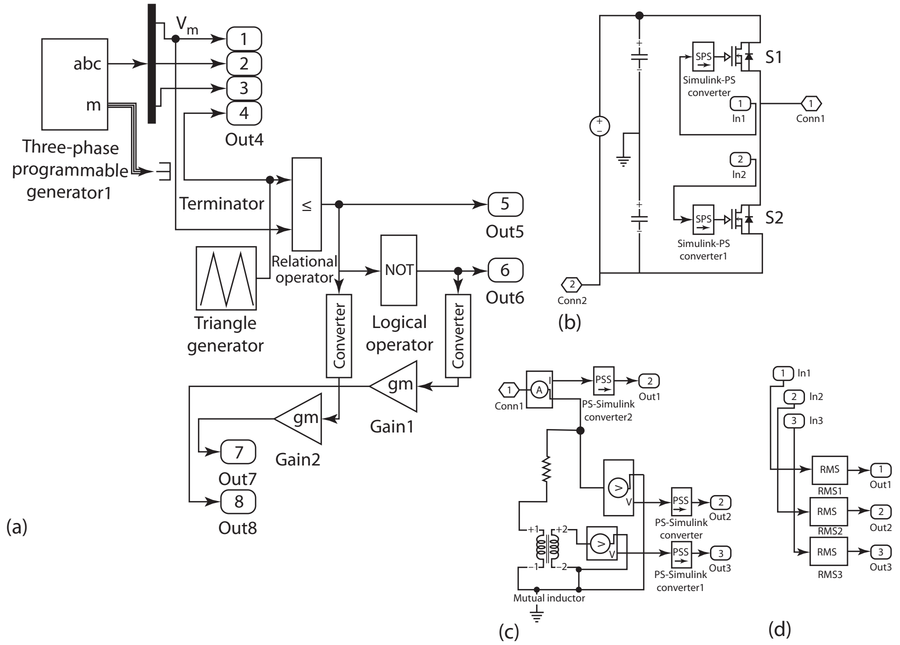

abc
m
Three-phase programmable generator1
Vm
1
2
3
4
Out4
Terminator
≤
Relational operator
Triangle generator
5
Out5
NOT
Logical operator
6
Out6
Converter
Converter
gm
Gain1
gm
Gain2
7
Out7
8
Out8
(a)
S1
SPS
Simulink-PS converter
1
In1
1
Conn1
2
In2
SPS
Simulink-PS converter1
S2
2
Conn2
(b)
1
Conn1
A
I
PSS
PS-Simulink converter2
2
Out1
V
PSS
PS-Simulink converter
2
Out2
+1
+2
−1
−2
V
PSS
PS-Simulink converter1
3
Out3
Mutual inductor
(c)
1 In1
2 In2
3 In3
RMS
RMS1
1
Out1
RMS
RMS2
2
Out2
RMS
RMS3
3
Out3
(d)

**FIGURE 11.2**
SPHHB PWM inverter model subsystems.

### 11.3.2 Code Composer Studio

The details regarding CCS are summarized as follows:

- Provides an environment for project development.
- Provides all tools required for real-time application using TI DSP.
- Programs can be written, compiled and executed either in C or in Assembler.
- Steps are Edit–Compile–Link, which are combined into Build and then Debug.
- Connects to the real-time hardware.
- Software design flow within CCS is shown in Figure 11.5.

### 11.3.3 Symmetric PWM Waveform Generation

Symmetric PWM waveform generation using TI DSP is given as follows:

1. Event managers:
    - The two event managers EVA and EVB provide a broad range of functions and have identical peripheral register sets.

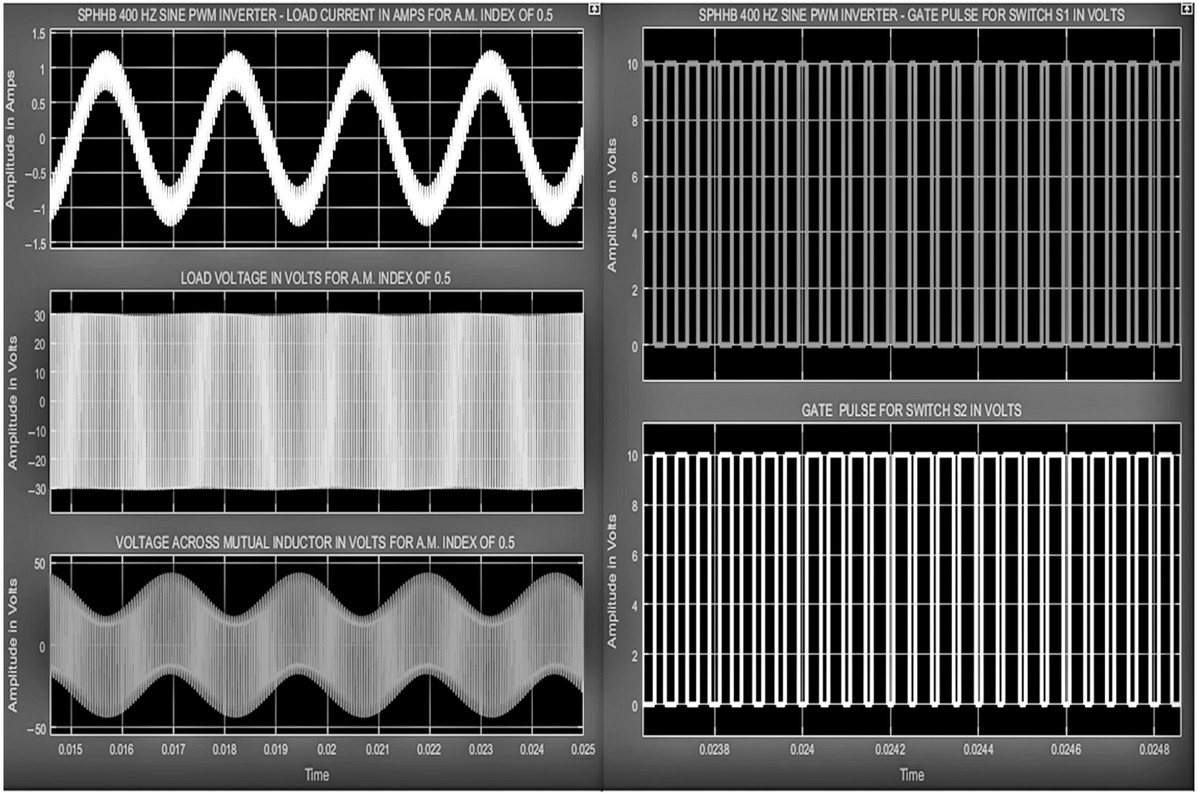


**FIGURE 11.3**
SPHHB sine PWM inverter: model simulation results. (a) Load current (left top). (b) Load voltage (left middle). (c) Voltage across mutual inductor (left bottom). (d) Switch S1 gate pulse (right top). (e) Switch S2 gate pulse (right bottom).

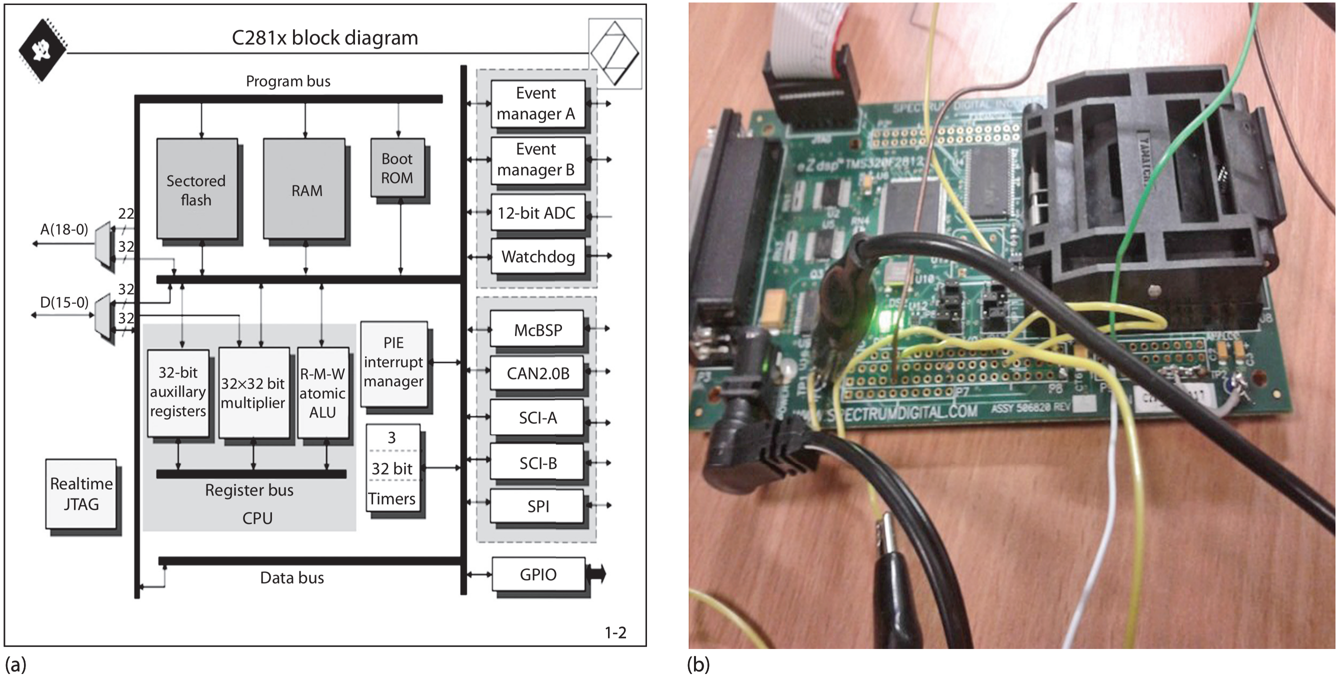

C281x block diagram
Program bus
Sectored flash
RAM
Boot ROM
A(18-0)
D(15-0)
22
32
32
32
32-bit auxillary registers
32×32 bit multiplier
R-M-W atomic ALU
PIE interrupt manager
3
32 bit
Timers
Register bus
CPU
Realtime JTAG
Data bus
Event manager A
Event manager B
12-bit ADC
Watchdog
McBSP
CAN2.0B
SCI-A
SCI-B
SPI
GPIO
1-2
(a)
(b)

**FIGURE 11.4**
TI DSP TMS 320F2812. (a) Block diagram. (b) Photograph.

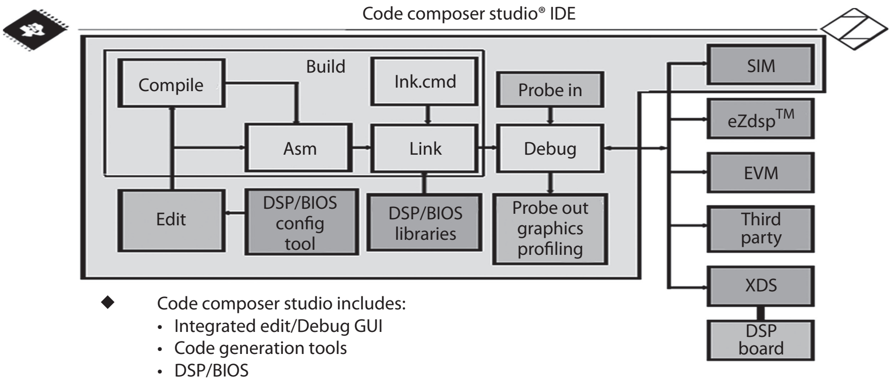

Code composer studio® IDE
Build
Compile
lnk.cmd
Probe in
Asm
Link
Debug
Edit
DSP/BIOS config tool
DSP/BIOS libraries
Probe out graphics profiling
SIM
eZdsp™
EVM
Third party
XDS
DSP board
◆ Code composer studio includes:
• Integrated edit/Debug GUI
• Code generation tools
• DSP/BIOS

**FIGURE 11.5**
Code Composer Studio: software design flow.

- Event manager (EV) modules include the following:
  - General-purpose (GP) timers.
  - Full compare/PWM units.
  - Capture units.
  - Quadrature encoder pulse (QEP) circuits.
- Each EV can control three half H-bridges.
- Each EV can provide complementary pair PWM control signals.

2. GP timers:
   - Two independent GP timers are available.
   - Provide time base for the operation of compare units and for the PWM circuits to generate PWM output.
   - One readable and writable (RW) 16-bit up/down counter register TxCNT ($x = 1, 2, 3, 4$).
   - TxCNT register stores current value of the count and keeps incrementing or decrementing depending on the direction of count.
   - One RW 16-bit timer compare register TxCMPR ($x = 1, 2, 3, 4$).
   - One RW 16-bit timer period register TxPR ($x = 1, 2, 3, 4$).
   - RW individual timer control register TxCON ($x = 1, 2, 3, 4$).
   - Programmable prescaler for internal and external clock inputs.
   - Control and interrupt logic.
   - One GP timer compare output pin TxCMP ($x = 1, 2, 3, 4$).
   - Output conditioning logic.
   - GPCONA/B indicates action to be taken by timers on different timer events. Also indicate counting direction of GP timers.

3. GP timer continuous UP/DOWN counting mode:
    - Figure 11.6 shows continuous UP/DOWN counting mode.
    - Counting direction changes from UP to DOWN when (1) period register value (TxPR) is reached or (2) the value FFFF h is reached if initial timer value is greater than period register value.
    - Counting direction changes from DOWN to UP when the timer value reaches zero.
    - Timer period is 2 * TxPR of the scaled clock input.
4. Symmetric PWM waveform generation:
    - In this mode (Figure 11.7), output waveform state is determined as shown as follows:
    - Zero before counting operation and unchanged until first compare match.
    - Toggles on first compare match and unchanged until second compare match.
    - Toggles on second compare match and unchanged until end of period.
    - Reset to zero at the end of period if there is *no* third compare match.

### 11.3.4 Sine-Triangle Carrier PWM Generation

- Here, the MATLAB/Simulink model developed using the Simulink Sources and Embedded Coder block set is used for gate pulse PWM waveform generation for the SPHHB inverter without deadband (Figure 11.8a) and with deadband (Figure 11.8b).
- Here, carrier period $Tc = 2 *$ (amplitude of carrier) * (CPU clock period).

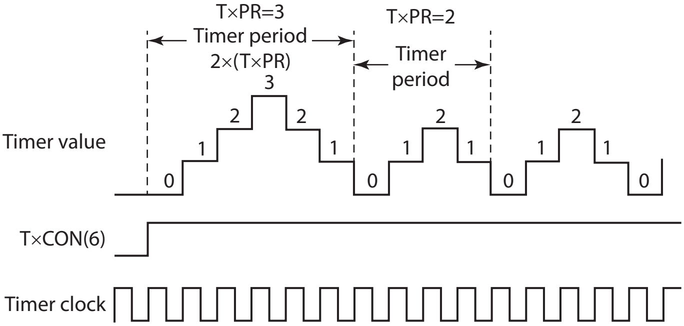


**FIGURE 11.6**
GP timer continuous UP/DOWN counting mode.

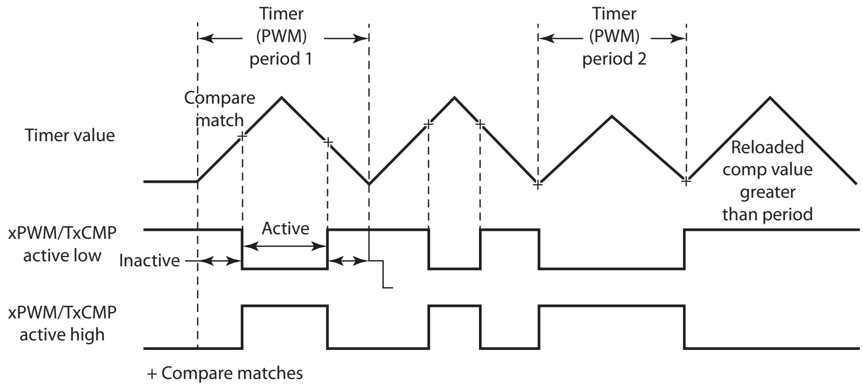
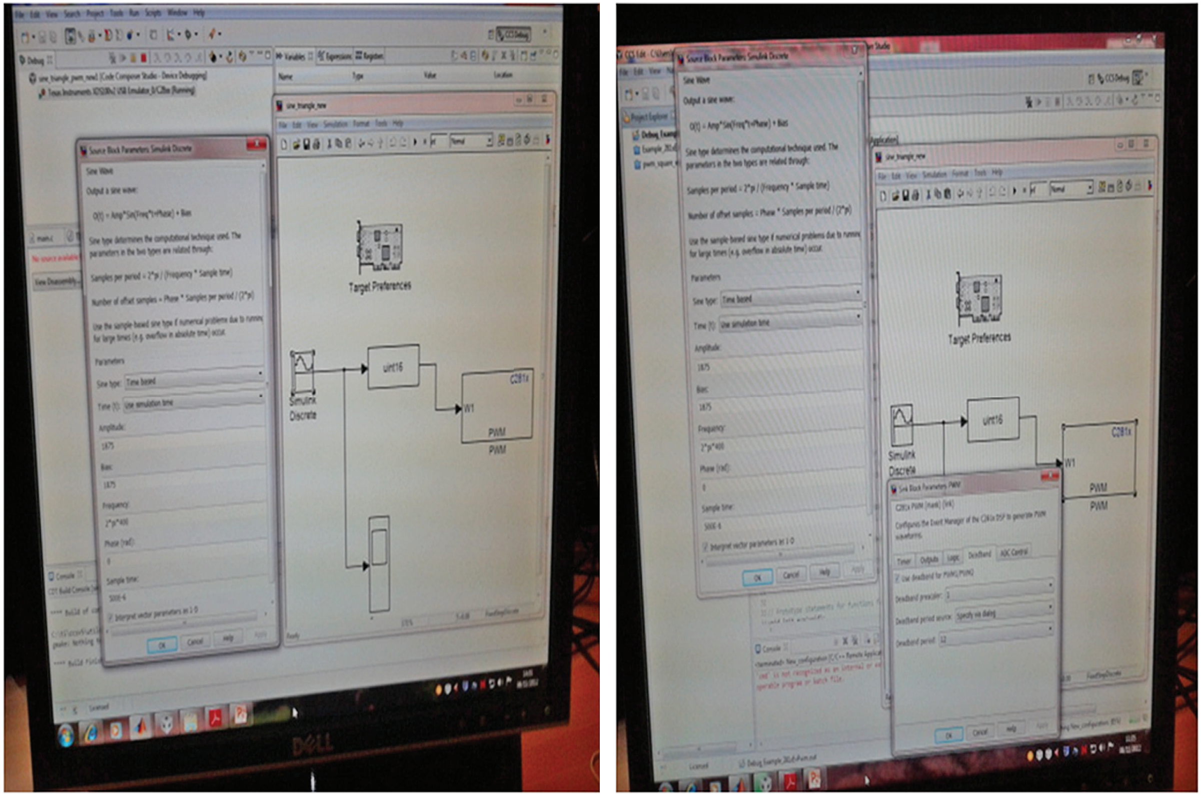

Timer (PWM) period 1
Timer (PWM) period 2
Compare match
Timer value
Reloaded comp value greater than period
xPWM/TxCMP active low
Active
Inactive
xPWM/TxCMP active high
+ Compare matches

**FIGURE 11.7**
GP timer compare PWM output in UP/DOWN counting mode.

- For carrier frequency 20 kHz and clock frequency 150 MHz, amplitude is 3750.
- Sine wave has to be in the positive quadrant. Hence, sine-wave amplitude is 3750/2, which is 1875. Sine-wave frequency is 400 Hz.
- Sine-wave offset/bias = 1875. Data type conversion uint16 is required, as eZDSP F2812 works with unsigned integer 16 data type.
- In the C281x PWM block shown in Figure 11.8a, module A, PWM period 3750, symmetric UP/DOWN, waveform period in clock cycles and PWM1/PWM2 outputs are selected. Deadband is selected in Figure 11.8b.
- In the target preferences, SD F2812 eZdsp, TI CCS v4 and CPU clock 150 MHz are selected.
- In the Simulink model (Figure 11.8a,b), press either Ctrl-b or go to menu Tools → Code Generation → Build Model.
- Simulink RTW generates the source code of the model.
- Turn on power supply to DSP and set target configurations from 'View' menu.
- The generated code from RTW is compiled and loaded to CCS.
- After compiling source code, 'projectname.out' is generated.
- This is loaded to DSP memory by clicking 'Load Program' from Run → Load menu.
- From 'Run' menu click 'Resume'.
- The gate drive experimental set-up is shown in Figure 11.9a and the gate drive waveform is shown in Figure 11.9b for 20 kHz triangle carrier and 400 Hz sine-wave frequency with *no* deadband. The gate


Target Preferences
Simulink
Discrete
uint16
W1
C281x
PWM
PWM

(a) (b)

**FIGURE 11.8**
SPHHB sine PWM inverter gate drive model (a) without deadband and (b) with deadband.

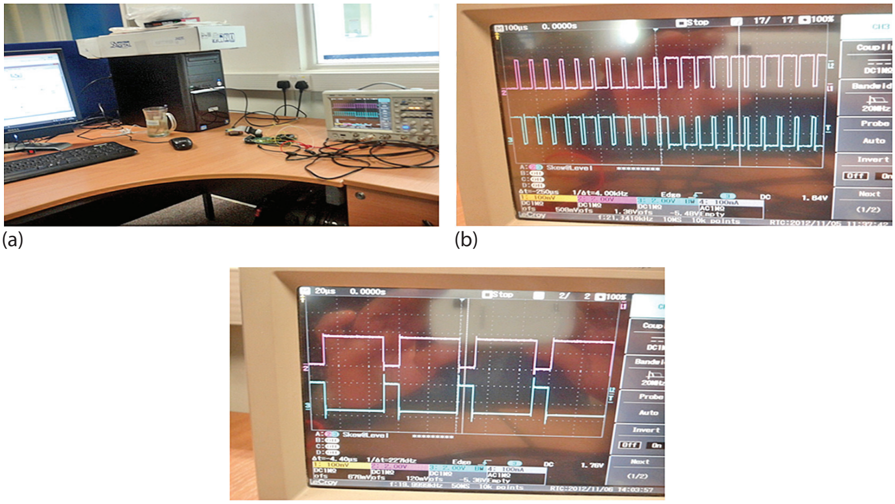

(a)
(b)
(c)

**FIGURE 11.9**
SPHHB sine PWM inverter gate drive experimental set-up and gate drive waveforms. (a) Experimental set-up. (b) Gate drive with no deadband. (c) Gate drive with deadband.

drive experimental result for a deadband prescale 1 and deadband period 12 is shown in Figure 11.9c [8].

- The experimental set-up of the SPHHB sine PWM 400 Hz inverter built using SiC power MOSFETs is shown in Figure 11.10 for the case with R–L Load.
- The output voltage and load current waveform of the SPHHB sine PWM inverter are shown in Figure 11.11a,b for the case with R–L load.

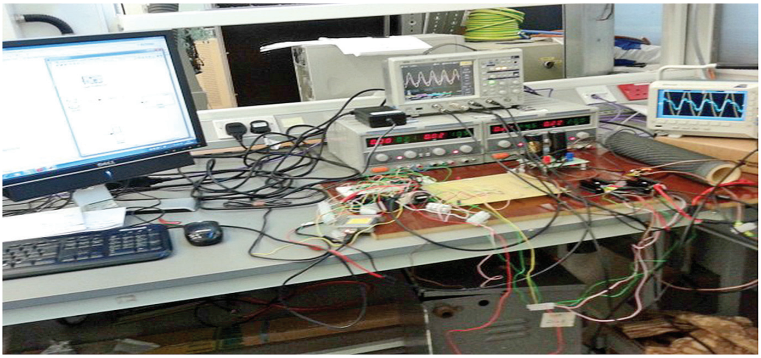
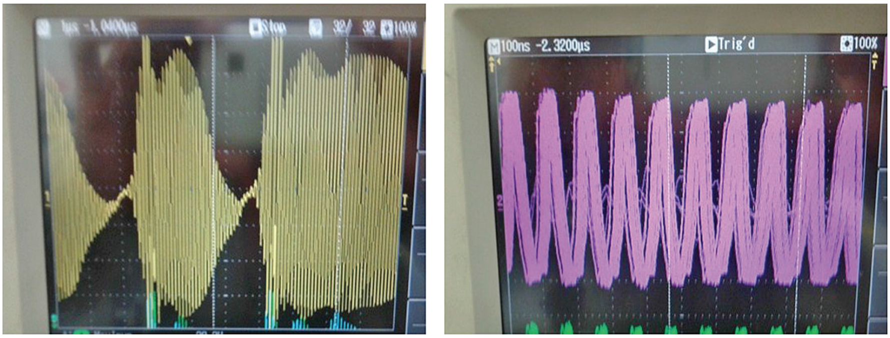


**FIGURE 11.10**
SPHHB sine PWM 400 Hz inverter experimental set-up.



(a) (b)

**FIGURE 11.11**
SPHHB sine PWM 400 Hz inverter output voltage and load current waveforms. (a) Output voltage. (b) Load current.

- The load current waveform must be divided by 15 to obtain actual load current.
- The experimental set-up of the SPHHB sine PWM 400 Hz inverter built using SiC power MOSFETs is shown in Figure 11.12a and the output voltage waveform is shown in Figure 11.12b for the case with purely resistive load.

## 11.4 Conclusions

Comparison of the gate drive waveform by model simulation shown in Figure 11.3d, e agree well with that shown in Figure 11.9b by real-time SIL simulation. Comparison of the load current waveform by model simulation shown in Figure 11.3a has some agreement with that by real-time SIL simulation shown in Figure 11.11b. The output voltage waveform by model simulation shown in Figure 11.3b has no perfect match with that by real-time SIL simulation shown in Figure 11.11a. One possible reason may be in the experimental set-up shown in Figure 11.10; the mutual inductor coil flux may be leaking to the surrounding atmosphere, whereas such an effect of leakage flux could not be incorporated in the interactive model shown Figure 11.1. Also, in Figure 11.3g, the load voltage waveform matches well with the one shown in Figure 11.12b by real-time SIL simulation.

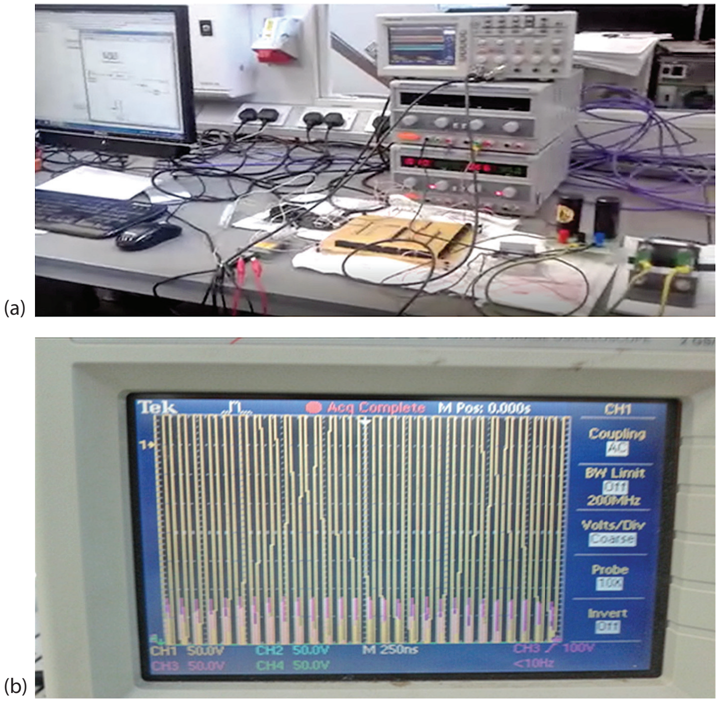

(a)
(b)
Tek
Acq Complete
M Pos: 0.000s
CH1
Coupling
AC
BW Limit
Off
200MHz
Volts/Div
Coarse
Probe
10X
Invert
Off
1
CH1 50.0V
CH2 50.0V
M 250ns
CH3 ∕ 100V
CH3 50.0V
CH4 50.0V
<10Hz

**FIGURE 11.12**
(a) SPHHB sine PWM inverter experimental set-up for purely resistive load. (b) Output voltage.

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